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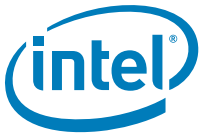
Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	Xeon E5645
Number of Cores/Bus Width	6 Core, 64-Bit
Speed	2.4GHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	-
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	-
Operating Temperature	-
Security Features	-
Package / Case	1366-LGA
Supplier Device Package	1366-LGA
Purchase URL	https://www.e-xfl.com/product-detail/advantech/96mpxe-2-4-12m13t1



1.4 References

Platform designers are strongly encouraged to maintain familiarity with the most up-to-date revisions of processor and platform collateral.

Table 1-2. References

Document	Location / Document#[1]	Notes
Advanced Configuration and Power Interface Specification	www.acpi.info.	
Compact Electronics Bay Specification: A Server System Infrastructure (SSI) Specification for Value Servers and Workstations	www.ssiforum.org	
Electronics Bay Specification for 2008 Servers and Workstation		
Entry-Level Electronics-Bay Specifications: A Server System Infrastructure (SSI) Specification for Entry Pedestal Servers and Workstations		
Thin Electronics Bay Specification: A Server System Infrastructure (SSI) Specification for Rack-Optimized Servers		
Intel® 64 and IA-32 Architecture Software Developer's Manual • *Volume 1: Basic Architecture* • *Volume 2A: Instruction Set Reference, A-M* • *Volume 2B: Instruction Set Reference, N-Z* • *Volume 3A: System Programming Guide, Part 1* • *Volume 3B: Systems Programming Guide, Part 2*	 253665 253666 253667 253668 253669	1
Intel® 64 and IA-32 Architectures Optimization Reference Manual	248966	1
Intel® Xeon® Processor 5600 Series Datasheet, Volume 2	323370	1
Intel® Xeon® Processor 5500/5600 Series Thermal/Mechanical Design Guidelines	323371	1

Notes:
1. Document is available publicly at http://www.intel.com.

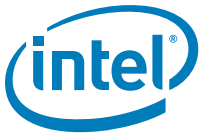
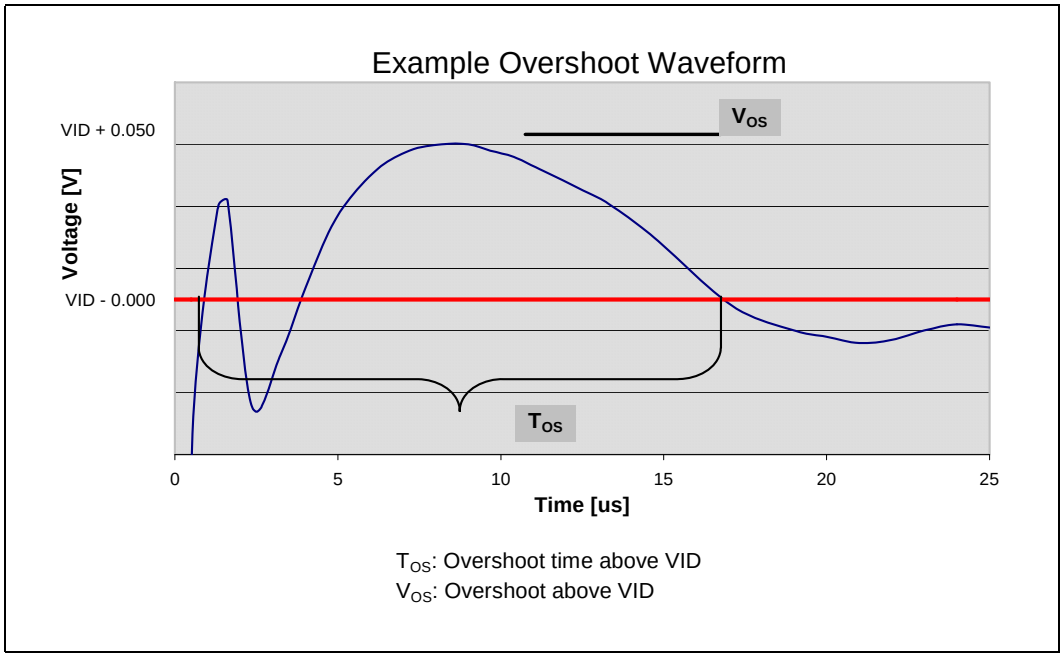


Table 2-2. Voltage Identification Definition (Sheet 3 of 6)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	V_{CC_MAX}
0	0	1	1	0	1	1	0	1.27500
0	0	1	1	0	1	1	1	1.26875
0	0	1	1	1	0	0	0	1.26250
0	0	1	1	1	0	0	1	1.25625
0	0	1	1	1	0	1	0	1.25000
0	0	1	1	1	0	1	1	1.24375
0	0	1	1	1	1	0	0	1.23750
0	0	1	1	1	1	0	1	1.23125
0	0	1	1	1	1	1	0	1.22500
0	0	1	1	1	1	1	1	1.21875
0	1	0	0	0	0	0	0	1.21250
0	1	0	0	0	0	0	1	1.20625
0	1	0	0	0	0	1	0	1.20000
0	1	0	0	0	0	1	1	1.19375
0	1	0	0	0	1	0	0	1.18750
0	1	0	0	0	1	0	1	1.18125
0	1	0	0	0	1	1	0	1.17500
0	1	0	0	0	1	1	1	1.16875
0	1	0	0	1	0	0	0	1.16250
0	1	0	0	1	0	0	1	1.15625
0	1	0	0	1	0	1	0	1.15000
0	1	0	0	1	0	1	1	1.14375
0	1	0	0	1	1	0	0	1.13750
0	1	0	0	1	1	0	1	1.13125
0	1	0	0	1	1	1	0	1.12500
0	1	0	0	1	1	1	1	1.11875
0	1	0	1	0	0	0	0	1.11250
0	1	0	1	0	0	0	1	1.10625
0	1	0	1	0	0	1	0	1.10000
0	1	0	1	0	0	1	1	1.09375
0	1	0	1	0	1	0	0	1.08750
0	1	0	1	0	1	0	1	1.08125
0	1	0	1	0	1	1	0	1.07500
0	1	0	1	0	1	1	1	1.06875
0	1	0	1	1	0	0	0	1.06250
0	1	0	1	1	0	0	1	1.05625
0	1	0	1	1	0	1	0	1.05000
0	1	0	1	1	0	1	1	1.04375
0	1	0	1	1	1	0	0	1.03750
0	1	0	1	1	1	0	1	1.03125
0	1	0	1	1	1	1	0	1.02500
0	1	0	1	1	1	1	1	1.01875

Figure 2-4. V_{CC} Overshoot Example Waveform

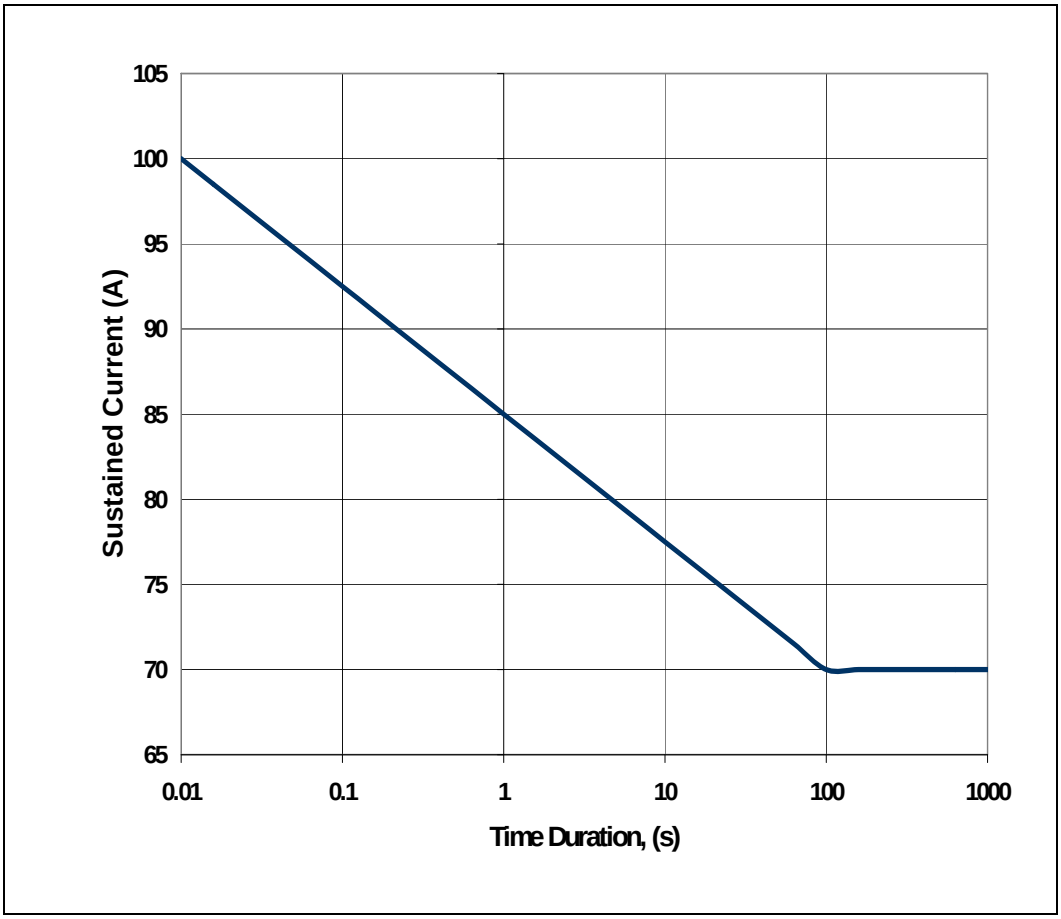


Notes:
1. V_{OS} is the measured overshoot voltage.
2. T_{OS} is the measured time duration above VID.

2.6.2 Die Voltage Validation

Core voltage (V_{CC}) overshoot events at the processor must meet the specifications in Table 2-10 when measured across the VCC_SENSE and VSS_SENSE lands. Overshoot events that are < 10 ns in duration may be ignored. These measurements of processor die level overshoot should be taken with a 100 MHz bandwidth limited oscilloscope.

Figure 2-7. Load Current Versus Time (Standard Server / Workstation)[1,2]



Notes:

1. Processor or voltage regulator thermal protection circuitry should not trip for load currents greater than I_{CC_TDC}.
2. Not 100% tested. Specified by design characterization.

Table 2-13. PECI Signal DC Electrical Limits (Sheet 2 of 2)

Symbol	Definition and Conditions	Min	Max	Units	Notes[1]
I_{Leak-}	High impedance leakage to GND (V_{leak} = V_{OH})	N/A	25	µA	3
C_{Bus}	Bus capacitance per node	N/A	10	pF	4,5
V_{Noise}	Signal noise immunity above 300 MHz	0.100 * V_{TTD}	N/A	V_{p-p}	

Note:
1. V_{TTD} supplies the PECI interface. PECI behavior does not affect V_{TTD} min/max specifications.
2. It is expected that the PECI driver will take into account, the variance in the receiver input thresholds and consequently, be able to drive its output within safe limits (-0.150 V to 0.275*V_{TTD} for the low level and 0.725*V_{TTD} to V_{TTD}+0.150 for the high level).
3. The leakage specification applies to powered devices on the PECI bus.
4. One node is counted for each client and one node for the system host. Extended trace lengths might appear as additional nodes.
5. Excessive capacitive loading on the PECI line may slow down the signal rise/fall times and consequently limit the maximum bit rate at which the interface can operate.
6. Please refer to Figure 2-2 for further information.

Table 2-14. System Reference Clock DC Specifications

Symbol	Parameter	Min	Max	Unit	Figure	Notes[1]
$V_{BCLK\_diff\_ih}$	Differential Input High Voltage	0.150	N/A	V		
$V_{BCLK\_diff\_il}$	Differential Input Low Voltage	N/A	-0.150	V		
V_{cross} (abs)	Absolute Crossing Point	0.250	0.550	V	2-16 2-19	2, 4
V_{cross}(rel)	Relative Crossing Point	0.250 + 0.5*(VH_{avg} - 0.700)	0.550 + 0.5*(VH_{avg} - 0.700)	V	2-16	3,4,5
ΔV_{cross}	Range of Crossing Points	N/A	0.140	V	2-20	6

Notes:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. Crossing Voltage is defined as the instantaneous voltage value when the rising edge of BCLK_DN is equal to the falling edge of BCLK_DP.
3. V_{Havg} is the statistical average of the VH measured by the oscilloscope.
4. The crossing point must meet the absolute and relative crossing point specifications simultaneously.
5. V_{Havg} can be measured directly using “Vtop” on Agilent* and “High” on Tektronix* oscilloscopes.
6. V_{CROSS} is defined as the total variation of all crossing voltages as defined in Note 2.

Table 2-15. RESET# Signal DC Specifications

Symbol	Parameter	Min	Typ	Max	Units	Notes[1]
V_{IL}	Input Low Voltage			0.6 * V_{TTA}	V	2
V_{IH}	Input High Voltage	0.7 * V_{TTA}			V	2,4
R_{ON}	Buffer On Resistance	10		18	Ω	
I_{LI}	Input Leakage Current			± 200	µA	3

Notes:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. The V_{TTA} referred to in these specifications refers to instantaneous V_{TTA}.
3. For V_{IN} between 0 V and V_{TTA}. Measured when the driver is tri-stated.
4. V_{IH} may experience excursions above V_{TT}. However, input signal drivers must comply with the signal quality specifications in Section 3.

Figure 2-20. Single-Ended Clock Measurement Points for Delta Cross Point

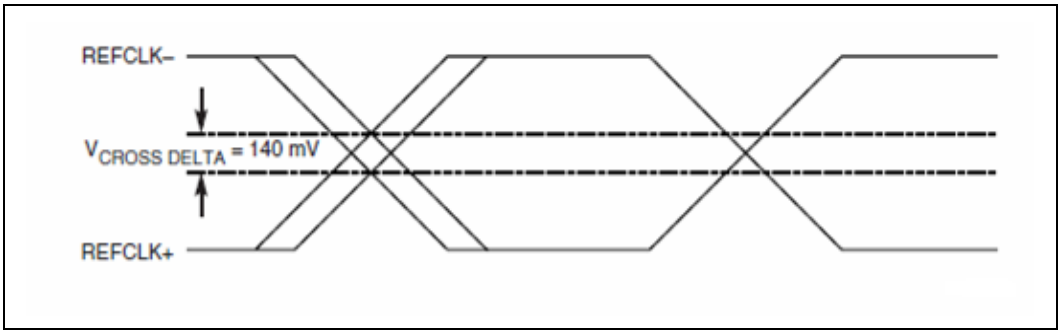


Figure 2-21. Differential Clock Measurement Point for Ringback

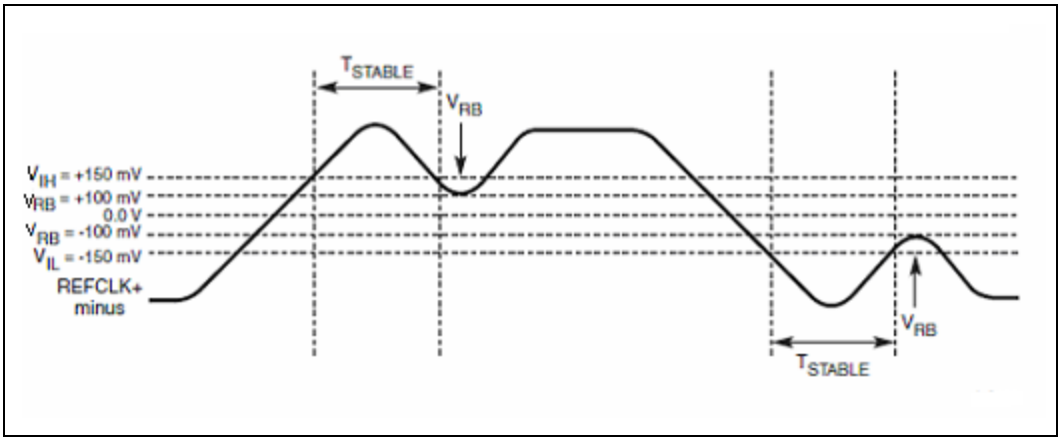
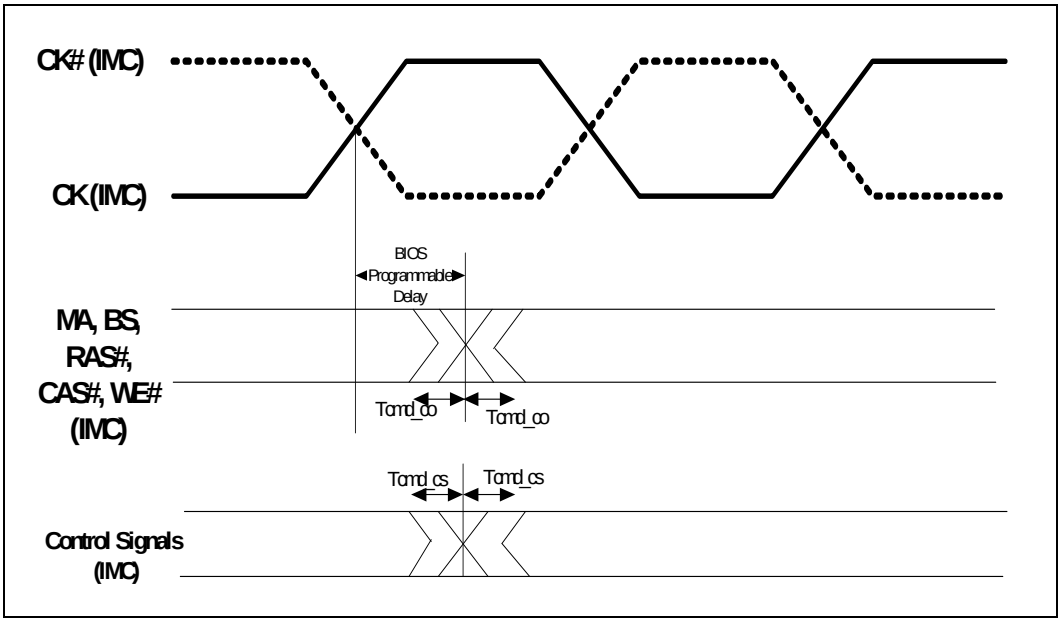


Figure 2-22. DDR3 Command / Control and Clock Timing Waveform



4.1.1 Package Mechanical Drawing

The package mechanical drawings are shown in Figure 4-2 and Figure 4-3. The drawings include dimensions necessary to design a thermal solution and reflect the processor as received by Intel. These dimensions include:

1. Package reference with tolerances (total height, length, width, and so forth)
2. IHS parallelism and tilt
3. Land dimensions
4. Top-side and back-side component keep-out dimensions
5. Reference datums
6. All drawing dimensions are in mm.
7. Guidelines on potential IHS flatness variation with socket load plate actuation and installation of the cooling solution is available in the *Intel® Xeon® Processor 5500/5600 Series Thermal/Mechanical Design Guidelines*.

Figure 4-3. Processor Package Drawing (Sheet 2 of 2)

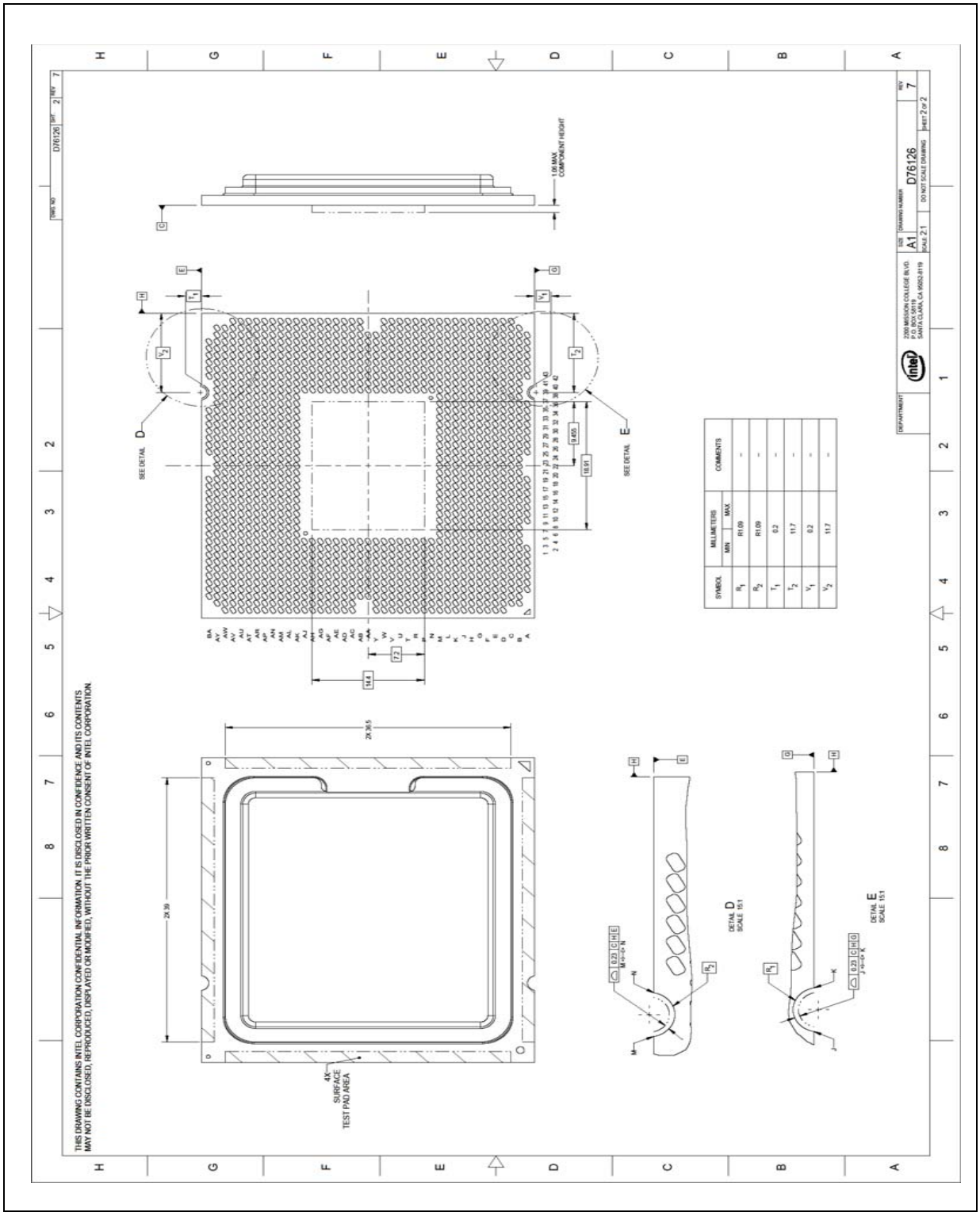


Table 5-1. By Land Name (Sheet 5 of 36)

Land Name	Land No.	Buffer Type	Direction
QPI1_DTX_DN[17]	AD7	QPI	O
QPI1_DTX_DN[18]	AE5	QPI	O
QPI1_DTX_DN[19]	AD8	QPI	O
QPI1_DTX_DN[2]	AJ6	QPI	O
QPI1_DTX_DN[3]	AK5	QPI	O
QPI1_DTX_DN[4]	AK4	QPI	O
QPI1_DTX_DN[5]	AG6	QPI	O
QPI1_DTX_DN[6]	AJ2	QPI	O
QPI1_DTX_DN[7]	AJ1	QPI	O
QPI1_DTX_DN[8]	AH4	QPI	O
QPI1_DTX_DN[9]	AG2	QPI	O
QPI1_DTX_DP[0]	AG8	QPI	O
QPI1_DTX_DP[1]	AJ8	QPI	O
QPI1_DTX_DP[10]	AF2	QPI	O
QPI1_DTX_DP[11]	AE1	QPI	O
QPI1_DTX_DP[12]	AD2	QPI	O
QPI1_DTX_DP[13]	AC3	QPI	O
QPI1_DTX_DP[14]	AE3	QPI	O
QPI1_DTX_DP[15]	AC4	QPI	O
QPI1_DTX_DP[16]	AB6	QPI	O
QPI1_DTX_DP[17]	AD6	QPI	O
QPI1_DTX_DP[18]	AD5	QPI	O
QPI1_DTX_DP[19]	AC8	QPI	O
QPI1_DTX_DP[2]	AH6	QPI	O
QPI1_DTX_DP[3]	AK6	QPI	O
QPI1_DTX_DP[4]	AJ4	QPI	O
QPI1_DTX_DP[5]	AG7	QPI	O
QPI1_DTX_DP[6]	AJ3	QPI	O
QPI1_DTX_DP[7]	AK1	QPI	O
QPI1_DTX_DP[8]	AH3	QPI	O
QPI1_DTX_DP[9]	AH2	QPI	O
DBR#	AF10	Asynch	I
DDR_COMP[0]	AA8	Analog	
DDR_COMP[1]	Y7	Analog	
DDR_COMP[2]	AC1	Analog	
DDR_THERM#	AB5	CMOS	I
DDR_THERM2#	AF4	CMOS	I
DDR_VREF	L23	Analog	I
DDR0_BA[0]	B16	CMOS	O
DDR0_BA[1]	A16	CMOS	O
DDR0_BA[2]	C28	CMOS	O

Table 5-1. By Land Name (Sheet 6 of 36)

Land Name	Land No.	Buffer Type	Direction
DDR0_CAS#	C12	CMOS	O
DDR0_CKE[0]	C29	CMOS	O
DDR0_CKE[1]	A30	CMOS	O
DDR0_CKE[2]	B30	CMOS	O
DDR0_CKE[3]	B31	CMOS	O
DDR0_CLK_N[0]	K19	CLOCK	O
DDR0_CLK_N[1]	C19	CLOCK	O
DDR0_CLK_N[2]	E18	CLOCK	O
DDR0_CLK_N[3]	E19	CLOCK	O
DDR0_CLK_P[0]	J19	CLOCK	O
DDR0_CLK_P[1]	D19	CLOCK	O
DDR0_CLK_P[2]	F18	CLOCK	O
DDR0_CLK_P[3]	E20	CLOCK	O
DDR0_CS#[0]	G15	CMOS	O
DDR0_CS#[1]	B10	CMOS	O
DDR0_CS#[2]	C13	CMOS	O
DDR0_CS#[3]	B9	CMOS	O
DDR0_CS#[4]	B15	CMOS	O
DDR0_CS#[5]	A7	CMOS	O
DDR0_CS#[6]/ DDR0_ODT[4]	C11	CMOS	O
DDR0_CS#[7]/ DDR0_ODT[5]	B8	CMOS	O
DDR0_DQ[0]	W41	CMOS	I/O
DDR0_DQ[1]	V41	CMOS	I/O
DDR0_DQ[10]	K42	CMOS	I/O
DDR0_DQ[11]	K43	CMOS	I/O
DDR0_DQ[12]	P42	CMOS	I/O
DDR0_DQ[13]	P41	CMOS	I/O
DDR0_DQ[14]	L43	CMOS	I/O
DDR0_DQ[15]	L42	CMOS	I/O
DDR0_DQ[16]	H41	CMOS	I/O
DDR0_DQ[17]	H43	CMOS	I/O
DDR0_DQ[18]	E42	CMOS	I/O
DDR0_DQ[19]	E43	CMOS	I/O
DDR0_DQ[2]	R43	CMOS	I/O
DDR0_DQ[20]	J42	CMOS	I/O
DDR0_DQ[21]	J41	CMOS	I/O
DDR0_DQ[22]	F43	CMOS	I/O
DDR0_DQ[23]	F42	CMOS	I/O
DDR0_DQ[24]	D40	CMOS	I/O
DDR0_DQ[25]	C41	CMOS	I/O

Table 5-1. By Land Name (Sheet 7 of 36)

Land Name	Land No.	Buffer Type	Direction
DDR0_DQ[26]	A38	CMOS	I/O
DDR0_DQ[27]	D37	CMOS	I/O
DDR0_DQ[28]	D41	CMOS	I/O
DDR0_DQ[29]	D42	CMOS	I/O
DDR0_DQ[3]	R42	CMOS	I/O
DDR0_DQ[30]	C38	CMOS	I/O
DDR0_DQ[31]	B38	CMOS	I/O
DDR0_DQ[32]	B5	CMOS	I/O
DDR0_DQ[33]	C4	CMOS	I/O
DDR0_DQ[34]	F1	CMOS	I/O
DDR0_DQ[35]	G3	CMOS	I/O
DDR0_DQ[36]	B6	CMOS	I/O
DDR0_DQ[37]	C6	CMOS	I/O
DDR0_DQ[38]	F3	CMOS	I/O
DDR0_DQ[39]	F2	CMOS	I/O
DDR0_DQ[4]	W40	CMOS	I/O
DDR0_DQ[40]	H2	CMOS	I/O
DDR0_DQ[41]	H1	CMOS	I/O
DDR0_DQ[42]	L1	CMOS	I/O
DDR0_DQ[43]	M1	CMOS	I/O
DDR0_DQ[44]	G1	CMOS	I/O
DDR0_DQ[45]	H3	CMOS	I/O
DDR0_DQ[46]	L3	CMOS	I/O
DDR0_DQ[47]	L2	CMOS	I/O
DDR0_DQ[48]	N1	CMOS	I/O
DDR0_DQ[49]	N2	CMOS	I/O
DDR0_DQ[5]	W42	CMOS	I/O
DDR0_DQ[50]	T1	CMOS	I/O
DDR0_DQ[51]	T2	CMOS	I/O
DDR0_DQ[52]	M3	CMOS	I/O
DDR0_DQ[53]	N3	CMOS	I/O
DDR0_DQ[54]	R4	CMOS	I/O
DDR0_DQ[55]	T3	CMOS	I/O
DDR0_DQ[56]	U4	CMOS	I/O
DDR0_DQ[57]	V1	CMOS	I/O
DDR0_DQ[58]	Y2	CMOS	I/O
DDR0_DQ[59]	Y3	CMOS	I/O
DDR0_DQ[6]	U41	CMOS	I/O
DDR0_DQ[60]	U1	CMOS	I/O
DDR0_DQ[61]	U3	CMOS	I/O
DDR0_DQ[62]	V4	CMOS	I/O

Table 5-1. By Land Name (Sheet 8 of 36)

Land Name	Land No.	Buffer Type	Direction
DDR0_DQ[63]	W4	CMOS	I/O
DDR0_DQ[7]	T42	CMOS	I/O
DDR0_DQ[8]	N41	CMOS	I/O
DDR0_DQ[9]	N43	CMOS	I/O
DDR0_DQS_N[0]	U43	CMOS	I/O
DDR0_DQS_N[1]	M41	CMOS	I/O
DDR0_DQS_N[10]	M43	CMOS	I/O
DDR0_DQS_N[11]	G43	CMOS	I/O
DDR0_DQS_N[12]	C39	CMOS	I/O
DDR0_DQS_N[13]	D4	CMOS	I/O
DDR0_DQS_N[14]	J1	CMOS	I/O
DDR0_DQS_N[15]	P1	CMOS	I/O
DDR0_DQS_N[16]	V3	CMOS	I/O
DDR0_DQS_N[17]	B35	CMOS	I/O
DDR0_DQS_N[2]	G41	CMOS	I/O
DDR0_DQS_N[3]	B40	CMOS	I/O
DDR0_DQS_N[4]	E4	CMOS	I/O
DDR0_DQS_N[5]	K3	CMOS	I/O
DDR0_DQS_N[6]	R3	CMOS	I/O
DDR0_DQS_N[7]	W1	CMOS	I/O
DDR0_DQS_N[8]	D35	CMOS	I/O
DDR0_DQS_N[9]	V42	CMOS	I/O
DDR0_DQS_P[0]	T43	CMOS	I/O
DDR0_DQS_P[1]	L41	CMOS	I/O
DDR0_DQS_P[10]	N42	CMOS	I/O
DDR0_DQS_P[11]	H42	CMOS	I/O
DDR0_DQS_P[12]	D39	CMOS	I/O
DDR0_DQS_P[13]	D5	CMOS	I/O
DDR0_DQS_P[14]	J2	CMOS	I/O
DDR0_DQS_P[15]	P2	CMOS	I/O
DDR0_DQS_P[16]	V2	CMOS	I/O
DDR0_DQS_P[17]	B36	CMOS	I/O
DDR0_DQS_P[2]	F41	CMOS	I/O
DDR0_DQS_P[3]	B39	CMOS	I/O
DDR0_DQS_P[4]	E3	CMOS	I/O
DDR0_DQS_P[5]	K2	CMOS	I/O
DDR0_DQS_P[6]	R2	CMOS	I/O
DDR0_DQS_P[7]	W2	CMOS	I/O
DDR0_DQS_P[8]	D34	CMOS	I/O
DDR0_DQS_P[9]	V43	CMOS	I/O
DDR0_ECC[0]	C36	CMOS	I/O

Table 5-1. By Land Name (Sheet 11 of 36)

Land Name	Land No.	Buffer Type	Direction
DDR1_DQ[3]	Y34	CMOS	I/O
DDR1_DQ[30]	L32	CMOS	I/O
DDR1_DQ[31]	K30	CMOS	I/O
DDR1_DQ[32]	E9	CMOS	I/O
DDR1_DQ[33]	E8	CMOS	I/O
DDR1_DQ[34]	E5	CMOS	I/O
DDR1_DQ[35]	F5	CMOS	I/O
DDR1_DQ[36]	F10	CMOS	I/O
DDR1_DQ[37]	G8	CMOS	I/O
DDR1_DQ[38]	D6	CMOS	I/O
DDR1_DQ[39]	F6	CMOS	I/O
DDR1_DQ[4]	AA35	CMOS	I/O
DDR1_DQ[40]	H8	CMOS	I/O
DDR1_DQ[41]	J6	CMOS	I/O
DDR1_DQ[42]	G4	CMOS	I/O
DDR1_DQ[43]	H4	CMOS	I/O
DDR1_DQ[44]	G9	CMOS	I/O
DDR1_DQ[45]	H9	CMOS	I/O
DDR1_DQ[46]	G5	CMOS	I/O
DDR1_DQ[47]	J5	CMOS	I/O
DDR1_DQ[48]	K4	CMOS	I/O
DDR1_DQ[49]	K5	CMOS	I/O
DDR1_DQ[5]	AB36	CMOS	I/O
DDR1_DQ[50]	R5	CMOS	I/O
DDR1_DQ[51]	T5	CMOS	I/O
DDR1_DQ[52]	J4	CMOS	I/O
DDR1_DQ[53]	M6	CMOS	I/O
DDR1_DQ[54]	R8	CMOS	I/O
DDR1_DQ[55]	R7	CMOS	I/O
DDR1_DQ[56]	W6	CMOS	I/O
DDR1_DQ[57]	W7	CMOS	I/O
DDR1_DQ[58]	Y10	CMOS	I/O
DDR1_DQ[59]	W10	CMOS	I/O
DDR1_DQ[6]	Y40	CMOS	I/O
DDR1_DQ[60]	V9	CMOS	I/O
DDR1_DQ[61]	W5	CMOS	I/O
DDR1_DQ[62]	AA7	CMOS	I/O
DDR1_DQ[63]	W9	CMOS	I/O
DDR1_DQ[7]	Y39	CMOS	I/O
DDR1_DQ[8]	P34	CMOS	I/O
DDR1_DQ[9]	P35	CMOS	I/O

Table 5-1. By Land Name (Sheet 12 of 36)

Land Name	Land No.	Buffer Type	Direction
DDR1_DQS_N[0]	Y37	CMOS	I/O
DDR1_DQS_N[1]	R37	CMOS	I/O
DDR1_DQS_N[10]	P37	CMOS	I/O
DDR1_DQS_N[11]	K37	CMOS	I/O
DDR1_DQS_N[12]	K33	CMOS	I/O
DDR1_DQS_N[13]	F7	CMOS	I/O
DDR1_DQS_N[14]	J7	CMOS	I/O
DDR1_DQS_N[15]	M4	CMOS	I/O
DDR1_DQS_N[16]	Y5	CMOS	I/O
DDR1_DQS_N[17]	E35	CMOS	I/O
DDR1_DQS_N[2]	L36	CMOS	I/O
DDR1_DQS_N[3]	L31	CMOS	I/O
DDR1_DQS_N[4]	D7	CMOS	I/O
DDR1_DQS_N[5]	G6	CMOS	I/O
DDR1_DQS_N[6]	L5	CMOS	I/O
DDR1_DQS_N[7]	Y9	CMOS	I/O
DDR1_DQS_N[8]	G34	CMOS	I/O
DDR1_DQS_N[9]	AA41	CMOS	I/O
DDR1_DQS_P[0]	Y38	CMOS	I/O
DDR1_DQS_P[1]	R38	CMOS	I/O
DDR1_DQS_P[10]	P36	CMOS	I/O
DDR1_DQS_P[11]	L37	CMOS	I/O
DDR1_DQS_P[12]	K34	CMOS	I/O
DDR1_DQS_P[13]	F8	CMOS	I/O
DDR1_DQS_P[14]	H7	CMOS	I/O
DDR1_DQS_P[15]	M5	CMOS	I/O
DDR1_DQS_P[16]	Y4	CMOS	I/O
DDR1_DQS_P[17]	F35	CMOS	I/O
DDR1_DQS_P[2]	L35	CMOS	I/O
DDR1_DQS_P[3]	L30	CMOS	I/O
DDR1_DQS_P[4]	E7	CMOS	I/O
DDR1_DQS_P[5]	H6	CMOS	I/O
DDR1_DQS_P[6]	L6	CMOS	I/O
DDR1_DQS_P[7]	Y8	CMOS	I/O
DDR1_DQS_P[8]	G33	CMOS	I/O
DDR1_DQS_P[9]	AA40	CMOS	I/O
DDR1_ECC[0]	D36	CMOS	I/O
DDR1_ECC[1]	F36	CMOS	I/O
DDR1_ECC[2]	E33	CMOS	I/O
DDR1_ECC[3]	G36	CMOS	I/O
DDR1_ECC[4]	E37	CMOS	I/O

Table 5-1. By Land Name (Sheet 15 of 36)

Land Name	Land No.	Buffer Type	Direction
DDR2_DQ[33]	J12	CMOS	I/O
DDR2_DQ[34]	H13	CMOS	I/O
DDR2_DQ[35]	L13	CMOS	I/O
DDR2_DQ[36]	G11	CMOS	I/O
DDR2_DQ[37]	G10	CMOS	I/O
DDR2_DQ[38]	H12	CMOS	I/O
DDR2_DQ[39]	L12	CMOS	I/O
DDR2_DQ[4]	U34	CMOS	I/O
DDR2_DQ[40]	L10	CMOS	I/O
DDR2_DQ[41]	K10	CMOS	I/O
DDR2_DQ[42]	M9	CMOS	I/O
DDR2_DQ[43]	N9	CMOS	I/O
DDR2_DQ[44]	L11	CMOS	I/O
DDR2_DQ[45]	M10	CMOS	I/O
DDR2_DQ[46]	L8	CMOS	I/O
DDR2_DQ[47]	M8	CMOS	I/O
DDR2_DQ[48]	P7	CMOS	I/O
DDR2_DQ[49]	N6	CMOS	I/O
DDR2_DQ[5]	V34	CMOS	I/O
DDR2_DQ[50]	P9	CMOS	I/O
DDR2_DQ[51]	P10	CMOS	I/O
DDR2_DQ[52]	N8	CMOS	I/O
DDR2_DQ[53]	N7	CMOS	I/O
DDR2_DQ[54]	R10	CMOS	I/O
DDR2_DQ[55]	R9	CMOS	I/O
DDR2_DQ[56]	U5	CMOS	I/O
DDR2_DQ[57]	U6	CMOS	I/O
DDR2_DQ[58]	T10	CMOS	I/O
DDR2_DQ[59]	U10	CMOS	I/O
DDR2_DQ[6]	V37	CMOS	I/O
DDR2_DQ[60]	T6	CMOS	I/O
DDR2_DQ[61]	T7	CMOS	I/O
DDR2_DQ[62]	V8	CMOS	I/O
DDR2_DQ[63]	U9	CMOS	I/O
DDR2_DQ[7]	V38	CMOS	I/O
DDR2_DQ[8]	U38	CMOS	I/O
DDR2_DQ[9]	U39	CMOS	I/O
DDR2_DQS_N[0]	W36	CMOS	I/O
DDR2_DQS_N[1]	T38	CMOS	I/O
DDR2_DQS_N[10]	T40	CMOS	I/O
DDR2_DQS_N[11]	L38	CMOS	I/O

Table 5-1. By Land Name (Sheet 16 of 36)

Land Name	Land No.	Buffer Type	Direction
DDR2_DQS_N[12]	G38	CMOS	I/O
DDR2_DQS_N[13]	J11	CMOS	I/O
DDR2_DQS_N[14]	K8	CMOS	I/O
DDR2_DQS_N[15]	P4	CMOS	I/O
DDR2_DQS_N[16]	V7	CMOS	I/O
DDR2_DQS_N[17]	G31	CMOS	I/O
DDR2_DQS_N[2]	K39	CMOS	I/O
DDR2_DQS_N[3]	E40	CMOS	I/O
DDR2_DQS_N[4]	J9	CMOS	I/O
DDR2_DQS_N[5]	K7	CMOS	I/O
DDR2_DQS_N[6]	P5	CMOS	I/O
DDR2_DQS_N[7]	T8	CMOS	I/O
DDR2_DQS_N[8]	G30	CMOS	I/O
DDR2_DQS_N[9]	T35	CMOS	I/O
DDR2_DQS_P[0]	W37	CMOS	I/O
DDR2_DQS_P[1]	T37	CMOS	I/O
DDR2_DQS_P[10]	U40	CMOS	I/O
DDR2_DQS_P[11]	M38	CMOS	I/O
DDR2_DQS_P[12]	H38	CMOS	I/O
DDR2_DQS_P[13]	H11	CMOS	I/O
DDR2_DQS_P[14]	K9	CMOS	I/O
DDR2_DQS_P[15]	N4	CMOS	I/O
DDR2_DQS_P[16]	V6	CMOS	I/O
DDR2_DQS_P[17]	H31	CMOS	I/O
DDR2_DQS_P[2]	K40	CMOS	I/O
DDR2_DQS_P[3]	E39	CMOS	I/O
DDR2_DQS_P[4]	J10	CMOS	I/O
DDR2_DQS_P[5]	L7	CMOS	I/O
DDR2_DQS_P[6]	P6	CMOS	I/O
DDR2_DQS_P[7]	U8	CMOS	I/O
DDR2_DQS_P[8]	G29	CMOS	I/O
DDR2_DQS_P[9]	U35	CMOS	I/O
DDR2_ECC[0]	H32	CMOS	I/O
DDR2_ECC[1]	F33	CMOS	I/O
DDR2_ECC[2]	E29	CMOS	I/O
DDR2_ECC[3]	E30	CMOS	I/O
DDR2_ECC[4]	J31	CMOS	I/O
DDR2_ECC[5]	J30	CMOS	I/O
DDR2_ECC[6]	F31	CMOS	I/O
DDR2_ECC[7]	F30	CMOS	I/O
DDR2_MA[0]	A18	CMOS	O

Table 5-2. By Land Number (Sheet 5 of 35)

Land Name	Land No.	Buffer Type	Direction
VTTA	AF33	PWR	
VTTA	AF34	PWR	
VSS	AF35	GND	
VTTD	AF36	PWR	
VTTD	AF37		
VSS	AF38	GND	
QPI0_DTX_DP[1]	AF39	QPI	O
DDR_THERM2#	AF4		
QPI0_DTX_DN[19]	AF40	QPI	O
VSS	AF41	GND	
QPI0_CLKTX_DN	AF42	QPI	O
QPI0_DTX_DP[10]	AF43	QPI	O
VSS	AF5	GND	
QPI1_CLKTX_DP	AF6	QPI	O
VTT_VID3	AF7	CMOS	O
VTTD	AF8	PWR	
VTTD	AF9	PWR	
RSVD	AG1		
TMS	AG10	TAP	I
VSS	AG11	GND	
QPI1_DTX_DN[9]	AG2	QPI	O
VSS	AG3	GND	
VSS	AG33	GND	
VTTA	AG34	PWR	
PROCHOT#	AG35	GTL	I/O
SKTOCC#	AG36		O
THERMTRIP#	AG37	GTL	O
QPI0_DTX_DP[0]	AG38	QPI	O
QPI0_DTX_DN[1]	AG39	QPI	O
RSVD	AG4		
QPI0_DTX_DP[9]	AG40	QPI	O
QPI0_DTX_DN[9]	AG41	QPI	O
QPI0_CLKTX_DP	AG42	QPI	O
VSS	AG43	GND	
RSVD	AG5		
QPI1_DTX_DN[5]	AG6	QPI	O
QPI1_DTX_DP[5]	AG7	QPI	O
QPI1_DTX_DP[0]	AG8	QPI	O
VSS	AG9	GND	
VSS	AH1	GND	
TCK	AH10	TAP	I

Table 5-2. By Land Number (Sheet 6 of 35)

Land Name	Land No.	Buffer Type	Direction
VCC	AH11	PWR	
QPI1_DTX_DP[9]	AH2	QPI	O
QPI1_DTX_DP[8]	AH3	QPI	O
VCC	AH33	PWR	
VSS	AH34	GND	
BCLK_DN	AH35	CMOS	I
PECI	AH36	Asynch	I/O
VSS	AH37	GND	
QPI0_DTX_DN[0]	AH38	QPI	O
VSS	AH39	GND	
QPI1_DTX_DN[8]	AH4	QPI	O
QPI0_DTX_DP[4]	AH40	QPI	O
QPI0_DTX_DP[6]	AH41	QPI	O
QPI0_DTX_DN[6]	AH42	QPI	O
QPI0_DTX_DN[8]	AH43	QPI	O
TAPPWRGOOD	AH5		
QPI1_DTX_DP[2]	AH6	QPI	O
VSS	AH7	GND	
QPI1_DTX_DN[0]	AH8	QPI	O
TRST#	AH9	TAP	I
QPI1_DTX_DN[7]	AJ1	QPI	O
TDO	AJ10	TAP	O
VCC	AJ11	PWR	
QPI1_DTX_DN[6]	AJ2	QPI	O
QPI1_DTX_DP[6]	AJ3	QPI	O
VCC	AJ33	PWR	
VSS	AJ34	GND	
BCLK_DP	AJ35	CMOS	I
VSS	AJ36	GND	
GTLREF	AJ37	Analog	I
QPI0_DTX_DP[3]	AJ38	QPI	O
QPI0_DTX_DN[3]	AJ39	QPI	O
QPI1_DTX_DP[4]	AJ4	QPI	O
QPI0_DTX_DN[4]	AJ40	QPI	O
VSS	AJ41	GND	
QPI0_DTX_DN[7]	AJ42	QPI	O
QPI0_DTX_DP[8]	AJ43	QPI	O
VSS	AJ5	GND	
QPI1_DTX_DN[2]	AJ6	QPI	O
QPI1_DTX_DN[1]	AJ7	QPI	O
QPI1_DTX_DP[1]	AJ8	QPI	O

Table 5-2. By Land Number (Sheet 7 of 35)

Land Name	Land No.	Buffer Type	Direction
TDI	AJ9	TAP	I
QPI1_DTX_DP[7]	AK1	QPI	O
VSS	AK10	GND	
VCC	AK11	PWR	
VCC	AK12	PWR	
VCC	AK13	PWR	
VSS	AK14	GND	
VCC	AK15	PWR	
VCC	AK16	PWR	
VSS	AK17	GND	
VCC	AK18	PWR	
VCC	AK19	PWR	
RSVD	AK2		
VSS	AK20	GND	
VCC	AK21	PWR	
VSS	AK22	GND	
VSS	AK23	GND	
VCC	AK24	PWR	
VCC	AK25	PWR	
VSS	AK26	GND	
VCC	AK27	PWR	
VCC	AK28	PWR	
VSS	AK29	GND	
VSS	AK3	GND	
VCC	AK30	PWR	
VCC	AK31	PWR	
VSS	AK32	GND	
VCC	AK33	PWR	
VSS	AK34	GND	
PECI_ID#	AK35	Asynch	I
RSVD	AK36		
QPI0_DTX_DP[2]	AK37	QPI	O
QPI0_DTX_DN[2]	AK38	QPI	O
VSS	AK39	GND	
QPI1_DTX_DN[4]	AK4	QPI	O
QPI0_DTX_DP[5]	AK40	QPI	O
QPI0_DTX_DN[5]	AK41	QPI	O
QPI0_DTX_DP[7]	AK42	QPI	O
VSS	AK43	GND	
QPI1_DTX_DN[3]	AK5	QPI	O
QPI1_DTX_DP[3]	AK6	QPI	O

Table 5-2. By Land Number (Sheet 8 of 35)

Land Name	Land No.	Buffer Type	Direction
RSVD	AK7		
ISENSE	AK8	Analog	I
VSS	AK9	GND	
VSS	AL1	GND	
VID[0]/MSID[0]	AL10	CMOS	O
VSS	AL11	GND	
VCC	AL12	PWR	
VCC	AL13	PWR	
VSS	AL14	GND	
VCC	AL15	PWR	
VCC	AL16	PWR	
VSS	AL17	GND	
VCC	AL18	PWR	
VCC	AL19	PWR	
VSS	AL2	GND	
VSS	AL20	GND	
VCC	AL21	PWR	
VSS	AL22	GND	
VSS	AL23	GND	
VCC	AL24	PWR	
VCC	AL25	PWR	
VSS	AL26	GND	
VCC	AL27	PWR	
VCC	AL28	PWR	
VSS	AL29	GND	
RSVD	AL3		
VCC	AL30	PWR	
VCC	AL31	PWR	
VSS	AL32	GND	
VCC	AL33	PWR	
VCC	AL34	PWR	
VSS	AL35	GND	
VSS	AL36	GND	
VSS	AL37	GND	
RSVD	AL38		
RESET#	AL39	Asynch	I
RSVD	AL4		
RSVD	AL40		
RSVD	AL41		
VSS	AL42	GND	
QPI0_COMP	AL43	Analog	

Table 5-2. By Land Number (Sheet 21 of

Land Name	Land No.	Buffer Type	Direction
DDR0_DQ[30]	C38	CMOS	I/O
DDR0_DQS_N[12]	C39	CMOS	I/O
DDR0_DQ[33]	C4	CMOS	I/O
VSS	C40	GND	
DDR0_DQ[25]	C41	CMOS	I/O
PREQ#	C42	GTL	I
VSS	C43	GND	
VSS	C5	GND	
DDR0_DQ[37]	C6	CMOS	I/O
DDR0_ODT[3]	C7	CMOS	O
DDR1_ODT[1]	C8	CMOS	O
DDR0_ODT[1]	C9	CMOS	O
BPM#[4]	D1	GTL	I/O
DDR2_ODT[3]	D10	CMOS	O
DDR1_ODT[0]	D11	CMOS	O
DDR1_CS#[0]	D12	CMOS	O
VDDQ	D13	PWR	
DDR1_ODT[2]	D14	CMOS	O
DDR2_ODT[2]	D15	CMOS	O
DDR2_CS#[2]	D16	CMOS	O
DDR2_RAS#	D17	CMOS	O
VDDQ	D18	PWR	
DDR0_CLK_P[1]	D19	CLOCK	O
BPM#[6]	D2	GTL	I/O
DDR1_MA_PAR	D20	CMOS	O
DDR1_CLK_N[0]	D21	CLOCK	O
DDR1_MA[7]	D22	CMOS	O
VDDQ	D23	PWR	
DDR0_MA[3]	D24	CMOS	O
DDR0_PAR_ERR#[0]	D25	Asynch	I
DDR2_CKE[2]	D26	CMOS	O
DDR1_CKE[2]	D27	CMOS	O
VDDQ	D28	PWR	
DDR1_RESET#	D29	CMOS	O
VSS	D3	GND	
RSVD	D30		
RSVD	D31		
DDR0_RESET#	D32	CMOS	O
VSS	D33	GND	
DDR0_DQS_P[8]	D34	CMOS	I/O
DDR0_DQS_N[8]	D35	CMOS	I/O

Table 5-2. By Land Number (Sheet 22 of

Land Name	Land No.	Buffer Type	Direction
DDR1_ECC[0]	D36	CMOS	I/O
DDR0_DQ[27]	D37	CMOS	I/O
VSS	D38	GND	
DDR0_DQS_P[12]	D39	CMOS	I/O
DDR0_DQS_N[13]	D4	CMOS	I/O
DDR0_DQ[24]	D40	CMOS	I/O
DDR0_DQ[28]	D41	CMOS	I/O
DDR0_DQ[29]	D42	CMOS	I/O
VSS	D43	GND	
DDR0_DQS_P[13]	D5	CMOS	I/O
DDR1_DQ[38]	D6	CMOS	I/O
DDR1_DQS_N[4]	D7	CMOS	I/O
VSS	D8	GND	
DDR2_CS#[5]	D9	CMOS	O
VSS	E1	GND	
DDR1_CS#[5]	E10	CMOS	O
VDDQ	E11	PWR	
DDR1_CS#[7]/ DDR1_ODT[5]	E12	CMOS	O
DDR1_CS#[3]	E13	CMOS	O
DDR1_CAS#	E14	CMOS	O
DDR1_CS#[2]	E15	CMOS	O
VDDQ	E16	PWR	
DDR2_CS#[4]	E17	CMOS	O
DDR0_CLK_N[2]	E18	CLOCK	O
DDR0_CLK_N[3]	E19	CLOCK	O
BPM#[7]	E2	GTL	I/O
DDR0_CLK_P[3]	E20	CLOCK	O
VDDQ	E21	PWR	
DDR1_MA[8]	E22	CMOS	O
DDR1_MA[11]	E23	CMOS	O
DDR1_MA[12]	E24	CMOS	O
DDR1_PAR_ERR#[1]	E25	Asynch	I
VDDQ	E26	PWR	
DDR1_CKE[1]	E27	CMOS	O
RSVD	E28		
DDR2_ECC[2]	E29	CMOS	I/O
DDR0_DQS_P[4]	E3	CMOS	I/O
DDR2_ECC[3]	E30	CMOS	I/O
VDDQ	E31	PWR	
DDR2_RESET#	E32	CMOS	O
DDR1_ECC[2]	E33	CMOS	I/O

Table 6-1. Signal Definitions (Sheet 4 of 4)

Name	Type	Description	Notes
VCCPWRGOOD	I	VCCPWRGOOD (Power Good) is a processor input. The processor requires this signal to be a clean indication that BCLK, V_{CC}, V_{CCPLL}, V_{TTA} and V_{TTD} supplies are stable and within their specifications. 'Clean' implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state. VCCPWRGOOD can be driven inactive at any time, but BCLK and power must again be stable before a subsequent rising edge of VCCPWRGOOD. In addition at the time VCCPWRGOOD is asserted RESET# must be active. The VCCPWRGOOD signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout boundary scan operation.	
V_{CCPLL}	I	Analog Power for Clocks.	
V_{DDQ}	I	Power supply for the DDR3 interface.	
VTT_VID[4:2]	O	VTT_VID[4:2] is used to support automatic selection of power supply voltages (V_{TT}). The voltage supply for this signal must be valid before the VR can supply V_{TT} to the processor. Conversely, the VR output must be disabled until the voltage supply for the VID signal become valid. The VID signal is needed to support the processor voltage specification variations. The VR must supply the voltage that is requested by the signal.	
V_{TTA}	I	Power for the analog portion of the Intel QuickPath and Shared Cache.	
V_{TTD}	I	Power for the digital portion of the Intel QuickPath and Shared Cache.	
VDDPWRGOOD	I	VDDPWRGOOD is an input that indicates the VDDQ power supply is good. The processor requires this signal to be a clean indication that the Vddq power supply is stable and within their specifications. "Clean" implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the VDDQ supply is turned on until it comes within specification. The signals must then transition monotonically to a high state. The VDDPWRGOOD signal must be supplied to the processor. This signal is used to protect internal circuits against voltage sequencing issues.	
VID[7:0]	I/O	VID[7:0] (Voltage ID) are output signals that are used to support automatic selection of power supply voltages (V_{CC}). The voltage supply for these signals must be valid before the VR can supply V_{CC} to the processor. Conversely, the VR output must be disabled until the voltage supply for the VID signals become valid. The VID signals are needed to support the processor voltage specification variations. The VR must supply the voltage that is requested by the signals, or disable itself. MSID[2:0] - Market Segment ID, or MSID are provided to indicate the Market Segment for the processor and may be used for future processor compatibility or for keying. In addition, MSID protects the platform by preventing a higher power processor from booting in a platform designed for lower power processors. This value is latched from the platform in to the CPU, on the rising edge of VTTPWRGOOD, during the cold boot power up sequence. CSC[2:0] - Current Sense Configuration bits are output signals for ISENSE gain setting.This value is latched on the rising edge of VTTPWRGOOD.	2
V_{TTD_SENSE} $V_{SS\_SENSE\_VTT}$	O O	V_{TTD_SENSE} and $V_{SS\_SENSE\_VTT}$ provide an isolated, low impedance connection to the processor core power and ground. They can used to sense or measure power near the silicon.	
VTTPWRGOOD	I	The processor requires this input signal to be a clean indication that the VTT power supply is stable and within their specifications. 'Clean' implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state. to determine that the VTT voltage is stable and within specification. Note it is not valid for VTTPWRGOOD to be deasserted while VCCPWRGOOD is asserted.	

Notes:

1. DDR{0/1/2} refers to DDR3 Channel 0, DDR3 Channel 1, and DDR3 Channel 2.
2. VID[7:0] is an Input only during Power On Configuration. It is an Output signal during normal operation.

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3. Refer to the *Intel® Xeon® Processor 5500/5600 Series Thermal/Mechanical Design Guidelines* for system and environmental implementation details.

Table 7-15. Low Power Platform 40W Thermal Profile (4 Core)

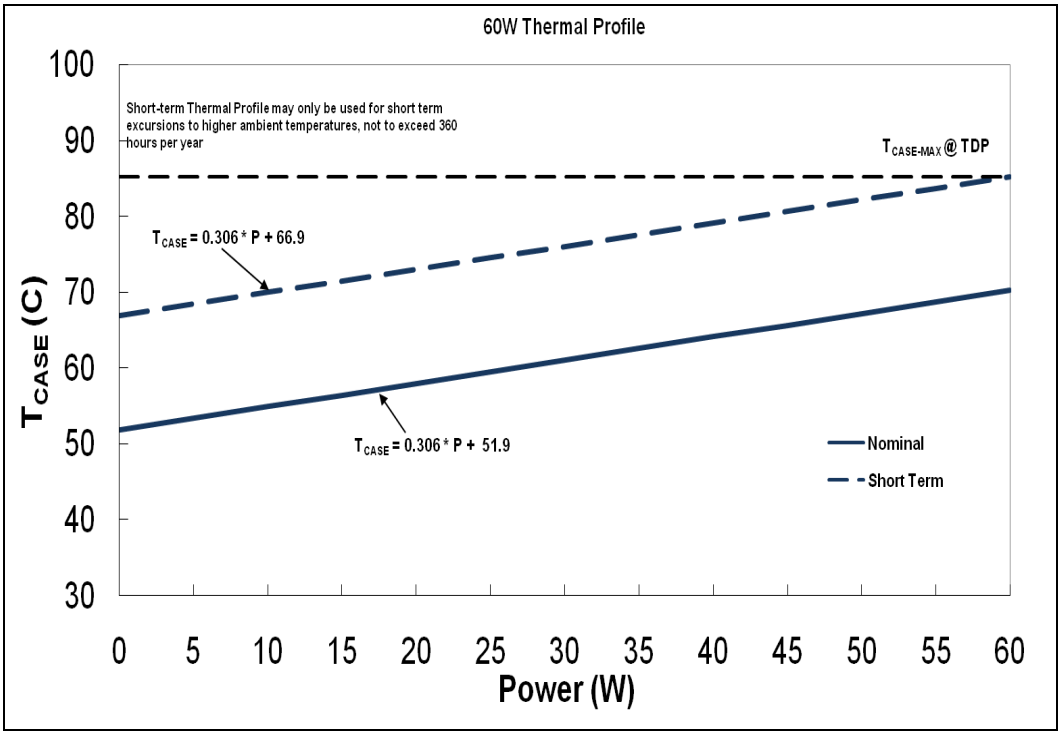
Power (W)	Maximum T_{CASE} (°C)
0	50.4
10	53.6
20	56.8
30	59.9
40	63.1

Table 7-16. LV-60W Processor Thermal Specifications

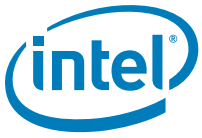
Core Frequency	Thermal Design Power (W)	Minimum TCASE (°C)	Maximum TCASE (°C)	Notes
Launch to FMB	60	5	See Figure 7-9; Table 7-17	1, 2, 3, 4

Notes:
1. These values are specified at V_{CC_MAX} for all processor frequencies. Systems must be designed to ensure the processor is not to be subjected to any static V_{CC} and I_{CC} combination wherein V_{CC} exceeds V_{CC_MAX} at specified I_{CC}. Please refer to the loadline specifications in Section 2.
2. Thermal Design Power (TDP) should be used for processor thermal solution design targets. TDP is not the maximum power that the processor can dissipate. TDP is measured at maximum T_{CASE}.
3. Power specifications are defined at all VIDs found in Table 2-2. The processor may be shipped under multiple VIDs for each frequency.
4. FMB, or Flexible Motherboard, guidelines provide a design target for meeting all planned processor frequency requirements.

Figure 7-9. LV-60W Processor Dual Thermal Profile



Notes:
1. The Thermal Profile is representative of a volumetrically constrained platform. Please refer to Table 7-17 for discrete points that constitute the thermal profile.



will accept lower bit rates from a host according to timing negotiation specifications. What follows is a processor-specific PECI client definition. PECI commands listed in Table 7-20 apply to Intel Xeon processor 5600 series only.

Table 7-20. Summary of Processor-Specific PECI Commands

Command	Intel® Xeon® Processor 5600 Series Support
Ping()	Yes
GetDIB()	Yes
GetTemp()	Yes
PCIConfigRd()	Yes
PCIConfigWr()	Yes
MbxSend() [1]	Yes
MbxGet() [1]	Yes

Note:
1. Refer to Table 7-25 for a summary of mailbox commands supported by the Intel Xeon processor 5600 series.

7.3.1 PECI Client Capabilities

Intel Xeon processor 5600 series acting as PECI clients support the following sideband functions:

- Processor and DRAM thermal management
- Platform manageability functions including thermal, power and electrical error monitoring
- Processor interface tuning and diagnostics capabilities (Intel® IBIST).

7.3.1.1 Thermal Management

Processor fan speed control is managed by comparing PECI thermal readings against the processor-specific fan speed control reference point, or $T_{CONTROL}$. Both $T_{CONTROL}$ and PECI thermal readings are accessible via the processor PECI client. These variables are referenced to a common temperature, the TCC activation point, and are both defined as negative offsets from that reference.

PECI-based access to DRAM thermal readings and throttling control coefficients provide a means for Board Management Controllers (BMCs) or other platform management devices to feed hints into on-die memory controller throttling algorithms. These control coefficients are accessible using PCI configuration space writes via PECI. The PECI-based configuration write functionality is defined in Section 7.3.2.5, and the DRAM throttling coefficient control functions are documented in the *Intel® Xeon® Processor 5600 Series Datasheet, Volume 2*.

7.3.1.2 Platform Manageability

PECI allows full read access to error and status monitoring registers within the processor's PCI configuration space. It also provides insight into thermal monitoring functions such as TCC activation timers and thermal error logs.

The exact list of RAS-related registers in the PCI configuration space can be found in the *Intel® Xeon® Processor 5600 Series Datasheet, Volume 2*.

- Assured Write FCS (AW FCS) failure. Note that under most circumstances, an Assured Write failure will appear as a bad FCS. However, when an originator issues a poorly formatted command with a miscalculated AW FCS, the client will intentionally abort the FCS in order to guarantee originator notification.

7.3.4.2 Completion Codes

Some PECI commands respond with a completion code byte. These codes are designed to communicate the pass/fail status of the command and also provide more detailed information regarding the class of pass or fail. For all commands listed in Section 7.3.2 that support completion codes, each command's completion codes is listed in its respective section. What follows are some generalizations regarding completion codes.

An originator that is decoding these commands can apply a simple mask to determine pass or fail. Bit 7 is always set on a failed command, and is cleared on a passing command.

Table 7-33. Completion Code Pass/Fail Mask

0xxx xxxxb	Command passed
1xxx xxxxb	Command failed

Table 7-34. Device Specific Completion Code (CC) Definition

Completion Code	Description
0x00..0x3F	Device specific pass code
0x40	Command Passed
0x4X	Command passed with a transaction ID of 'X' (0x40 | Transaction_ID[3:0])
0x50..0x7F	Device specific pass code
0x80	Error causing a response timeout. Either due to a rare, internal timing condition or a processor RESET condition or processor S1 state. Retry is appropriate outside of the RESET or S1 states.
0x81	Thermal configuration data was malformed or exceeded limits.
0x82	Thermal status mask is illegal
0x83	Invalid counter select
0x84	Invalid Machine Check Bank or Index
0x85	Failure due to lack of Mailbox lock or invalid Transaction ID
0x86	Mailbox interface is unavailable or busy
0x88	Machine Check Banks is currently unavailable (selected core is asleep or unavailable)
0x89	Invalid Core Select for Machine Check Bank Read
0xFF	Unknown/Invalid Request

Note: The codes explicitly defined in this table may be useful in PECI originator response algorithms. All reserved or undefined codes may be generated by a PECI client device, and the originating agent must be capable of tolerating any code. The Pass/Fail mask defined in Table 7-33 applies to all codes and general response policies may be based on that limited information.