# Microchip Technology - DSPIC33FJ16GP101-I/SS Datasheet

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

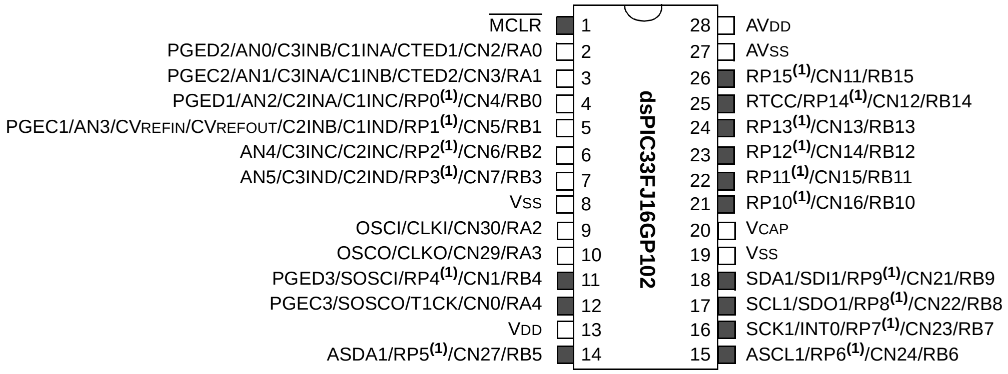
## Applications of "Embedded - Microcontrollers"

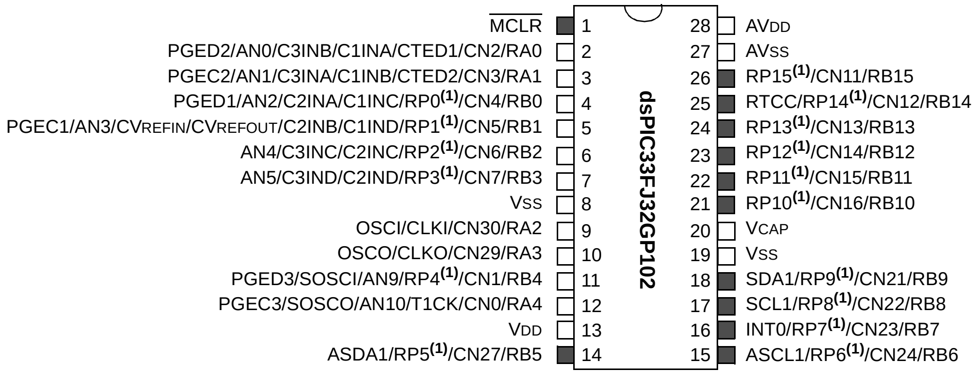
| **Details** | |
|---|---|
| Product Status | Active |
| Core Processor | dsPIC |
| Core Size | 16-Bit |
| Speed | 16 MIPs |
| Connectivity | I²C, IrDA, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 13 |
| Program Memory Size | 16KB (16K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 1K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 3.6V |
| Data Converters | A/D 4x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 20-SSOP (0.209", 5.30mm Width) |
| Supplier Device Package | 20-SSOP |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj16gp101-i-ss |

## Pin Diagrams (Continued)

**28-Pin SPDIP/SOIC/SSOP**

■ = Pins are up to 5V tolerant



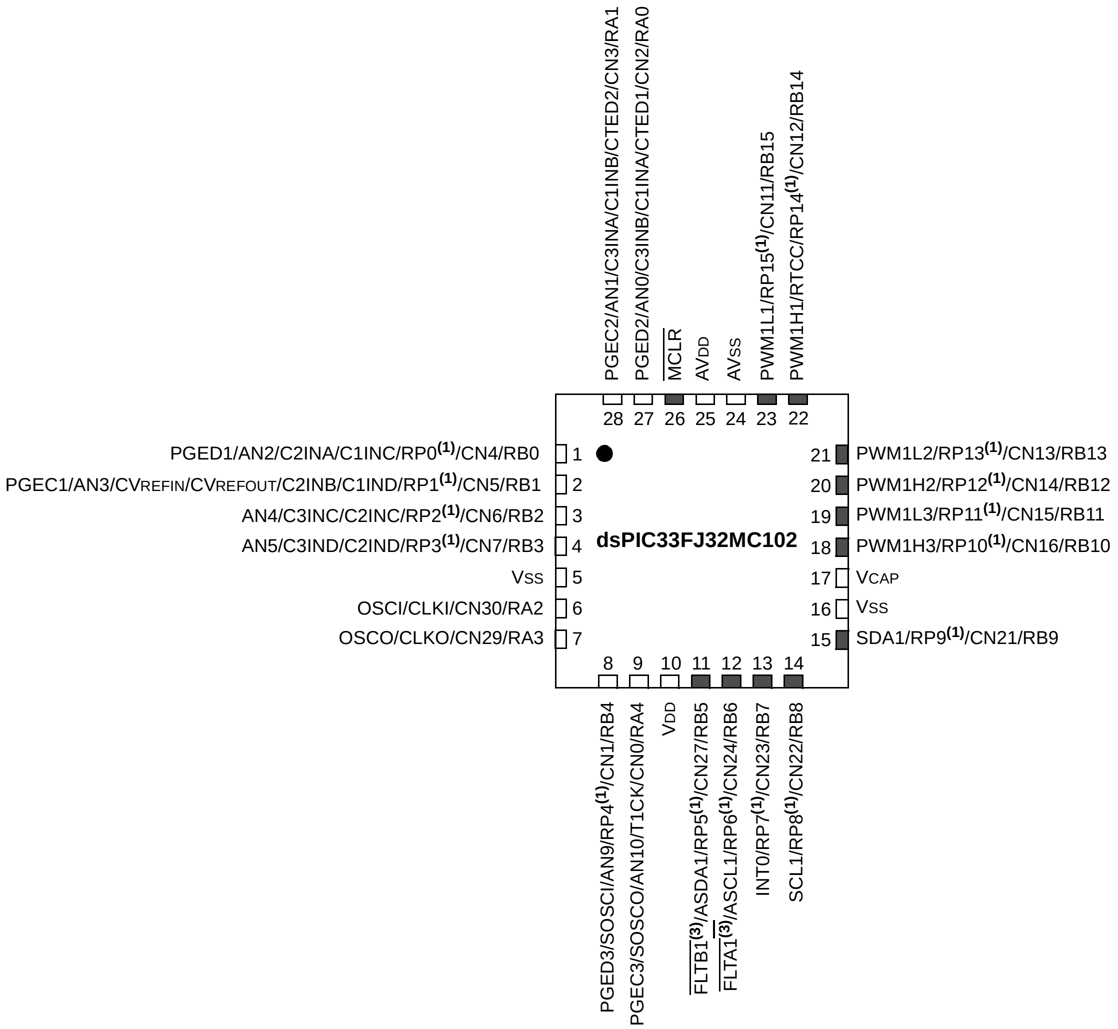


**Note 1:** The RPn pins can be used by any remappable peripheral. See Table 1 for the list of available peripherals.

## Pin Diagrams (Continued)

**28-Pin QFN$^{(2)}$**

■ = Pins are up to 5V tolerant

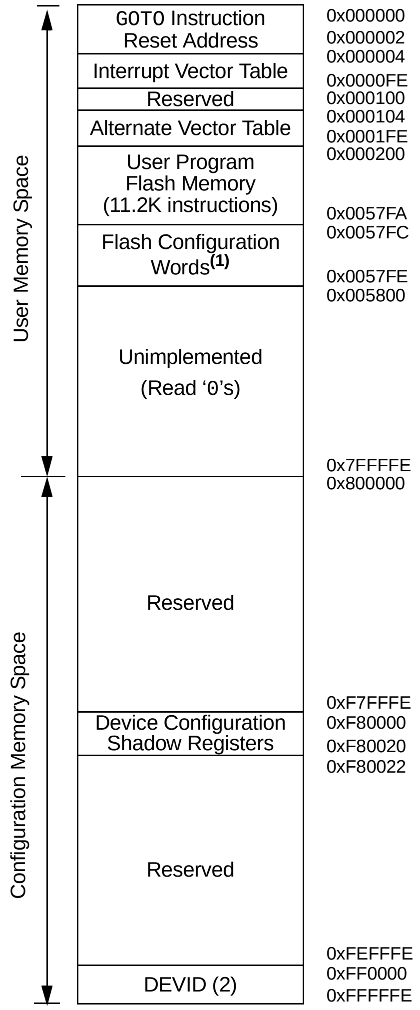


**Note 1:** The RPn pins can be used by any remappable peripheral. See Table 1 for the list of available peripherals.

**2:** The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

**3:** The PWM Fault pins are enabled and asserted during any Reset event. Refer to **Section 15.2 "PWM Faults"** for more information on the PWM Faults.

**FIGURE 4-2: PROGRAM MEMORY MAP FOR dsPIC33FJ32(GP/MC)101/102/104 DEVICES**



**Note 1:** On Reset, these bits are automatically copied into the device Configuration Shadow registers.

### 4.1.1 PROGRAM MEMORY ORGANIZATION

The program memory space is organized in word-addressable blocks. Although it is treated as 24 bits wide, it is more appropriate to think of each address of the program memory as a lower and upper word, with the upper byte of the upper word being unimplemented. The lower word always has an even address, while the upper word has an odd address (Figure 4-3).

Program memory addresses are always word-aligned on the lower word and addresses are incremented or decremented by two during code execution. This arrangement provides compatibility with data memory space addressing and makes data in the program memory space accessible.

### 4.1.2 INTERRUPT AND TRAP VECTORS

All of the dsPIC33FJ16(GP/MC)101/102 and dsPIC33FJ32(GP/MC)101/102/104 devices reserve the addresses between 0x00000 and 0x000200 for hard-coded program execution vectors. A hardware Reset vector is provided to redirect code execution from the default value of the PC on device Reset to the actual start of code. A `GOTO` instruction is programmed by the user application at 0x000000, with the actual address for the start of code at 0x000002.

dsPIC33FJ16(GP/MC)101/102 and dsPIC33FJ32(GP/MC)101/102/104 devices also have two Interrupt Vector Tables (IVTs), located from 0x000004 to 0x0000FF and 0x000100 to 0x0001FF. These vector tables allow each of the device interrupt sources to be handled by separate Interrupt Service Routines (ISRs). A more detailed discussion of the Interrupt Vector Tables is provided in **Section 7.1 “Interrupt Vector Table”**.

**FIGURE 4-3: PROGRAM MEMORY ORGANIZATION**

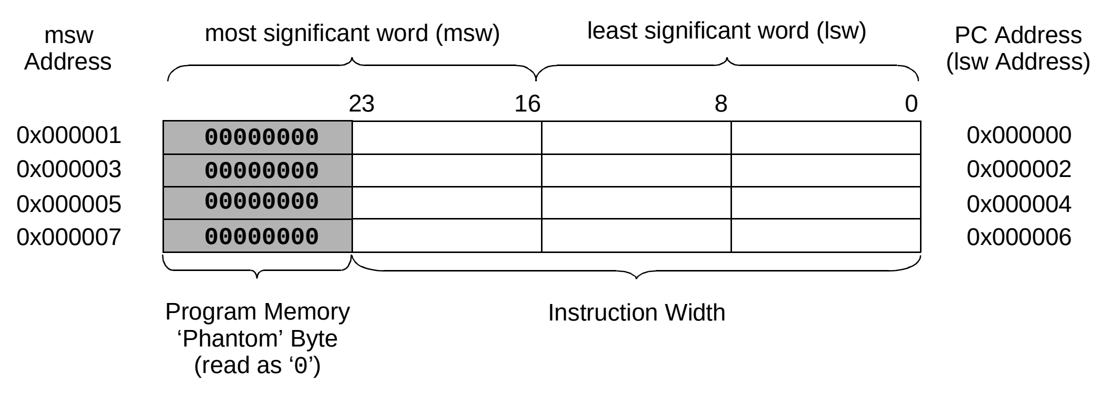
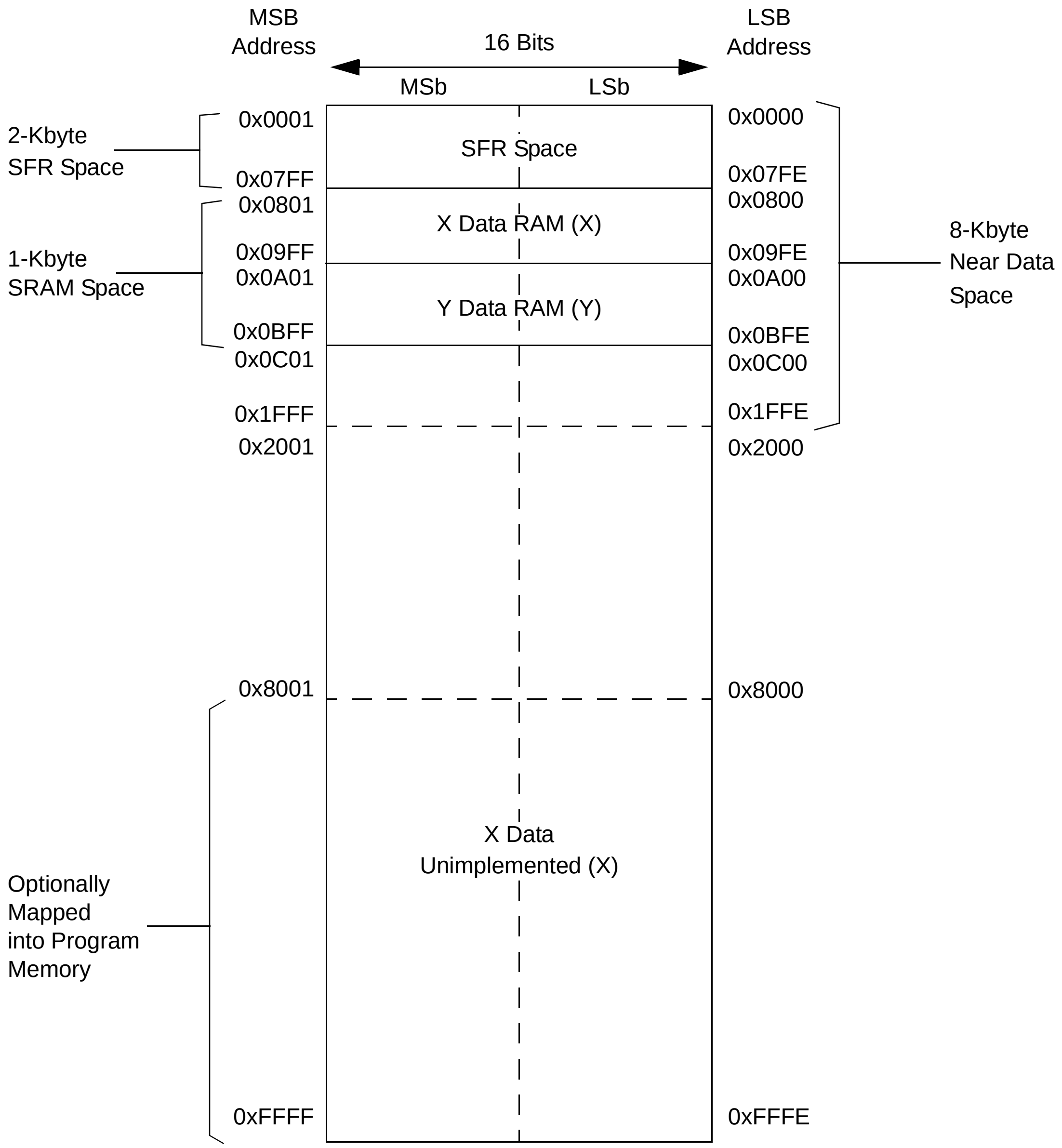


**FIGURE 4-4: DATA MEMORY MAP FOR dsPIC33FJ16(GP/MC)101/102 DEVICES WITH 1-KBYTE RAM**



## TABLE 4-16: ADC1 REGISTER MAP FOR dsPIC33FJXX(GP/MC)102 DEVICES

| File Name | SFR Addr | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ADC1BUF0 | 0300 | ADC1 Data Buffer 0 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUF1 | 0302 | ADC1 Data Buffer 1 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUF2 | 0304 | ADC1 Data Buffer 2 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUF3 | 0306 | ADC1 Data Buffer 3 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUF4 | 0308 | ADC1 Data Buffer 4 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUF5 | 030A | ADC1 Data Buffer 5 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUF6 | 030C | ADC1 Data Buffer 6 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUF7 | 030E | ADC1 Data Buffer 7 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUF8 | 0310 | ADC1 Data Buffer 8 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUF9 | 0312 | ADC1 Data Buffer 9 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUFA | 0314 | ADC1 Data Buffer 10 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUFB | 0316 | ADC1 Data Buffer 11 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUFC | 0318 | ADC1 Data Buffer 12 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUFD | 031A | ADC1 Data Buffer 13 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUFE | 031C | ADC1 Data Buffer 14 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUFF | 031E | ADC1 Data Buffer 15 | | | | | | | | | | | | | | | | xxxx |
| AD1CON1 | 0320 | ADON | — | ADSIDL | — | — | — | FORM1 | FORM0 | SSRC2 | SSRC1 | SSRC0 | — | SIMSAM | ASAM | SAMP | DONE | 0000 |
| AD1CON2 | 0322 | VCFG2 | VCFG1 | VCFG0 | — | — | CSCNA | CHPS1 | CHPS0 | BUFS | — | SMPI3 | SMPI2 | SMPI1 | SMPI0 | BUFM | ALTS | 0000 |
| AD1CON3 | 0324 | ADRC | — | — | SAMC4 | SAMC3 | SAMC2 | SAMC1 | SAMC0 | ADCS7 | ADCS6 | ADCS5 | ADCS4 | ADCS3 | ADCS2 | ADCS1 | ADCS0 | 0000 |
| AD1CHS123 | 0326 | — | — | — | — | — | CH123NB1 | CH123NB0 | CH123SB | — | — | — | — | — | CH123NA1 | CH123NA0 | CH123SA | 0000 |
| AD1CHS0 | 0328 | CH0NB | — | — | CH0SB4 | CH0SB3 | CH0SB2 | CH0SB1 | CH0SB0 | CH0NA | — | — | CH0SA4 | CH0SA3 | CH0SA2 | CH0SA1 | CH0SA0 | 0000 |
| AD1PCFGL | 032C | — | — | — | — | — | PCFG<10:9>(1) | | — | — | — | PCFG<5:0> | | | | | | 0000 |
| AD1CSSL | 0330 | — | — | — | — | — | CSS<10:9>(1) | | — | — | — | CSS<5:0> | | | | | | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as ‘0’. Reset values are shown in hexadecimal.

**Note 1:** The PCFG<10:9> and CSS<10:9> bits are available in dsPIC33FJ32(GP/MC)101/102 devices only.

## 4.6 Interfacing Program and Data Memory Spaces

The dsPIC33FJ16(GP/MC)101/102 and dsPIC33FJ32(GP/MC)101/102/104 architecture uses a 24-bit-wide program space and a 16-bit-wide data space. The architecture is also a modified Harvard scheme, meaning that data can also be present in the program space. To use this data successfully, it must be accessed in a way that preserves the alignment of information in both spaces.

Aside from normal execution, the dsPIC33FJ16(GP/MC)101/102 and dsPIC33FJ32(GP/MC)101/102/104 architecture provides two methods by which program space can be accessed during operation:

- Using table instructions to access individual bytes, or words, anywhere in the program space
- Remapping a portion of the program space into the data space (Program Space Visibility)

Table instructions allow an application to read or write to small areas of the program memory. This capability makes the method ideal for accessing data tables that need to be updated periodically. It also allows access to all bytes of the program word. The remapping method allows an application to access a large block of data on a read-only basis, which is ideal for lookups from a large table of static data. The application can only access the lsw of the program word.

### 4.6.1 ADDRESSING PROGRAM SPACE

Since the address ranges for the data and program spaces are 16 and 24 bits, respectively, a method is needed to create a 23-bit or 24-bit program address from 16-bit data registers. The solution depends on the interface method to be used.

For table operations, the 8-bit Table Page (TBLPAG) register is used to define a 32K word region within the program space. This is concatenated with a 16-bit EA to arrive at a full 24-bit program space address. In this format, the MSb of TBLPAG is used to determine if the operation occurs in the user memory (TBLPAG<7> = `0`) or the configuration memory (TBLPAG<7> = `1`).

For remapping operations, the 8-bit Program Space Visibility (PSVPAG) register is used to define a 16K word page in the program space. When the MSb of the EA is ‘`1`’, PSVPAG is concatenated with the lower 15 bits of the EA to form a 23-bit program space address. Unlike table operations, this limits remapping operations strictly to the user memory area.

Table 4-42 and Figure 4-9 show how the program EA is created for table operations and remapping accesses from the data EA.

**TABLE 4-42: PROGRAM SPACE ADDRESS CONSTRUCTION**

| Access Type | Access Space | Program Space Address | | | | |
|---|---|---|---|---|---|---|
| | | <23> | <22:16> | <15> | <14:1> | <0> |
| Instruction Access<br>(Code Execution) | User | `0` | PC<22:1> | | | `0` |
| | | `0xx xxxx xxxx xxxx xxxx xxx0` | | | | |
| `TBLRD/TBLWT`<br>(Byte/Word Read/Write) | User | TBLPAG<7:0> | | Data EA<15:0> | | |
| | | `0xxx xxxx` | | `xxxx xxxx xxxx xxxx` | | |
| | Configuration | TBLPAG<7:0> | | Data EA<15:0> | | |
| | | `1xxx xxxx` | | `xxxx xxxx xxxx xxxx` | | |
| Program Space Visibility<br>(Block Remap/Read) | User | `0` | PSVPAG<7:0> | | Data EA<14:0>(1) | |
| | | `0` | `xxxx xxxx` | | `xxx xxxx xxxx xxxx` | |

**Note 1:** Data EA<15> is always ‘`1`’ in this case, but is not used in calculating the program space address. Bit 15 of the address is PSVPAG<0>.

### 6.10.2 UNINITIALIZED W REGISTER RESET

Any attempts to use the Uninitialized W register as an Address Pointer will reset the device. The W register array (with the exception of W15) is cleared during all Resets and is considered uninitialized until written to.

### 6.10.3 SECURITY RESET

If a Program Flow Change (PFC) or Vector Flow Change (VFC) targets a restricted location in a protected segment (Boot and Secure Segment), that operation will cause a Security Reset.

The PFC occurs when the Program Counter is reloaded as a result of a Call, Jump, Computed Jump, Return, Return from Subroutine or other form of branch instruction.

The VFC occurs when the Program Counter is reloaded with an interrupt or trap vector.

## 6.11 Using the RCON Status Bits

The user application can read the Reset Control (RCON) register after any device Reset to determine the cause of the Reset.

**Note:** The status bits in the RCON register should be cleared after they are read so that the next RCON register value after a device Reset will be meaningful.

Table 6-3 provides a summary of Reset flag bit operation.

**TABLE 6-3: RESET FLAG BIT OPERATION**

| Flag Bit | Set by: | Cleared by: |
|---|---|---|
| TRAPR (RCON<15>) | Trap conflict event | POR, BOR |
| IOPWR (RCON<14>) | Illegal opcode or uninitialized W register access or Security Reset | POR, BOR |
| CM (RCON<9>) | Configuration Mismatch | POR, BOR |
| EXTR (RCON<7>) | $\overline{\text{MCLR}}$ Reset | POR |
| SWR (RCON<6>) | `RESET` instruction | POR, BOR |
| WDTO (RCON<4>) | WDT Time-out | `PWRSAV` instruction,<br>`CLRWDT` instruction, POR, BOR |
| SLEEP (RCON<3>) | `PWRSAV #SLEEP` instruction | POR, BOR |
| IDLE (RCON<2>) | `PWRSAV #IDLE` instruction | POR, BOR |
| BOR (RCON<1>) | POR, BOR | — |
| POR (RCON<0>) | POR | — |

**Note:** All Reset flag bits can be set or cleared by user software.

### REGISTER 7-5: IFS0: INTERRUPT FLAG STATUS REGISTER 0 (CONTINUED)

| | |
|---|---|
| bit 2 | **OC1IF:** Output Compare Channel 1 Interrupt Flag Status bit<br>`1` = Interrupt request has occurred<br>`0` = Interrupt request has not occurred |
| bit 1 | **IC1IF:** Input Capture Channel 1 Interrupt Flag Status bit<br>`1` = Interrupt request has occurred<br>`0` = Interrupt request has not occurred |
| bit 0 | **INT0IF:** External Interrupt 0 Flag Status bit<br>`1` = Interrupt request has occurred<br>`0` = Interrupt request has not occurred |

### REGISTER 7-19: IPC4: INTERRUPT PRIORITY CONTROL REGISTER 4

| U-0 | R/W-1 | R/W-0 | R/W-0 | U-0 | R/W-1 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | CNIP2 | CNIP1 | CNIP0 | — | CMIP2 | CMIP1 | CMIP0 |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-1 | R/W-0 | R/W-0 | U-0 | R/W-1 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | MI2C1IP2 | MI2C1IP1 | MI2C1IP0 | — | SI2C1IP2 | SI2C1IP1 | SI2C1IP0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

| | |
|---|---|
| bit 15 | **Unimplemented:** Read as ‘`0`’ |
| bit 14-12 | **CNIP<2:0>:** Change Notification Interrupt Priority bits<br>`111` = Interrupt is Priority 7 (highest priority interrupt)<br>•<br>•<br>•<br>`001` = Interrupt is Priority 1<br>`000` = Interrupt source is disabled |
| bit 11 | **Unimplemented:** Read as ‘`0`’ |
| bit 10-8 | **CMIP<2:0>:** Comparator Interrupt Priority bits<br>`111` = Interrupt is Priority 7 (highest priority interrupt)<br>•<br>•<br>•<br>`001` = Interrupt is Priority 1<br>`000` = Interrupt source is disabled |
| bit 7 | **Unimplemented:** Read as ‘`0`’ |
| bit 6-4 | **MI2C1IP<2:0>:** I2C1 Master Events Interrupt Priority bits<br>`111` = Interrupt is Priority 7 (highest priority interrupt)<br>•<br>•<br>•<br>`001` = Interrupt is Priority 1<br>`000` = Interrupt source is disabled |
| bit 3 | **Unimplemented:** Read as ‘`0`’ |
| bit 2-0 | **SI2C1IP<2:0>:** I2C1 Slave Events Interrupt Priority bits<br>`111` = Interrupt is Priority 7 (highest priority interrupt)<br>•<br>•<br>•<br>`001` = Interrupt is Priority 1<br>`000` = Interrupt source is disabled |

# 9.0 POWER-SAVING FEATURES

**Note 1:** This data sheet summarizes the features of the dsPIC33FJ16(GP/MC)101/102 and dsPIC33FJ32(GP/MC)101/102/104 family devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Watchdog Timer and Power-Saving Modes"** (DS70196) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33FJ16(GP/MC)101/102 and dsPIC33FJ32(GP/MC)101/102/104 devices provide the ability to manage power consumption by selectively managing clocking to the CPU and the peripherals. In general, a lower clock frequency and a reduction in the number of circuits being clocked constitutes lower consumed power. Devices can manage power consumption in four different ways:

- Clock Frequency
- Instruction-Based Sleep and Idle modes
- Software-Controlled Doze mode
- Selective Peripheral Control in Software

Combinations of these methods can be used to selectively tailor an application's power consumption while still maintaining critical application features, such as timing-sensitive communications.

## 9.1 Clock Frequency and Clock Switching

dsPIC33FJ16(GP/MC)101/102 and dsPIC33FJ32(GP/MC)101/102/104 devices allow a wide range of clock frequencies to be selected under application control. If the system clock configuration is not locked, users can choose low-power or high-precision oscillators by simply changing the NOSC<2:0> bits (OSCCON<10:8>). The process of changing a system clock during operation, as well as limitations to the process, are discussed in more detail in **Section 8.0 "Oscillator Configuration"**.

## 9.2 Instruction-Based Power-Saving Modes

dsPIC33FJ16(GP/MC)101/102 and dsPIC33FJ32(GP/MC)101/102/104 devices have two special power-saving modes that are entered through the execution of a special `PWRSAV` instruction. Sleep mode stops clock operation and halts all code execution. Idle mode halts the CPU and code execution, but allows peripheral modules to continue operation. The assembler syntax of the `PWRSAV` instruction is shown in Example 9-1.

**Note:** `SLEEP_MODE` and `IDLE_MODE` are constants defined in the assembler include file for the selected device.

Sleep and Idle modes can be exited as a result of an enabled interrupt, WDT time-out or a device Reset. When the device exits these modes, it is said to wake-up.

### 9.2.1 SLEEP MODE

The following occurs in Sleep mode:

- The system clock source is shut down. If an on-chip oscillator is used, it is turned off.
- The device current consumption is reduced to a minimum, provided that no I/O pin is sourcing current
- The Fail-Safe Clock Monitor does not operate, since the system clock source is disabled
- The LPRC clock continues to run in Sleep mode if the WDT is enabled
- The WDT, if enabled, is automatically cleared prior to entering Sleep mode
- Some device features or peripherals may continue to operate. This includes items such as the Input Change Notification (ICN) on the I/O ports or peripherals that use an external clock input.
- Any peripheral that requires the system clock source for its operation is disabled

The device will wake-up from Sleep mode on any of the these events:

- Any interrupt source that is individually enabled
- Any form of device Reset
- A WDT time-out

On wake-up from Sleep mode, the processor restarts with the same clock source that was active when Sleep mode was entered.

**EXAMPLE 9-1: `PWRSAV` INSTRUCTION SYNTAX**

```
PWRSAV  #SLEEP_MODE    ; Put the device into SLEEP mode
PWRSAV  #IDLE_MODE     ; Put the device into IDLE mode
```

### REGISTER 10-7: RPINR11: PERIPHERAL PIN SELECT INPUT REGISTER 11

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
|---|---|---|---|---|---|---|---|
| — | — | — | OCFAR4 | OCFAR3 | OCFAR2 | OCFAR1 | OCFAR0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-5 **Unimplemented:** Read as ‘`0`’

bit 4-0 **OCFAR<4:0>:** Assign Output Capture A (OCFA) to the Corresponding RPn Pin bits

`11111` = Input tied to Vss
`11110` = Reserved
.
.
.
`11010` = Reserved
`11001` = Input tied to RP25
.
.
.
`00001` = Input tied to RP1
`00000` = Input tied to RP0

## 11.1 Timer1 Control Register

### REGISTER 11-1: T1CON: TIMER1 CONTROL REGISTER

| R/W-0 | U-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| TON[1] | — | TSIDL | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | TGATE | TCKPS1 | TCKPS0 | — | TSYNC | TCS[1] | — |
| bit 7 | | | | | | | bit 0 |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15 **TON:** Timer1 On bit[1]
1 = Starts 16-bit Timer1
0 = Stops 16-bit Timer1

bit 14 **Unimplemented:** Read as ‘0’

bit 13 **TSIDL:** Timer1 Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12-7 **Unimplemented:** Read as ‘0’

bit 6 **TGATE:** Timer1 Gated Time Accumulation Enable bit
When TCS = 1:
This bit is ignored.
When TCS = 0:
1 = Gated time accumulation is enabled
0 = Gated time accumulation is disabled

bit 5-4 **TCKPS<1:0>** Timer1 Input Clock Prescale Select bits
11 = 1:256
10 = 1:64
01 = 1:8
00 = 1:1

bit 3 **Unimplemented:** Read as ‘0’

bit 2 **TSYNC:** Timer1 External Clock Input Synchronization Select bit
When TCS = 1:
1 = Synchronizes external clock input
0 = Does not synchronize external clock input
When TCS = 0:
This bit is ignored.

bit 1 **TCS:** Timer1 Clock Source Select bit[1]
1 = External clock from pin, T1CK (on the rising edge)
0 = Internal clock (FCY)

bit 0 **Unimplemented:** Read as ‘0’

**Note 1:** When TCS = 1 and TON = 1, writes to the TMR1 register are inhibited from the CPU.

### REGISTER 20-2: CMxCON: COMPARATOR x CONTROL REGISTER

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
| CON | COE | CPOL | — | — | — | CEVT | COUT |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| R/W-0 | R/W-0 | U-0 | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 |
| EVPOL1 | EVPOL0 | — | CREF | — | — | CCH1 | CCH0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

| | |
|---|---|
| bit 15 | **CON:** Comparator x Enable bit<br>1 = Comparator x is enabled<br>0 = Comparator x is disabled |
| bit 14 | **COE:** Comparator x Output Enable bit<br>1 = Comparator output is present on the CxOUT pin<br>0 = Comparator output is internal only |
| bit 13 | **CPOL:** Comparator x Output Polarity Select bit<br>1 = Comparator x output is inverted<br>0 = Comparator x output is not inverted |
| bit 12-10 | **Unimplemented:** Read as ‘0’ |
| bit 9 | **CEVT:** Comparator x Event bit<br>1 = Comparator x event according to EVPOL<1:0> settings occurred; disables future triggers and interrupts until the bit is cleared<br>0 = Comparator x event did not occur |
| bit 8 | **COUT:** Comparator x Output bit<br>When CPOL = 0 (non-inverted polarity):<br>1 = VIN+ > VIN-<br>0 = VIN+ < VIN-<br>When CPOL = 1 (inverted polarity):<br>1 = VIN+ < VIN-<br>0 = VIN+ > VIN- |
| bit 7-6 | **EVPOL<1:0>:** Trigger/Event/Interrupt Polarity Select bits<br>11 = Trigger/event/interrupt is generated on any change of the comparator output (while CEVT = 0)<br>10 = Trigger/event/interrupt is generated only on high-to-low transition of the polarity selected comparator output (while CEVT = 0)<br>If CPOL = 1 (inverted polarity):<br>Low-to-high transition of the comparator output.<br>If CPOL = 0 (non-inverted polarity):<br>High-to-low transition of the comparator output.<br>01 = Trigger/event/interrupt is generated only on low-to-high transition of the polarity selected comparator output (while CEVT = 0)<br>If CPOL = 1 (inverted polarity):<br>High-to-low transition of the comparator output.<br>If CPOL = 0 (non-inverted polarity):<br>Low-to-high transition of the comparator output.<br>00 = Trigger/event/interrupt generation is disabled |
| bit 5 | **Unimplemented:** Read as ‘0’ |

**TABLE 26-7: DC CHARACTERISTICS: IDLE CURRENT ($I_{IDLE}$)**

| DC CHARACTERISTICS | | | | **Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)**<br>Operating temperature -40°C ≤ $T_A$ ≤ +85°C for Industrial<br>-40°C ≤ $T_A$ ≤ +125°C for Extended | | |
|---|---|---|---|---|---|---|
| **Parameter No.** | **Typical[1]** | **Max** | **Units** | **Conditions** | | |
| **Idle Current ($I_{IDLE}$): Core Off, Clock On Base Current[2] – dsPIC33FJ16(GP/MC)10X Devices** | | | | | | |
| DC40d | 0.4 | 1.0 | mA | -40°C | 3.3V | LPRC (32.768 kHz)[3] |
| DC40a | 0.4 | 1.0 | mA | +25°C | | |
| DC40b | 0.4 | 1.0 | mA | +85°C | | |
| DC40c | 0.5 | 1.0 | mA | +125°C | | |
| DC41d | 0.5 | 1.1 | mA | -40°C | 3.3V | 1 MIPS[3] |
| DC41a | 0.5 | 1.1 | mA | +25°C | | |
| DC41b | 0.5 | 1.1 | mA | +85°C | | |
| DC41c | 0.8 | 1.1 | mA | +125°C | | |
| DC42d | 0.9 | 1.6 | mA | -40°C | 3.3V | 4 MIPS[3] |
| DC42a | 0.9 | 1.6 | mA | +25°C | | |
| DC42b | 1.0 | 1.6 | mA | +85°C | | |
| DC42c | 1.2 | 1.6 | mA | +125°C | | |
| DC43a | 1.6 | 2.6 | mA | +25°C | 3.3V | 10 MIPS[3] |
| DC43d | 1.6 | 2.6 | mA | -40°C | | |
| DC43b | 1.7 | 2.6 | mA | +85°C | | |
| DC43c | 2 | 2.6 | mA | +125°C | | |
| DC44d | 2.4 | 3.8 | mA | -40°C | 3.3V | 16 MIPS[3] |
| DC44a | 2.4 | 3.8 | mA | +25°C | | |
| DC44b | 2.6 | 3.8 | mA | +85°C | | |
| DC44c | 2.9 | 3.8 | mA | +125°C | | |

**Note 1:** Data in “Typical” column is at 3.3V, +25°C unless otherwise stated.

**2:** Base Idle current is measured as follows:

- CPU core is off, oscillator is configured in EC mode, OSC1 is driven with external square wave from rail-to-rail
- CLKO is configured as an I/O input pin in the Configuration Word
- External Secondary Oscillator (SOSC) is disabled (i.e., SOSCO and SOSCI pins are configured as digital I/O inputs)
- All I/O pins are configured as inputs and pulled to $V_{SS}$
- $\overline{MCLR}$ = $V_{DD}$, WDT and FSCM are disabled
- No peripheral modules are operating; however, every peripheral is being clocked (PMDx bits are all zeroed)

**3:** These parameters are characterized, but not tested in manufacturing.

**TABLE 26-10: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS (CONTINUED)**

| DC CHARACTERISTICS | | | **Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)**<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ[1]** | **Max** | **Units** | **Conditions** |
| DI60a | IICL | **Input Low Injection Current** | 0 | -5[5,8] | — | mA | All pins except VDD, VSS, AVDD, AVSS, $\overline{\text{MCLR}}$, VCAP, SOSCI, SOSCO and RB14 |
| DI60b | IICH | **Input High Injection Current** | 0 | — | +5[6,7,8] | mA | All pins except VDD, VSS, AVDD, AVSS, $\overline{\text{MCLR}}$, VCAP, SOSCI, SOSCO, RB14 and digital 5V tolerant designated pins |
| DI60c | ∑ IICT | **Total Input Injection Current** (sum of all I/O and control pins) | -20[9] | — | +20[9] | mA | Absolute instantaneous sum of all ± input injection currents from all I/O pins<br>( \| IICL + \| IICH \| ) ≤ ∑ IICT |

**Note 1:** Data in “Typ” column is at 3.3V, +25°C unless otherwise stated.

**2:** The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current can be measured at different input voltages.

**3:** Negative current is defined as current sourced by the pin.

**4:** See the **“Pin Diagrams”** section for the 5V tolerant I/O pins.

**5:** VIL source < (VSS – 0.3). Characterized but not tested.

**6:** Non-5V tolerant pins, VIH source > (VDD + 0.3), 5V tolerant pins, VIH source > 5.5V. Characterized but not tested.

**7:** Digital 5V tolerant pins cannot tolerate any “positive” input injection current from input sources > 5.5V.

**8:** Injection currents > | 0 | can affect the ADC results by approximately 4-6 counts.

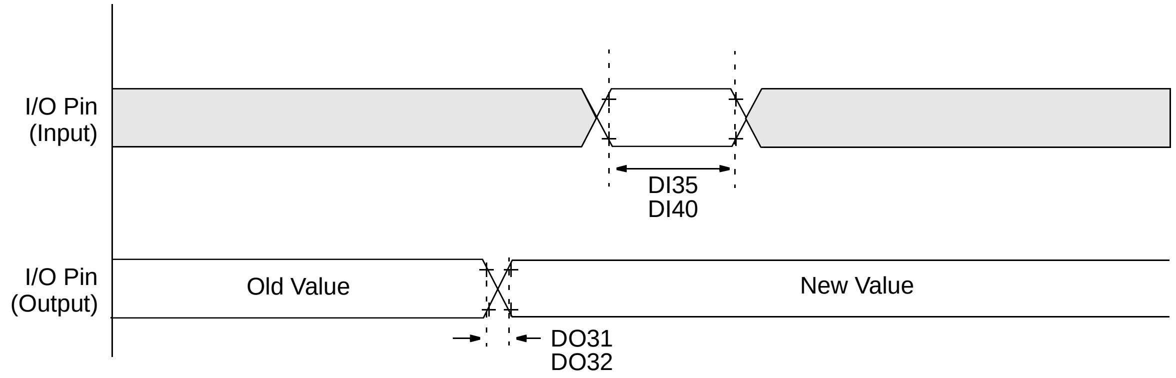
**9:** Any number and/or combination of I/O pins, not excluded under IICL or IICH conditions, are permitted provided the mathematical “absolute instantaneous” sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.

**TABLE 26-11: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS**

| **DC CHARACTERISTICS** | | | **Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)**<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ(1)** | **Max** | **Units** | **Conditions** |
| DO10 | VOL | **Output Low Voltage**<br>I/O Pins:<br>4x Sink Driver Pins – All Pins excluding OSCO | — | — | 0.4 | V | IOL ≤ 6 mA, VDD = 3.3V, See **Note 1** |
| | | **Output Low Voltage**<br>I/O Pins:<br>8x Sink Driver Pins – OSCO | — | — | 0.4 | V | IOL ≤ 10 mA, VDD = 3.3V, See **Note 1** |
| DO20 | VOH | **Output High Voltage**<br>I/O Pins:<br>4x Source Driver Pins – All Pins excluding OSCO | 2.4 | — | — | V | IOL ≥ -6 mA, VDD = 3.3V, See **Note 1** |
| | | **Output High Voltage**<br>I/O Pins:<br>8x Source Driver Pins – OSCO | 2.4 | — | — | V | IOL ≥ -10 mA, VDD = 3.3V, See **Note 1** |
| DO20A | VOH1 | **Output High Voltage**<br>I/O Pins:<br>4x Source Driver Pins – All Pins excluding OSCO | 1.5 | — | — | V | IOH ≥ -12 mA, VDD = 3.3V, See **Note 1** |
| | | | 2.0 | — | — | | IOH ≥ -11 mA, VDD = 3.3V, See **Note 1** |
| | | | 3.0 | — | — | | IOH ≥ -3 mA, VDD = 3.3V, See **Note 1** |
| | | **Output High Voltage**<br>I/O Pins:<br>8x Source Driver Pins – OSCO | 1.5 | — | — | V | IOH ≥ -16 mA, VDD = 3.3V, See **Note 1** |
| | | | 2.0 | — | — | | IOH ≥ -12 mA, VDD = 3.3V, See **Note 1** |
| | | | 3.0 | — | — | | IOH ≥ -4 mA, VDD = 3.3V, See **Note 1** |

**Note 1:** Data in “Typ” column is at 3.3V, +25°C unless otherwise stated.

**FIGURE 26-3: CLKO AND I/O TIMING CHARACTERISTICS**



**Note:** Refer to Figure 26-1 for load conditions.

**TABLE 26-20: I/O TIMING REQUIREMENTS**

| **AC CHARACTERISTICS** | **Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)**<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended |
|---|---|

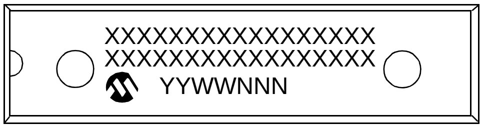
| Param No. | Symbol | Characteristic[(2)] | Min | Typ[(1)] | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| DO31 | TIOR | Port Output Rise Time | — | 10 | 25 | ns | |
| DO32 | TIOF | Port Output Fall Time | — | 10 | 25 | ns | |
| DI35 | TINP | INTx Pin High or Low Time (input) | 25 | — | — | ns | |
| DI40 | TRBP | CNx High or Low Time (input) | 2 | — | — | TCY | |

**Note 1:** Data in “Typ” column is at 3.3V, +25°C unless otherwise stated.

**2:** These parameters are characterized, but are not tested in manufacturing.

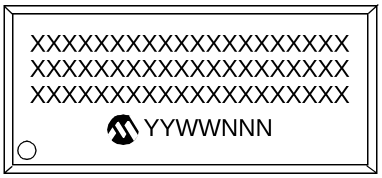
## 28.1 Package Marking Information (Continued)

28-Lead SPDIP

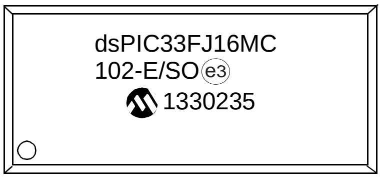


Example

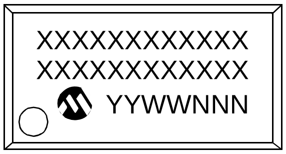
28-Lead SOIC



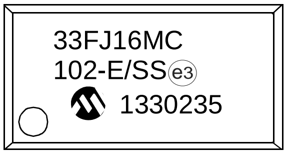
Example



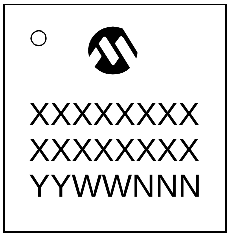
28-Lead SSOP



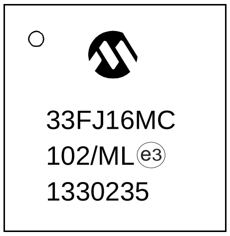
Example



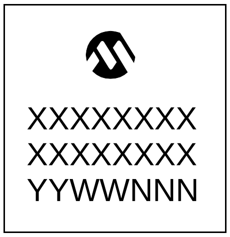
28-Lead QFN



Example



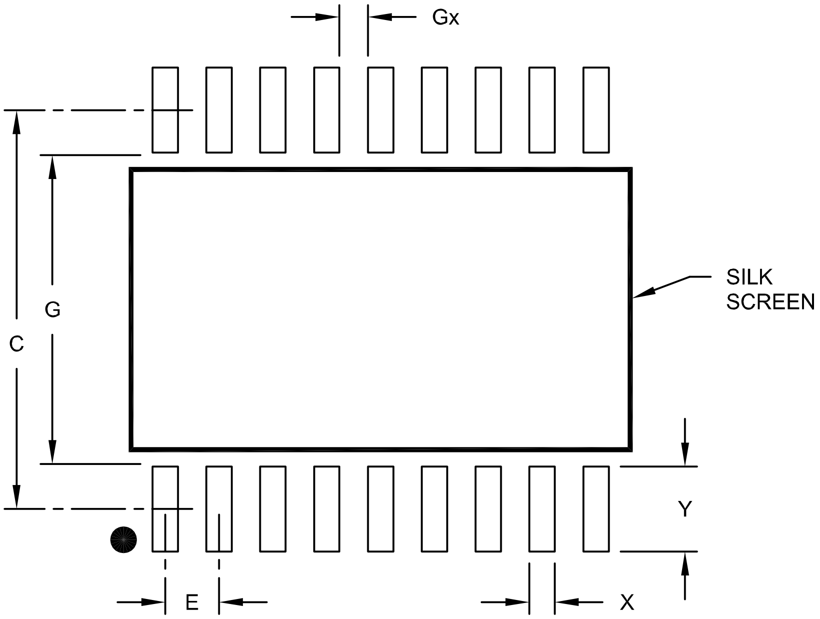
36-Lead VTLA



Example

## 18-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

| **Note:** | For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging |
|---|---|



RECOMMENDED LAND PATTERN

| | Units | MILLIMETERS | | |
|---|---|---|---|---|
| | Dimension Limits | MIN | NOM | MAX |
| Contact Pitch | E | 1.27 BSC | | |
| Contact Pad Spacing | C | | 9.40 | |
| Contact Pad Width | X | | | 0.60 |
| Contact Pad Length | Y | | | 2.00 |
| Distance Between Pads | Gx | 0.67 | | |
| Distance Between Pads | G | 7.40 | | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2051A