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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	16 MIPs
Connectivity	I <sup>2</sup> C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	21
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj16gp102-e-ss

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



#### **Pin Diagrams (Continued)**



### Pin Diagrams (Continued)



### **Pin Diagrams (Continued)**



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# FIGURE 1-1: dsPIC33FJ16(GP/MC)101/102 AND dsPIC33FJ32(GP/MC)101/102/104 BLOCK DIAGRAM



#### 3.5 Arithmetic Logic Unit (ALU)

The dsPIC33FJ16(GP/MC)101/102 and dsPIC33FJ32(GP/MC)101/102/104 ALU is 16 bits wide, and is capable of addition, subtraction, bit shifts and logic operations. Unless otherwise mentioned, arithmetic operations are 2's complement in nature. Depending on the operation, the ALU can affect the values of the Carry (C), Zero (Z), Negative (N), Overflow (OV) and Digit Carry (DC) Status bits in the SR register. The C and DC Status bits operate as Borrow and Digit Borrow bits, respectively, for subtraction operations.

The ALU can perform 8-bit or 16-bit operations, depending on the mode of the instruction that is used. Data for the ALU operation can come from the W register array or data memory, depending on the addressing mode of the instruction. Likewise, output data from the ALU can be written to the W register array or a data memory location.

Refer to the *"16-Bit MCU and DSC Programmer's Reference Manual"* (DS70157) for information on the SR bits affected by each instruction.

The dsPIC33FJ16(GP/MC)101/102 and dsPIC33FJ32(GP/MC)101/102/104 CPU incorporates hardware support for both multiplication and division. This includes a dedicated hardware multiplier and support hardware for 16-bit-divisor division.

#### 3.5.1 MULTIPLIER

Using the high-speed, 17-bit x 17-bit multiplier of the DSP engine, the ALU supports unsigned, signed or mixed-sign operation in several MCU multiplication modes:

- 16-bit x 16-bit signed
- 16-bit x 16-bit unsigned
- 16-bit signed x 5-bit (literal) unsigned
- 16-bit unsigned x 16-bit unsigned
- 16-bit unsigned x 5-bit (literal) unsigned
- 16-bit unsigned x 16-bit signed
- 8-bit unsigned x 8-bit unsigned

#### 3.5.2 DIVIDER

The divide block supports 32-bit/16-bit and 16-bit/16-bit signed and unsigned integer divide operations with the following data sizes:

- 32-bit signed/16-bit signed divide
- 32-bit unsigned/16-bit unsigned divide
- 16-bit signed/16-bit signed divide
- 16-bit unsigned/16-bit unsigned divide

The quotient for all divide instructions ends up in W0 and the remainder in W1. The 16-bit signed and unsigned DIV instructions can specify any W register for both the 16-bit divisor (Wn) and any W register (aligned) pair (W(m + 1):Wm) for the 32-bit dividend. The divide algorithm takes one cycle per bit of divisor, so both 32-bit/16-bit and 16-bit/16-bit instructions take the same number of cycles to execute.

### 3.6 DSP Engine

The DSP engine consists of a high-speed, 17-bit x 17-bit multiplier, a barrel shifter and a 40-bit adder/subtracter (with two target accumulators, round and saturation logic).

The dsPIC33FJ16(GP/MC)101/102 and dsPIC33FJ32(GP/MC)101/102/104 is a single-cycle instruction flow architecture; therefore, concurrent operation of the DSP engine with MCU instruction flow is not possible. However, some MCU ALU and DSP engine resources can be used concurrently by the same instruction (e.g., ED, EDAC).

The DSP engine can also perform inherent accumulatorto-accumulator operations that require no additional data. These instructions are ADD, SUB and NEG.

The DSP engine has options selected through bits in the CPU Core Control register (CORCON), as listed below:

- Fractional or Integer DSP Multiply (IF)
- Signed or Unsigned DSP Multiply (US)
- Conventional or Convergent Rounding (RND)
- · Automatic Saturation On/Off for ACCA (SATA)
- Automatic Saturation On/Off for ACCB (SATB)
- Automatic Saturation On/Off for Writes to Data Memory (SATDW)
- Accumulator Saturation mode Selection (ACCSAT)
- A block diagram of the DSP engine is shown in Figure 3-3.

TABLE 3-1:	DSP INSTRUCTIONS
	SUMMARY

Instruction	Algebraic Operation	ACC Write Back
CLR	A = 0	Yes
ED	$A = (x - y)^2$	No
EDAC	$A = A + (x - y)^2$	No
MAC	A = A + (x * y)	Yes
MAC	$A = A + x^2$	No
MOVSAC	No change in A	Yes
MPY	A = x * y	No
MPY	$A = x^2$	No
MPY.N	A = -x * y	No
MSC	A = A - x * y	Yes

U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
		_	SCK1R4 <sup>(1)</sup>	SCK1R3 <sup>(1)</sup>	SCK1R2 <sup>(1)</sup>	SCK1R1 <sup>(1)</sup>	SCK1R0 <sup>(1)</sup>
bit 15							bit 8
U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	—	—	SDI1R4 <sup>(1)</sup>	SDI1R3 <sup>(1)</sup>	SDI1R2 <sup>(1)</sup>	SDI1R1 <sup>(1)</sup>	SDI1R0 <sup>(1)</sup>
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	l as '0'	
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkn	iown
bit 15-13	Unimplement	ted: Read as '	)'				
bit 12-8	SCK1R<4:0>	: Assign SPI1 (	Clock Input (S	CK1IN) to the	Corresponding	RPn Pin bits <sup>(1)</sup>	
	11111 = Inpu	t tied to Vss					
	11110 = Rese	erved					
	•						
	•						
	11010 = Rese	erved					
	11001 = Inpu	t tied to RP25					
	•						
	00001 = Inpu	t tied to RP1					
	00000 = Inpu	t tied to RP0					
bit 7-5	Unimplement	ted: Read as 'd	)'				
bit 4-0	SDI1R<4:0>:	Assign SPI1 D	ata Input (SDI	1) to the Corre	esponding RPn	Pin bits <sup>(1)</sup>	
	11111 = Inpu	t tied to Vss					
	11110 = Rese	erved					
	•						
	•						
	11010 = Rese	erved					
	11001 = Inpu	t tied to RP25					
	•						
	•						
	00001 <b>= l</b> ppu	t tied to RP1					
	00000 = Input	t tied to RP0					
	· · · · · · · · · · · · · · · · · · ·						

#### REGISTER 10-9: RPINR20: PERIPHERAL PIN SELECT INPUT REGISTER 20



## 11.0 **TIMER1**

- Note 1: This data sheet summarizes the features of the dsPIC33FJ16(GP/MC)101/102 and dsPIC33FJ32(GP/MC)101/102/104 family devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Timers" (DS70205) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
  - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The Timer1 module is a 16-bit timer, which can serve as the time counter for the Real-Time Clock (RTC) or operate as a free-running interval timer/counter. Timer1 can operate in three modes:

- 16-Bit Timer
- 16-Bit Synchronous Counter
- 16-Bit Asynchronous Counter

Timer1 also supports these features:

- Timer gate operation
- · Selectable prescaler settings
- Timer operation during CPU Idle and Sleep modes
- Interrupt on 16-bit Period register match or falling edge of external gate signal

Figure 11-1 presents a block diagram of the 16-bit timer module.

To configure Timer1 for operation:

- 1. Load the timer value into the TMR1 register.
- 2. Load the timer period value into the PR1 register.
- 3. Select the timer prescaler ratio using the TCKPS<1:0> bits in the T1CON register.
- 4. Set the Clock and Gating modes using the TCS and TGATE bits in the T1CON register.
- 5. Set or clear the TSYNC bit in T1CON to select synchronous or asynchronous operation.
- 6. If interrupts are required, set the Timer1 Interrupt Enable bit, T1IE. Use the Timer1 Interrupt Priority bits, T1IP<2:0>, to set the interrupt priority.
- 7. Set the TON bit (= 1) in the T1CON register.



#### FIGURE 11-1: 16-BIT TIMER1 MODULE BLOCK DIAGRAM

NOTES:

### 14.1 Output Compare Modes

Configure the Output Compare modes by setting the appropriate Output Compare Mode bits (OCM<2:0>) in the Output Compare x Control (OCxCON<2:0>) register. Table 14-1 lists the different bit settings for the Output Compare modes. Figure 14-2 illustrates the output compare operation for various modes. The user

TABLE 14-1: OUTPUT COMPARE x MODES

application must disable the associated timer when writing to the Output Compare Control registers to avoid malfunctions.

Note: See "Output Compare" in the "dsPIC33/ PIC24 Family Reference Manual" (DS70209) for OCxR and OCxRS register restrictions.

OCM<2:0>	Mode	OCx Pin Initial State	OCx Interrupt Generation
000	Module Disabled	Controlled by GPIO register	_
001	Active-Low One-Shot	0	OCx Rising Edge
010	Active-High One-Shot	1	OCx Falling Edge
011	Toggle	Current output is maintained	OCx Rising and Falling Edge
100	Delayed One-Shot	0	OCx Falling Edge
101	Continuous Pulse	0	OCx Falling Edge
110	PWM without Fault Protection	0, if OCxR is zero 1, if OCxR is non-zero	No Interrupt
111	PWM with Fault Protection	0, if OCxR is zero 1, if OCxR is non-zero	OCFA Falling Edge for OC1 to OC4

#### FIGURE 14-2: OUTPUT COMPARE x OPERATION



R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0		
FRMEN	SPIFSD	FRMPOL	—	—	—	—	—		
bit 15							bit 8		
U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	U-0		
—	—	—	—	—	—	FRMDLY	—		
bit 7							bit 0		
Legend:									
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	as '0'			
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cleared		x = Bit is unkn	own		
bit 15	FRMEN: Frar	med SPIx Supp	ort bit						
	1 = Framed S	SPIx support is	enabled ( <mark>SS</mark> x	pin is used as	Frame Sync pu	Ilse input/outpu	t)		
	0 = Framed S	SPIx support is	disabled						
bit 14	SPIFSD: Fran	me Sync Pulse	Direction Cor	ntrol bit					
	1 = Frame Sy	nc pulse input	(slave)						
hit 12		ama Svna Bula	o Dolority bit						
DIL 13	1 - Erame Sv	une oyne ruis vne oulse is act							
	0 = Frame Sy	nc pulse is act	ive-low						
bit 12-2	Unimplemen	ted: Read as '	0'						
bit 1	FRMDLY: Fra	ame Sync Pulse	e Edge Select	bit					
	1 = Frame Sy	nc pulse coinci	ides with first	bit clock					
	0 = Frame Sy	nc pulse prece	des first bit cl	ock					
bit 0	Unimplemen	Unimplemented: This bit must not be set to '1' by the user application							

### REGISTER 16-3: SPIxCON2: SPIx CONTROL REGISTER 2



FIGURE 17-1:  $I^2C^{TM}$  BLOCK DIAGRAM (x = 1)

# **REGISTER 21-8:** ALRMVAL (WHEN ALRMPTR<1:0> = 10): ALARM MONTH AND DAY VALUE REGISTER<sup>(1)</sup>

U-0	U-0	U-0	R/W-x	R/W-x	R/W-x R/W-x		R/W-x
—	—	—	MTHTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0
bit 15							bit 8

U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	DAYTEN1	DAYTEN0	DAYONE3	DAYONE2	DAYONE1	DAYONE0
bit 7							bit 0

Legend:					
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'			
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

bit 15-13	Unimplemented: Read as '0'
bit 12	MTHTEN0: Binary Coded Decimal Value of Month's Tens Digit bit
	Contains a value of 0 or 1.
bit 11-8	MTHONE<3:0>: Binary Coded Decimal Value of Month's Ones Digit bits
	Contains a value from 0 to 9.
bit 7-6	Unimplemented: Read as '0'
bit 5-4	DAYTEN<1:0>: Binary Coded Decimal Value of Day's Tens Digit bits
	Contains a value from 0 to 3.
bit 3-0	DAYONE<3:0>: Binary Coded Decimal Value of Day's Ones Digit bits
	Contains a value from 0 to 9.

**Note 1:** A write to this register is only allowed when RTCWREN = 1.

DC CHARACTERISTICS			$\label{eq:standard operating Conditions: 3.0V to 3.6V} \end{tabular} \begin{tabular}{lllllllllllllllllllllllllllllllllll$				
Param No.	Symbol	Characteristic <sup>(3)</sup>	Min	Тур <sup>(1)</sup>	Max	Units	Conditions
-		Program Flash Memory					
D130a	Eр	Cell Endurance	10,000	—	—	E/W	-40°C to +125°C
D131	Vpr	VDD for Read	Vmin	_	3.6	V	VMIN = Minimum operating voltage
D132b	Vpew	VDD for Self-Timed Write	VMIN	—	3.6	V	VMIN = Minimum operating voltage
D134	Tretd	Characteristic Retention	20	—	—	Year	Provided no other specifications are violated
D135	IDDP	Supply Current during Programming	—	10	—	mA	
D137a	TPE	Page Erase Time	20.1	_	26.5	ms	TPE = 168517 FRC cycles, TA = +85°C, See <b>Note 2</b>
D137b	TPE	Page Erase Time	19.5	_	27.3	ms	TPE = 168517 FRC cycles, TA = +125°C, See <b>Note 2</b>
D138a	Tww	Word Write Cycle Time	47.4	—	49.3	μs	Tww = 355 FRC cycles, TA = +85°C, See <b>Note 2</b>
D138b	Tww	Word Write Cycle Time	47.4	—	49.3	μs	Tww = 355 FRC cycles, Ta = +125°C, See <b>Note 2</b>

#### TABLE 26-12: DC CHARACTERISTICS: PROGRAM MEMORY

**Note 1:** Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.

2: Other conditions: FRC = 7.37 MHz, TUN<5:0> = b'011111 (for Min), TUN<5:0> = b'100000 (for Max). This parameter depends on the FRC accuracy (see Table 26-18) and the value of the FRC Oscillator Tuning register (see Register 8-3). For complete details on calculating the Minimum and Maximum time, see Section 5.3 "Programming Operations".

3: These parameters are ensured by design, but are not characterized or tested in manufacturing.

#### TABLE 26-13: INTERNAL VOLTAGE REGULATOR SPECIFICATIONS

DC CHARACTERISTICS		$\begin{tabular}{ l l l l l l l l l l l l l l l l l l l$					
Param No.	Symbol	Characteristics	Min	Тур	Max	Units	Comments
	Cefc	External Filter Capacitor Value <sup>(1)</sup>	4.7	10	_	μF	Capacitor must be low series resistance (< 5 ohms)

**Note 1:** Typical VCAP voltage = 2.5V when VDD  $\ge$  VDDMIN.

# TABLE 26-34:SPIX SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0) TIMING<br/>REQUIREMENTS FOR dsPIC33FJ16(GP/MC)10X

AC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions: 2.4V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^\circ C \leq TA \leq +85^\circ C \mbox{ for Industrial} \\ & -40^\circ C \leq TA \leq +125^\circ C \mbox{ for Extended} \end{array}$				
Param No.	Symbol	Characteristic <sup>(1)</sup>	Min	Typ <sup>(2)</sup>	Max	Units	Conditions
SP70	TscP	Maximum SCKx Input Frequency	—	—	11	MHz	See Note 3
SP72	TscF	SCKx Input Fall Time	_	—		ns	See Parameter DO32 and <b>Note 4</b>
SP73	TscR	SCKx Input Rise Time	—	_		ns	See Parameter DO31 and <b>Note 4</b>
SP30	TdoF	SDOx Data Output Fall Time	—	—	_	ns	See Parameter DO32 and <b>Note 4</b>
SP31	TdoR	SDOx Data Output Rise Time	—	—	_	ns	See Parameter DO31 and <b>Note 4</b>
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	_		ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	—		ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	—	_	ns	
SP50	TssL2scH, TssL2scL	$\overline{SSx} \downarrow$ to SCKx $\uparrow$ or SCKx Input	120	_		ns	
SP51	TssH2doZ	SSx ↑ to SDOx Output High-Impedance	10	—	50	ns	See Note 4
SP52	TscH2ssH TscL2ssH	SSx after SCKx Edge	1.5 TCY + 40	—	—	ns	See Note 4
SP60	TssL2doV	SDOx Data Output Valid after SSx Edge	—	—	50	ns	

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.

**3:** The minimum clock period for SCKx is 91 ns. Therefore, the SCKx clock generated by the Master must not violate this specification.

4: Assumes 50 pF load on all SPIx pins.

AC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended				
Param.	Symbol	Charac	teristic	Min	Max	Units	Conditions	
IS10	TLO:SCL	Clock Low Time	100 kHz mode	4.7	—	μS	Device must operate at a minimum of 1.5 MHz	
			400 kHz mode	1.3	—	μS	Device must operate at a minimum of 10 MHz	
			1 MHz mode <sup>(1)</sup>	0.5	—	μS		
IS11	THI:SCL	Clock High Time	100 kHz mode	4.0	—	μS	Device must operate at a minimum of 1.5 MHz	
			400 kHz mode	0.6	—	μS	Device must operate at a minimum of 10 MHz	
			1 MHz mode <sup>(1)</sup>	0.5		μS		
IS20	TF:SCL	SDAx and SCLx Fall Time	100 kHz mode	_	300	ns	CB is specified to be from	
			400 kHz mode	20 + 0.1 Св	300	ns	10 to 400 pF	
			1 MHz mode <sup>(1)</sup>	_	100	ns		
IS21	TR:SCL	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	CB is specified to be from	
			400 kHz mode	20 + 0.1 Св	300	ns	10 to 400 pF	
			1 MHz mode <sup>(1)</sup>	—	300	ns		
IS25	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	ns		
			400 kHz mode	100		ns		
			1 MHz mode <sup>(1)</sup>	100		ns		
IS26	THD:DAT	Data Input Hold Time	100 kHz mode	0		μs		
			400 kHz mode	0	0.9	μs		
			1 MHz mode <sup>(1)</sup>	0	0.3	μs		
IS30	TSU:STA	Start Condition Setup Time	100 kHz mode	4.7	—	μs	Only relevant for Repeated Start condition	
			400 kHz mode	0.6		μs		
			1 MHz mode <sup>(1)</sup>	0.25	—	μs		
IS31	THD:STA	Start Condition Hold Time	100 kHz mode	4.0	—	μS	After this period, the first	
			400 kHz mode	0.6	—	μs	clock pulse is generated	
			1 MHz mode <sup>(1)</sup>	0.25	—	μS		
IS33	Τςυ:ςτο	Stop Condition Setup Time	100 kHz mode	4.7	—	μS		
			400 kHz mode	0.6	_	μS		
			1 MHz mode <sup>(1)</sup>	0.6		μS		
IS34	THD:STO	Stop Condition Hold Time	100 kHz mode	4000		ns		
			400 kHz mode	600		ns		
			1 MHz mode <sup>(1)</sup>	250		ns		
IS40	TAA:SCL	Output Valid from Clock	100 kHz mode	0	3500	ns		
			400 kHz mode	0	1000	ns		
			1 MHz mode <sup>(1)</sup>	0	350	ns		
IS45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	_	μS	Time the bus must be free	
			400 kHz mode	1.3		μs	before a new transmission	
			1 MHz mode <sup>(1)</sup>	0.5	_	μS	can start	
IS50	Св	Bus Capacitive Loading			400	pF		

### TABLE 26-46: I2Cx BUS DATA TIMING REQUIREMENTS (SLAVE MODE)

Note 1: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to $3.6V^{(4)}$ (unless otherwise stated)Operating temperature-40°C $\leq$ TA $\leq$ +85°C for Industrial					
			-40°C $\leq$ TA $\leq$ +125°C for Extended					
Param No.	Symbol	Characteristic	Min.	Тур	Max.	Units	Conditions	
10-Bit ADC Accuracy – Measurements with AVDD/AVss <sup>(3)</sup>								
AD20b	Nr	Resolution	10 Data Bits		bits			
AD21b	INL	Integral Nonlinearity	-1	—	+1	LSb	VINL = AVSS = 0V, AVDD = 3.6V	
AD22b	DNL	Differential Nonlinearity	>-1		<1	LSb	VINL = AVSS = 0V, AVDD = 3.6V	
AD23b	Gerr	Gain Error	3	7	15	LSb	VINL = AVSS = 0V, AVDD = 3.6V	
AD24b	EOFF	Offset Error	1.5	3	7	LSb	VINL = AVSS = 0V, AVDD = 3.6V	
AD25b	_	Monotonicity	_		_	-	Guaranteed <sup>(1)</sup>	
Dynamic Performance (10-Bit Mode) <sup>(2)</sup>								
AD30b	THD	Total Harmonic Distortion	—	—	-64	dB		
AD31b	SINAD	Signal to Noise and Distortion	57	58.5	_	dB		
AD32b	SFDR	Spurious Free Dynamic Range	72	—	—	dB		
AD33b	FNYQ	Input Signal Bandwidth	—	—	550	kHz		
AD34b	ENOB	Effective Number of Bits	9.16	9.4	—	bits		

## TABLE 26-48: 10-BIT ADC MODULE SPECIFICATIONS

**Note 1:** The Analog-to-Digital conversion result never decreases with an increase in the input voltage and has no missing codes.

2: These parameters are characterized by similarity, but are not tested in manufacturing.

3: These parameters are characterized, but are tested at 20 ksps only.

4: Overall functional device operation at VBOR < VDD < VDDMIN is guaranteed but not characterized. All device analog modules, such as the ADC, etc., will function but with degraded performance below VDDMIN

### 28.1 Package Marking Information (Continued)

#### 28-Lead SPDIP



28-Lead SOIC





Example



#### 28-Lead SSOP



#### 28-Lead QFN



#### 36-Lead VTLA



## Example



#### Example



#### Example



SPIx Master Transmit Mode (Half-Duplex)
for dsPIC33FJ16(GP/MC)10X
SPIx Master Transmit Mode (Half-Duplex)
for dsPIC33FJ32(GP/MC)10X
SPIx Slave Mode (Full-Duplex, CKE = 0, CKP = 0,
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