Microchip Technology - DSPIC33FJ16GP102-I/SS Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	16 MIPs
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	21
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj16gp102-i-ss

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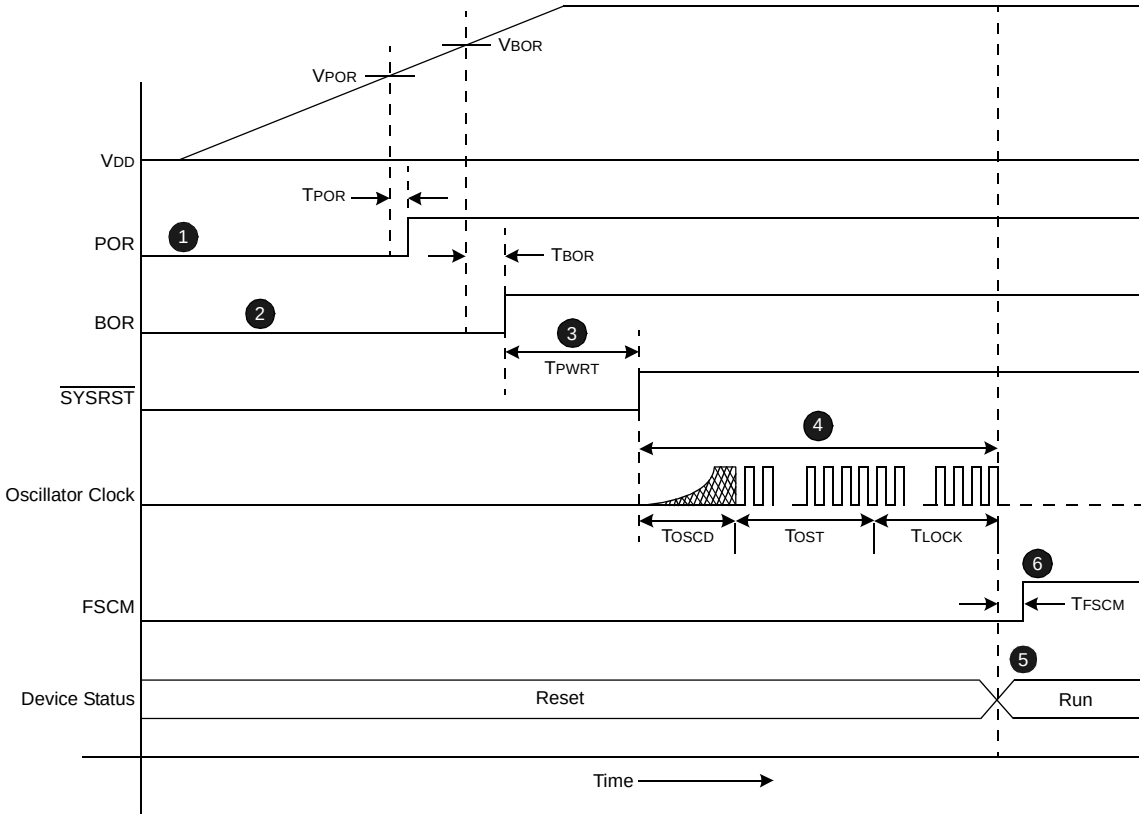
NOTES:

FIGURE 6-2: SYSTEM RESET TIMING



1. **POR:** A POR circuit holds the device in Reset when the power supply is turned on. The POR circuit is active until VDD crosses the VPOR threshold and the delay, TPOR, has elapsed.
2. **BOR:** The on-chip voltage regulator has a BOR circuit that keeps the device in Reset until VDD crosses the VBOR threshold and the delay, TBOR, has elapsed. The delay, TBOR, ensures the voltage regulator output becomes stable.
3. **PWRT Timer:** The Power-up Timer continues to hold the processor in Reset for a specific period of time (TPWRT) after a BOR. The delay, TPWRT, ensures that the system power supplies have stabilized at the appropriate level for full-speed operation. After the delay, TPWRT, has elapsed, the SYSRST becomes inactive, which in turn, enables the selected oscillator to start generating clock cycles.
4. **Oscillator Delay:** The total delay for the clock to be ready for various clock source selections is given in Table 6-1. Refer to **Section 8.0 "Oscillator Configuration"** for more information.
5. When the oscillator clock is ready, the processor begins execution from location, 0x000000. The user application programs a GOTO instruction at the Reset address, which redirects program execution to the appropriate start-up routine.
6. The Fail-Safe Clock Monitor (FSCM), if enabled, begins to monitor the system clock when the system clock is ready and the delay, TFSCM, has elapsed.

TABLE 6-2: OSCILLATOR PARAMETERS

Symbol	Parameter	Value
VPOR	POR Threshold	1.8V nominal
TPOR	POR Extension Time	30 μs maximum
VBOR	BOR Threshold	2.5V nominal
TBOR	BOR Extension Time	100 μs maximum
TPWRT	Power-up Time Delay	64 ms nominal
TFSCM	Fail-Safe Clock Monitor Delay	900 μs maximum

Note: When the device exits the Reset condition (begins normal operation), the device operating parameters (voltage, frequency, temperature, etc.) must be within their operating ranges; otherwise, the device may not function correctly. The user application must ensure that the delay between the time power is first applied, and the time SYSRST becomes inactive, is long enough to get all operating parameters within specification.

REGISTER 7-27: IPC19: INTERRUPT PRIORITY CONTROL REGISTER 19

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	CTMUIP2	CTMUIP1	CTMUIP0	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-7 **Unimplemented:** Read as ‘0’

bit 6-4 **CTMUIP<2:0>:** CTMU Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3-0 **Unimplemented:** Read as ‘0’

8.2 Oscillator Control Registers

REGISTER 8-1: OSCCON: OSCILLATOR CONTROL REGISTER(1)

U-0	R-0	R-0	R-0	U-0	R/W-y	R/W-y	R/W-y
—	COSC2	COSC1	COSC0	—	NOSC2(2)	NOSC1(2)	NOSC0(2)
bit 15							bit 8

R/W-0	R/W-0	R-0	U-0	R/C-0	U-0	R/W-0	R/W-0
CLKLOCK	IOLOCK	LOCK	—	CF	—	LPOSCEN	OSWEN
bit 7							bit 0

Legend:	C = Clearable bit	y = Value set from Configuration bits on POR	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **COSC<2:0>:** Current Oscillator Selection bits (read-only)
111 = Fast RC Oscillator (FRC) with Divide-by-n
110 = Fast RC Oscillator (FRC) with Divide-by-16
101 = Low-Power RC Oscillator (LPRC)
100 = Secondary Oscillator (SOSC)
011 = Primary Oscillator (MS, EC) with PLL
010 = Primary Oscillator (MS, HS, EC)
001 = Fast RC Oscillator (FRC) with Divide-by-n and PLL (FRCPLL)
000 = Fast RC Oscillator (FRC)

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **NOSC<2:0>:** New Oscillator Selection bits(2)
111 = Fast RC Oscillator (FRC) with Divide-by-n
110 = Fast RC Oscillator (FRC) with Divide-by-16
101 = Low-Power RC Oscillator (LPRC)
100 = Secondary Oscillator (SOSC)
011 = Primary Oscillator (MS, EC) with PLL
010 = Primary Oscillator (MS, HS, EC)
001 = Fast RC Oscillator (FRC) with Divide-by-n and PLL (FRCPLL)
000 = Fast RC Oscillator (FRC)

bit 7 **CLKLOCK:** Clock Lock Enable bit
If Clock Switching is Enabled and FSCM is Disabled (FCKSM<1:0> (FOSC<7:6>) = 0b01):
1 = Clock switching is disabled, system clock source is locked
0 = Clock switching is enabled, system clock source can be modified by clock switching

bit 6 **IOLOCK:** Peripheral Pin Select Lock bit
1 = Peripheral Pin Select is locked, a write to Peripheral Pin Select registers is not allowed
0 = Peripheral Pin Select is not locked, a write to Peripheral Pin Select registers is allowed

bit 5 **LOCK:** PLL Lock Status bit (read-only)
1 = Indicates that PLL is in lock or PLL start-up timer is satisfied
0 = Indicates that PLL is out of lock, start-up timer is in progress or PLL is disabled

bit 4 **Unimplemented:** Read as '0'

Note 1: Writes to this register require an unlock sequence. Refer to **"Oscillator (Part VI)"** (DS70644) in the *"dsPIC33/PIC24 Family Reference Manual"* for details.

2: Direct clock switches between any primary oscillator mode with PLL and FRCPLL mode are not permitted. This applies to clock switches in either direction. In these instances, the application must switch to FRC mode as a transitional clock source between the two PLL modes.

10.4.3 CONTROLLING CONFIGURATION CHANGES

Because peripheral remapping can be changed during run time, some restrictions on peripheral remapping are needed to prevent accidental configuration changes. dsPIC33FJ16(GP/MC)101/102 and dsPIC33FJ32(GP/MC)101/102/104 devices include three features to prevent alterations to the peripheral map:

- Control register lock sequence
- Continuous state monitoring
- Configuration bit pin select lock

10.4.3.1 Control Register Lock

Under normal operation, writes to the RPINRx and RPORx registers are not allowed. Attempted writes appear to execute normally, but the contents of the registers remain unchanged. To change these registers, they must be unlocked in hardware. The register lock is controlled by the IOLOCK bit (OSCCON<6>). Setting IOLOCK prevents writes to the control registers; clearing IOLOCK allows writes.

To set or clear IOLOCK, a specific command sequence must be executed:

1. Write 0x46 to OSCCON<7:0>.
2. Write 0x57 to OSCCON<7:0>.
3. Clear (or set) IOLOCK as a single operation.

Note: MPLAB® C30 provides built-in C language functions for unlocking the OSCCON register:

```
__builtin_write_OSCCONL(value)
__builtin_write_OSCCONH(value)
```

See MPLAB IDE Help for more information.

Unlike the similar sequence with the oscillator's LOCK bit, IOLOCK remains in one state until changed. This allows all of the Peripheral Pin Selects to be configured with a single unlock sequence followed by an update to all control registers, then locked with a second lock sequence.

10.4.3.2 Continuous State Monitoring

In addition to being protected from direct writes, the contents of the RPINRx and RPORx registers are constantly monitored in hardware by shadow registers. If an unexpected change in any of the registers occurs (such as cell disturbances caused by ESD or other external events), a Configuration Mismatch Reset will be triggered.

10.4.3.3 Configuration Bit Pin Select Lock

As an additional level of safety, the device can be configured to prevent more than one write session to the RPINRx and RPORx registers. The IOL1WAY (FOSC<5>) Configuration bit blocks the IOLOCK bit from being cleared after it has been set once. If IOLOCK remains set, the register unlock procedure will not execute and the Peripheral Pin Select Control registers cannot be written to. The only way to clear the bit and re-enable peripheral remapping is to perform a device Reset.

In the default (unprogrammed) state, IOL1WAY is set, restricting users to one write session. Programming IOL1WAY allows user applications unlimited access (with the proper use of the unlock sequence) to the Peripheral Pin Select registers.

REGISTER 10-2: RPINR1: PERIPHERAL PIN SELECT INPUT REGISTER 1

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	—	INT2R4	INT2R3	INT2R2	INT2R1	INT2R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-5 **Unimplemented:** Read as ‘0’

bit 4-0 **INT2R<4:0>:** Assign External Interrupt 2 (INTR2) to the Corresponding RPn Pin bits

11111 = Input tied to Vss
11110 = Reserved
.
.
.
11010 = Reserved
11001 = Input tied to RP25
.
.
.
00001 = Input tied to RP1
00000 = Input tied to RP0

REGISTER 10-21: RPOR10: PERIPHERAL PIN SELECT OUTPUT REGISTER 10

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	RP21R<4:0>(1)				
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	RP20R<4:0>(1)				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **RP21R<4:0>:** Peripheral Output Function is Assigned to RP21 Output Pin bits(1)
(see Table 10-2 for peripheral function numbers)

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **RP20R<4:0>:** Peripheral Output Function is Assigned to RP20 Output Pin bits(1)
(see Table 10-2 for peripheral function numbers)

Note 1: These bits are available in dsPIC33FJ32(GP/MC)104 devices only.

REGISTER 10-22: RPOR11: PERIPHERAL PIN SELECT OUTPUT REGISTER 11

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	RP23R<4:0>(1)				
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	RP22R<4:0>(1)				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **RP23R<4:0>:** Peripheral Output Function is Assigned to RP23 Output Pin bits(1)
(see Table 10-2 for peripheral function numbers)

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **RP22R<4:0>:** Peripheral Output Function is Assigned to RP22 Output Pin bits(1)
(see Table 10-2 for peripheral function numbers)

Note 1: These bits are available in dsPIC33FJ32(GP/MC)104 devices only.

REGISTER 10-23: RPOR12: PERIPHERAL PIN SELECT OUTPUT REGISTER 12

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	RP25R<4:0>(1)				
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	RP24R<4:0>(1)				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **RP25R<4:0>:** Peripheral Output Function is Assigned to RP25 Output Pin bits(1)
(see Table 10-2 for peripheral function numbers)

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **RP24R<4:0>:** Peripheral Output Function is Assigned to RP24 Output Pin bits(1)
(see Table 10-2 for peripheral function numbers)

Note 1: These bits are available in dsPIC33FJ32(GP/MC)104 devices only.

NOTES:

15.0 MOTOR CONTROL PWM MODULE

Note 1: This data sheet summarizes the features of the dsPIC33FJ16(GP/MC)101/102 and dsPIC33FJ32(GP/MC)101/102/104 family devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Motor Control PWM"** (DS70187) in the "*dsPIC33/PIC24 Family Reference Manual"*, which is available on the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33FJ16MC10X devices have a 6-channel Pulse-Width Modulation (PWM) module.

The PWM module has the following features:

- Up to 16-bit resolution
- On-the-fly PWM frequency changes
- Edge-Aligned and Center-Aligned Output modes
- Single Pulse Generation mode
- Interrupt support for asymmetrical updates in Center-Aligned mode
- Output override control for Electrically Commutative Motor (ECM) operation or BLDC
- Special event comparator for scheduling other peripheral events
- Fault pins to optionally drive each of the PWM output pins to a defined state
- Duty cycle updates configurable to be immediate or synchronized to the PWM time base

15.1 PWM1: 6-Channel PWM Module

This module simplifies the task of generating multiple synchronized PWM outputs. The following power and motion control applications are supported by the PWM module:

- 3-Phase AC Induction Motor
- Switched Reluctance (SR) Motor
- Brushless DC (BLDC) Motor
- Uninterruptible Power Supply (UPS)

This module contains three duty cycle generators, numbered 1 through 3. The module has six PWM output pins, numbered PWM1H1/PWM1L1 through PWM1H3/PWM1L3. The six I/O pins are grouped into high/low numbered pairs, denoted by the suffix H or L, respectively. For complementary loads, the low PWM pins are always the complement of the corresponding high I/O pin.

15.2 PWM Faults

The Motor Control PWM module incorporates up to two Fault inputs, FLTA1 and FLTB1. These Fault inputs are implemented with Class B safety features. These features ensure that the PWM outputs enter a safe state when either of the Fault inputs is asserted.

The FLTA1 and FLTB1 pins, when enabled and having ownership of a pin, also enable a soft internal pull-down resistor. The soft pull-down provides a safety feature by automatically asserting the Fault should a break occur in the Fault signal connection.

The implementation of internal pull-down resistors is dependent on the device variant. Table 15-1 describes which devices and pins implement the internal pull-down resistors.

TABLE 15-1: INTERNAL PULL-DOWN RESISTORS ON PWM FAULT PINS

Device	Fault Pin	Internal Pull-Down Implemented?
dsPIC33FJXXMC101	FLTA1	No
dsPIC33FJXXMC102	FLTA1	Yes
	FLTB1	Yes
dsPIC33FJ32MC104	FLTA1	Yes
	FLTB1	Yes

On devices without internal pull-downs on the Fault pin, it is recommended to connect an external pull-down resistor for Class B safety features.

15.2.1 PWM FAULTS AT RESET

During any Reset event, the PWM module maintains ownership of both PWM Fault pins. At Reset, both Faults are enabled in latched mode to guarantee the fail-safe power-up of the application. The application software must clear both of the PWM Faults before enabling the Motor Control PWM module.

The Fault condition must be cleared by the external circuitry driving the Fault input pin high and clearing the Fault interrupt flag. After the Fault pin condition has been cleared, the PWM module restores the PWM output signals on the next PWM period or half-period boundary.

Refer to **"Motor Control PWM"** (DS70187) in the "*dsPIC33/PIC24 Family Reference Manual*" for more information on the PWM Faults.

Note:	The number of PWM Faults mapped to the device pins depend on the specific variant. Regardless of the variant, both Faults will be enabled during any Reset event. The application must clear both FLTA1 and FLTB1 before enabling the Motor Control PWM module. Refer to the specific device pin diagrams to see which Fault pins are mapped to the device pins.

15.3 Write-Protected Registers

On dsPIC33FJ(16/32)MC10X devices, write protection is implemented for the PWMxCON1, PxFLTACON and PxFLTBCON registers. The write protection feature prevents any inadvertent writes to these registers. The write protection feature can be controlled by the PWMLOCK Configuration bit in the FOSCSEL Configuration register. The default state of the write protection feature is enabled (PWMLOCK = 1). The write protection feature can be disabled by configuring PWMLOCK (FOSCSEL<6>) = 0.

The user application can gain access to these locked registers either by configuring the PWMLOCK bit (FOSCSEL<6>) = 0 or by performing the unlock sequence. To perform the unlock sequence, the user application must write two consecutive values (0xABCD and 0x4321) to the PWMxKEY register to perform the unlock operation. The write access to the PWMxCON1, PxFLTACON or PxFLTBCON registers must be the next SFR access following the unlock process. There can be no other SFR accesses during the unlock process and subsequent write access.

To write to all registers, the PWMxCON1, PxFLTACON and PxFLTBCON registers require three unlock operations.

The correct unlocking sequence is described in Example 15-1 and Example 15-2.

REGISTER 17-2: I2CxSTAT: I2Cx STATUS REGISTER (CONTINUED)

bit 4 **P:** Stop bit
1 = Indicates that a Stop bit has been detected last
0 = Stop bit was not detected last
Hardware sets or clears when Start, Repeated Start or Stop is detected.

bit 3 **S:** Start bit
1 = Indicates that a Start (or Repeated Start) bit has been detected last
0 = Start bit was not detected last
Hardware sets or clears when Start, Repeated Start or Stop is detected.

bit 2 **R_W:** Read/Write Information bit (when operating as I^2C slave)
1 = Read – Indicates data transfer is output from slave
0 = Write – Indicates data transfer is input to slave
Hardware sets or clears after reception of an I^2C device address byte.

bit 1 **RBF:** Receive Buffer Full Status bit
1 = Receive is complete, I2CxRCV is full
0 = Receive is not complete, I2CxRCV is empty
Hardware sets when I2CxRCV is written with received byte. Hardware clears when software reads I2CxRCV.

bit 0 **TBF:** Transmit Buffer Full Status bit
1 = Transmit in progress, I2CxTRN is full
0 = Transmit complete, I2CxTRN is empty
Hardware sets when software writes to I2CxTRN. Hardware clears at completion of data transmission.

REGISTER 19-7: AD1PCFGL: ADC1 PORT CONFIGURATION REGISTER LOW(1,2,3)

R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PCFG15(4,5)	—	—	PCFG<12:0>(4,5,7)				
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PCFG<7:0>(4,5,6)							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **PCFG15:** ADC1 Port Configuration Control bit(4,5)
1 = Port pin is in Digital mode, port read input is enabled, ADC1 input multiplexer is connected to AVSS
0 = Port pin is in Analog mode, port read input is disabled, ADC1 samples pin voltage

bit 14-13 **Unimplemented:** Read as '0'

bit 12-0 **PCFG<12:0>:** ADC1 Port Configuration Control bits(4,5,6,7)
1 = Port pin is in Digital mode, port read input is enabled, ADC1 input multiplexer is connected to AVSS
0 = Port pin is in Analog mode, port read input is disabled, ADC1 samples pin voltage

Note 1: On devices without 14 analog inputs, all PCFGx bits are R/W by user. However, PCFGx bits are ignored on ports without a corresponding input on the device.

2: PCFGx = ANx, where x = 0 through 12 and 15.

3: The PCFGx bits have no effect if the ADC module is disabled by setting the AD1MD bit in the PMD1 register. When the bit is set, all port pins that have been multiplexed with ANx will be in Digital mode.

4: Pins shared with analog functions (i.e., ANx) are analog by default and therefore, must be set by the user to enable any digital function on that pin. Reading any port pin with the analog function enabled will return a '0', regardless of the signal input level.

5: The PCFG<15,12:11,8:6> bits are available in the dsPIC33FJ32(GP/MC)104 devices only and are reserved in all other devices.

6: The PCFG<5:4> bits are available on all devices, excluding the dsPIC33FJXX(GP/MC)101 devices, where they are reserved.

7: The PCFG<10:9> bits are available on all devices, excluding the dsPIC33FJ16(GP/MC)101/102 devices, where they are reserved.

TABLE 26-7: DC CHARACTERISTICS: IDLE CURRENT (IIDLE)

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Parameter No.	**Typical(1)**	**Max**	**Units**	**Conditions**		
Idle Current (IIDLE): Core Off, Clock On Base Current(2) – dsPIC33FJ16(GP/MC)10X Devices						
DC40d	0.4	1.0	mA	-40°C	3.3V	LPRC (32.768 kHz)(3)
DC40a	0.4	1.0	mA	+25°C		
DC40b	0.4	1.0	mA	+85°C		
DC40c	0.5	1.0	mA	+125°C		
DC41d	0.5	1.1	mA	-40°C	3.3V	1 MIPS(3)
DC41a	0.5	1.1	mA	+25°C		
DC41b	0.5	1.1	mA	+85°C		
DC41c	0.8	1.1	mA	+125°C		
DC42d	0.9	1.6	mA	-40°C	3.3V	4 MIPS(3)
DC42a	0.9	1.6	mA	+25°C		
DC42b	1.0	1.6	mA	+85°C		
DC42c	1.2	1.6	mA	+125°C		
DC43a	1.6	2.6	mA	+25°C	3.3V	10 MIPS(3)
DC43d	1.6	2.6	mA	-40°C		
DC43b	1.7	2.6	mA	+85°C		
DC43c	2	2.6	mA	+125°C		
DC44d	2.4	3.8	mA	-40°C	3.3V	16 MIPS(3)
DC44a	2.4	3.8	mA	+25°C		
DC44b	2.6	3.8	mA	+85°C		
DC44c	2.9	3.8	mA	+125°C		

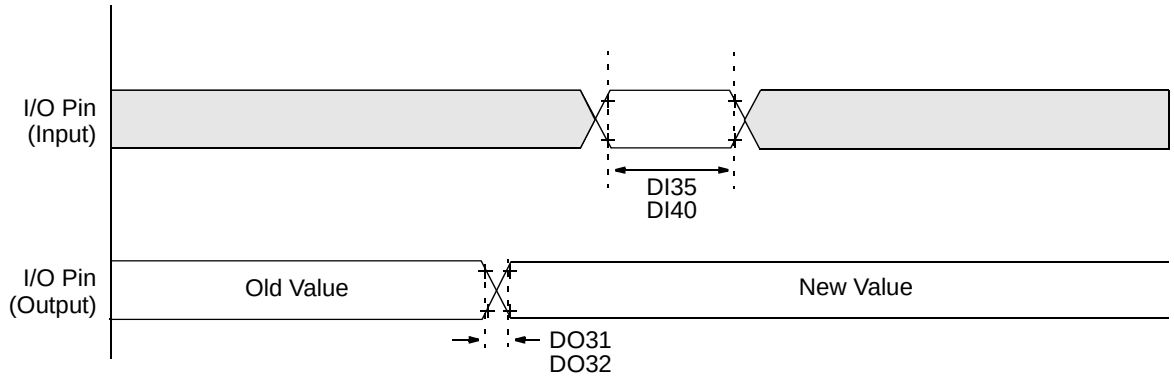
Note 1: Data in “Typical” column is at 3.3V, +25°C unless otherwise stated.

2: Base Idle current is measured as follows:

- CPU core is off, oscillator is configured in EC mode, OSC1 is driven with external square wave from rail-to-rail
- CLKO is configured as an I/O input pin in the Configuration Word
- External Secondary Oscillator (SOSC) is disabled (i.e., SOSCO and SOSCI pins are configured as digital I/O inputs)
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{\text{MCLR}}$ = VDD, WDT and FSCM are disabled
- No peripheral modules are operating; however, every peripheral is being clocked (PMDx bits are all zeroed)

3: These parameters are characterized, but not tested in manufacturing.

FIGURE 26-3: CLKO AND I/O TIMING CHARACTERISTICS



Note: Refer to Figure 26-1 for load conditions.

TABLE 26-20: I/O TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic(2)**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
DO31	TIOR	Port Output Rise Time	—	10	25	ns	
DO32	TIOF	Port Output Fall Time	—	10	25	ns	
DI35	TINP	INTx Pin High or Low Time (input)	25	—	—	ns	
DI40	TRBP	CNx High or Low Time (input)	2	—	—	TCY	

Note 1: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.

2: These parameters are characterized, but are not tested in manufacturing.

FIGURE 26-29: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (SLAVE MODE)

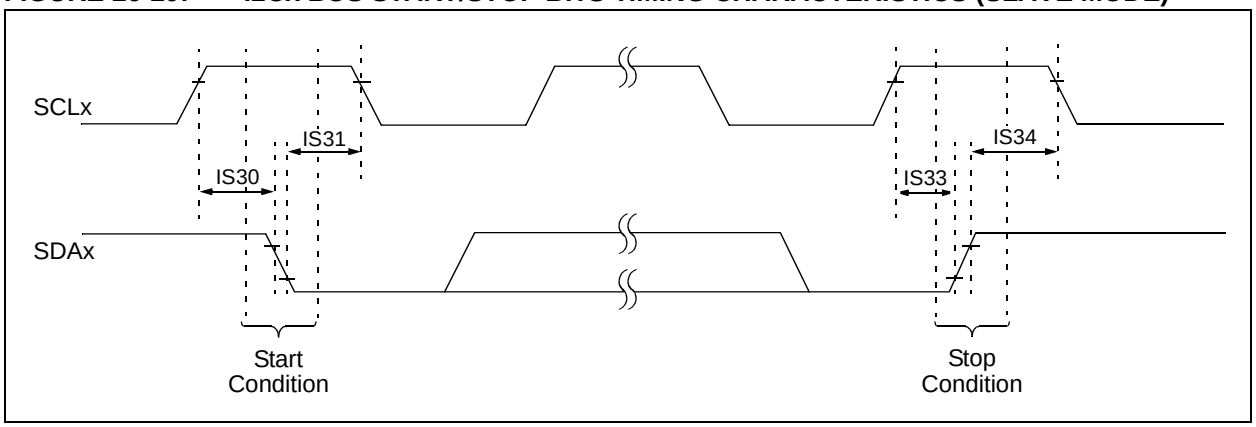
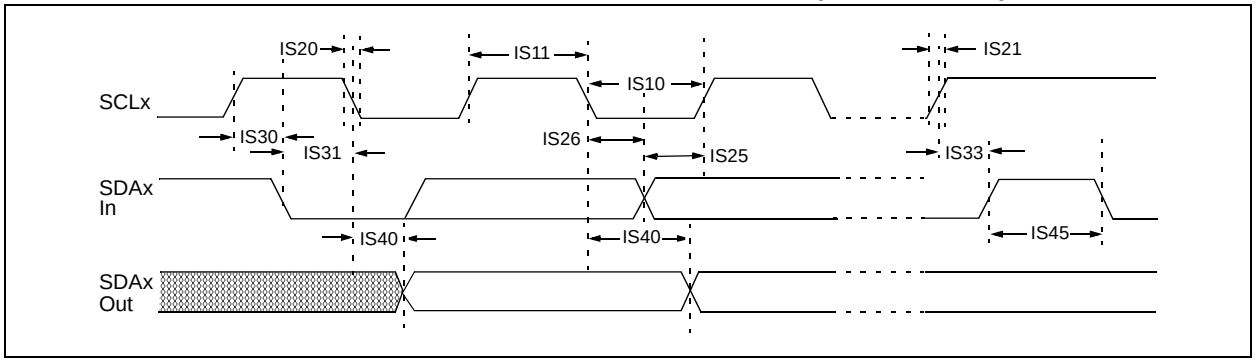
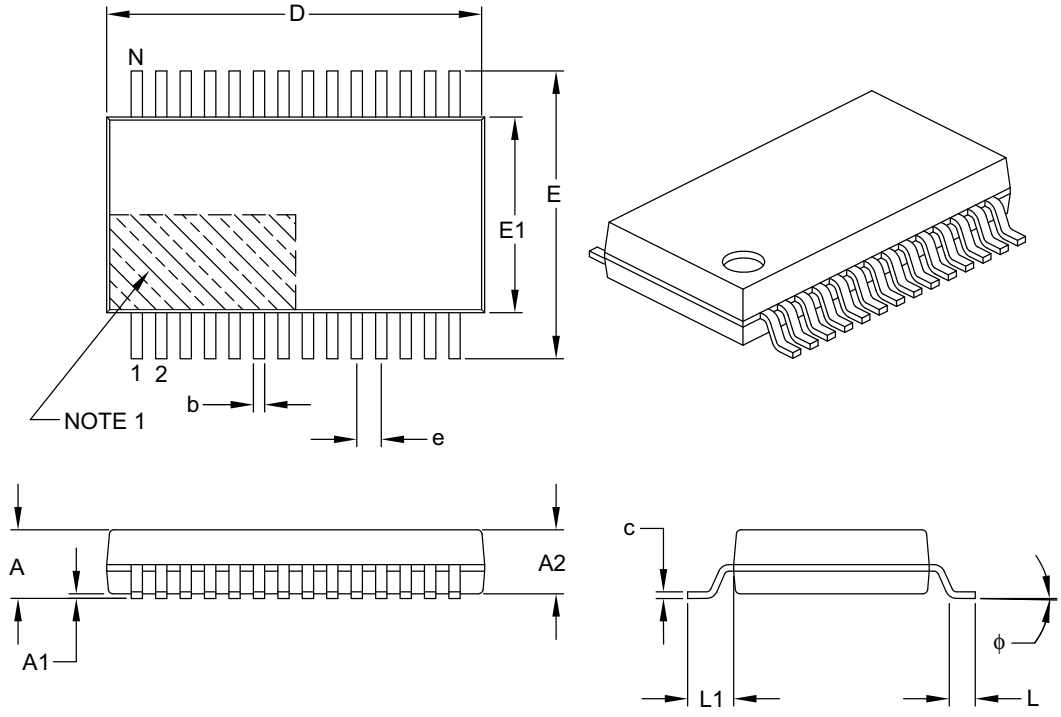


FIGURE 26-30: I2Cx BUS DATA TIMING CHARACTERISTICS (SLAVE MODE)



28-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	2.00
Molded Package Thickness	A2	1.65	1.75	1.85
Standoff	A1	0.05	–	–
Overall Width	E	7.40	7.80	8.20
Molded Package Width	E1	5.00	5.30	5.60
Overall Length	D	9.90	10.20	10.50
Foot Length	L	0.55	0.75	0.95
Footprint	L1		1.25 REF	
Lead Thickness	c	0.09	–	0.25
Foot Angle	ϕ	0°	4°	8°
Lead Width	b	0.22	–	0.38

Notes:

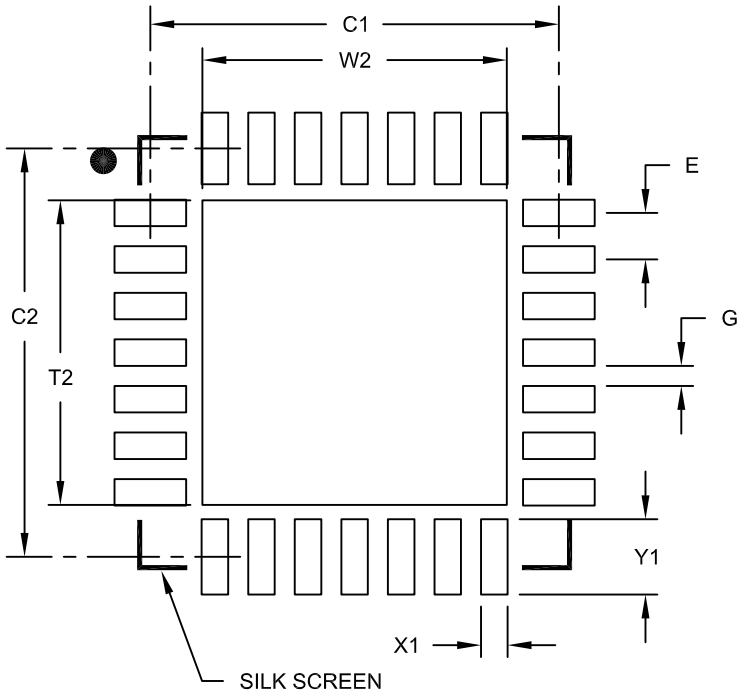
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-073B

28-Lead Plastic Quad Flat, No Lead Package (ML) – 6x6 mm Body [QFN] with 0.55 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Optional Center Pad Width	W2			4.25
Optional Center Pad Length	T2			4.25
Contact Pad Spacing	C1		5.70	
Contact Pad Spacing	C2		5.70	
Contact Pad Width (X28)	X1			0.37
Contact Pad Length (X28)	Y1			1.00
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2105A

Revision E (September 2012)

This revision includes updates to the values in **Section 26.0 "Electrical Characteristics"** and updated packaging diagrams in **Section 28.0 "Packaging Information"**. There are minor text edits throughout the document.

Revision F (January 2014)

This revision adds the High-Temperature Electrical Characteristics chapter and updated packaging diagrams in **Section 28.0 "Packaging Information"**. There are minor text edits throughout the document.