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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	16 MIPS
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	21
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj16gp102t-i-ml

FIGURE 1-1: dsPIC33FJ16(GP/MC)101/102 AND dsPIC33FJ32(GP/MC)101/102/104 BLOCK DIAGRAM

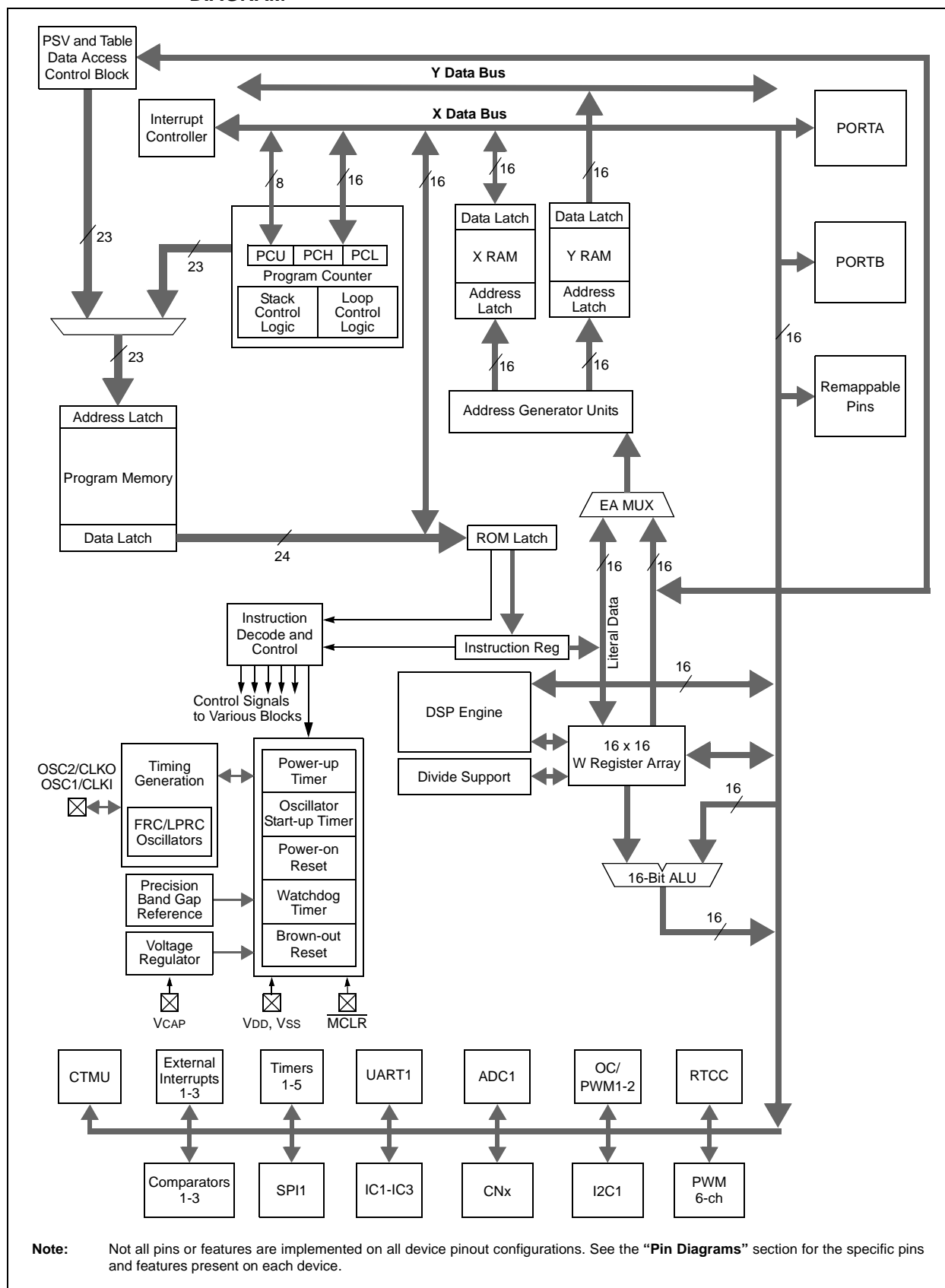


TABLE 4-17: ADC1 REGISTER MAP FOR dsPIC33FJ32(GP/MC)104 DEVICES

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
ADC1BUF0	0300	ADC1 Data Buffer 0																xxxx
ADC1BUF1	0302	ADC1 Data Buffer 1																xxxx
ADC1BUF2	0304	ADC1 Data Buffer 2																xxxx
ADC1BUF3	0306	ADC1 Data Buffer 3																xxxx
ADC1BUF4	0308	ADC1 Data Buffer 4																xxxx
ADC1BUF5	030A	ADC1 Data Buffer 5																xxxx
ADC1BUF6	030C	ADC1 Data Buffer 6																xxxx
ADC1BUF7	030E	ADC1 Data Buffer 7																xxxx
ADC1BUF8	0310	ADC1 Data Buffer 8																xxxx
ADC1BUF9	0312	ADC1 Data Buffer 9																xxxx
ADC1BUFA	0314	ADC1 Data Buffer 10																xxxx
ADC1BUFB	0316	ADC1 Data Buffer 11																xxxx
ADC1BUFC	0318	ADC1 Data Buffer 12																xxxx
ADC1BUFD	031A	ADC1 Data Buffer 13																xxxx
ADC1BUFE	031C	ADC1 Data Buffer 14																xxxx
ADC1BUFF	031E	ADC1 Data Buffer 15																xxxx
AD1CON1	0320	ADON	—	ADSIDL	—	—	—	FORM1	FORM0	SSRC2	SSRC1	SSRC0	—	SIMSAM	ASAM	SAMP	DONE	0000
AD1CON2	0322	VCFG2	VCFG1	VCFG0	—	—	CSCNA	CHPS1	CHPS0	BUFS	—	SMPI3	SMPI2	SMPI1	SMPI0	BUFM	ALTS	0000
AD1CON3	0324	ADRC	—	—	SAMC4	SAMC3	SAMC2	SAMC1	SAMC0	ADCS7	ADCS6	ADCS5	ADCS4	ADCS3	ADCS2	ADCS1	ADCS0	0000
AD1CHS123	0326	—	—	—	—	—	CH123NB1	CH123NB0	CH123SB	—	—	—	—	—	CH123NA1	CH123NA0	CH123SA	0000
AD1CHS0	0328	CH0NB	—	—	CH0SB4	CH0SB3	CH0SB2	CH0SB1	CH0SB0	CH0NA	—	—	CH0SA4	CH0SA3	CH0SA2	CH0SA1	CH0SA0	0000
AD1PCFGL	032C	PCFG15	—	—	PCFG<12:0> ⁽¹⁾													0000
AD1CSSL	0330	CSS15	—	—	CSS12:0> ⁽¹⁾													0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: The PCFG<10:9> and CSS<10:9> bits are available in dsPIC33FJ32(GP/MC)104 devices only.

TABLE 4-33: PORTB REGISTER MAP FOR dsPIC33FJ32GP101 DEVICES

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISB	02C8	TRISB<15:14>		—	—	—	—	TRISB<9:7>		—	—	TRISB4		—	—	TRISB<1:0>		C393
PORTB	02CA	RB<15:14>		—	—	—	—	RB<9:7>		—	—	RB4		—	—	RB<1:0>		xxxx
LATB	02CC	LATB<15:14>		—	—	—	—	LATB<9:7>		—	—	LATB4		—	—	LATB<1:0>		xxxx
ODCB	02CE	ODCB<15:14>		—	—	—	—	ODCB<9:7>		—	—	—		—	—	—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-34: PORTB REGISTER MAP FOR dsPIC33FJ32MC101 DEVICES

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISB	02C8	TRISB<15:12>				—	—	TRISB<9:7>			—	—	TRISB4	—	—	TRISB<1:0>		F393
PORTB	02CA	RB<15:12>				—	—	RB<9:7>			—	—	RB4	—	—	RB<1:0>		xxxx
LATB	02CC	LATB<15:12>				—	—	LATB<9:7>			—	—	LATB4	—	—	LATB<1:0>		xxxx
ODCB	02CE	ODCB<15:12>				—	—	ODCB<9:7>			—	—	—	—	—	—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-35: PORTB REGISTER MAP FOR dsPIC33FJ32(GP/MC)102 AND dsPIC33FJ32(GP/MC)104 DEVICES

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISB	02C8	TRISB<15:0>																FFFF
PORTB	02CA	RB<15:0>																xxxx
LATB	02CC	LATB<15:0>																xxxx
ODCB	02CE	ODCB<15:5>											—	—	—	—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-36: PORTC REGISTER MAP FOR dsPIC33FJ32(GP/MC)104 DEVICES

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISC	02D0	—	—	—	—	—	—	TRISC<9:0>										FFFF
PORTC	02D2	—	—	—	—	—	—	RC<9:0>										xxxx
LATC	02D4	—	—	—	—	—	—	LATC<9:0>										xxxx
ODCC	02D6	—	—	—	—	—	—	ODCC<9:6>				—	—	—	—	—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

4.6.2 DATA ACCESS FROM PROGRAM MEMORY USING TABLE INSTRUCTIONS

The TBLRDL and TBLWTL instructions offer a direct method of reading or writing the lower word of any address within the program space without going through data space. The TBLRDH and TBLWTH instructions are the only method to read or write the upper 8 bits of a program space word as data.

The PC is incremented by two for each successive 24-bit program word. This allows program memory addresses to directly map to data space addresses. Program memory can thus be regarded as two 16-bit-wide word address spaces, residing side by side, each with the same address range. TBLRDL and TBLWTL access the space that contains the least significant data word. TBLRDH and TBLWTH access the space that contains the upper data byte.

Two table instructions are provided to move byte or word-sized (16-bit) data to and from program space. Both function as either byte or word operations.

- TBLRDL (Table Read Low):
 - In Word mode, this instruction maps the lower word of the program space location ($P<15:0>$) to a data address ($D<15:0>$).
 - In Byte mode, either the upper or lower byte of the lower program word is mapped to the lower byte of a data address. The upper byte is selected when Byte Select is '1'; the lower byte is selected when it is '0'.

- TBLRDH (Table Read High):
 - In Word mode, this instruction maps the entire upper word of a program address ($P<23:16>$) to a data address. Note that $D<15:8>$, the 'phantom byte', will always be '0'.
 - In Byte mode, this instruction maps the upper or lower byte of the program word to $D<7:0>$ of the data address, in the TBLRDL instruction. The data is always '0' when the upper 'phantom' byte is selected (Byte Select = 1).

In a similar fashion, two table instructions, TBLWTH and TBLWTL, are used to write individual bytes or words to a program space address. The details of their operation are explained in **Section 5.0 "Flash Program Memory"**.

For all table operations, the area of program memory space to be accessed is determined by the Table Page register (TBLPAG). TBLPAG covers the entire program memory space of the device, including user and configuration spaces. When $TBLPAG<7> = 0$, the table page is located in the user memory space. When $TBLPAG<7> = 1$, the page is located in configuration space.

FIGURE 4-10: ACCESSING PROGRAM MEMORY WITH TABLE INSTRUCTIONS

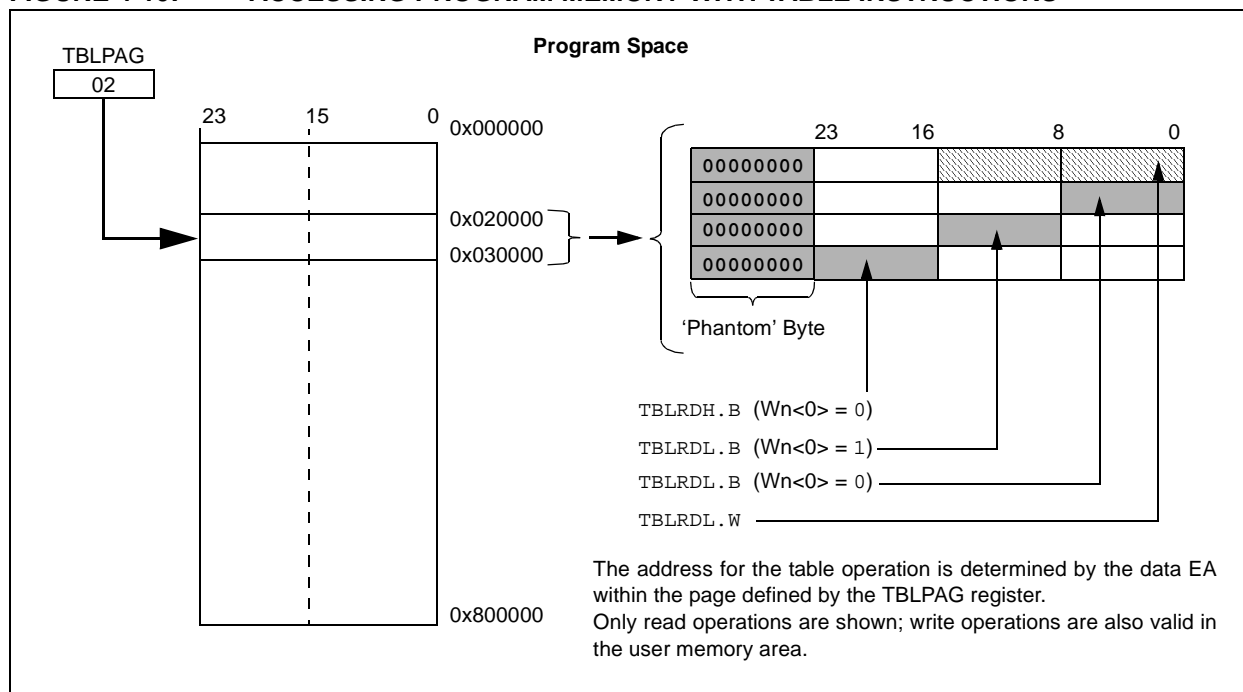


FIGURE 6-2: SYSTEM RESET TIMING

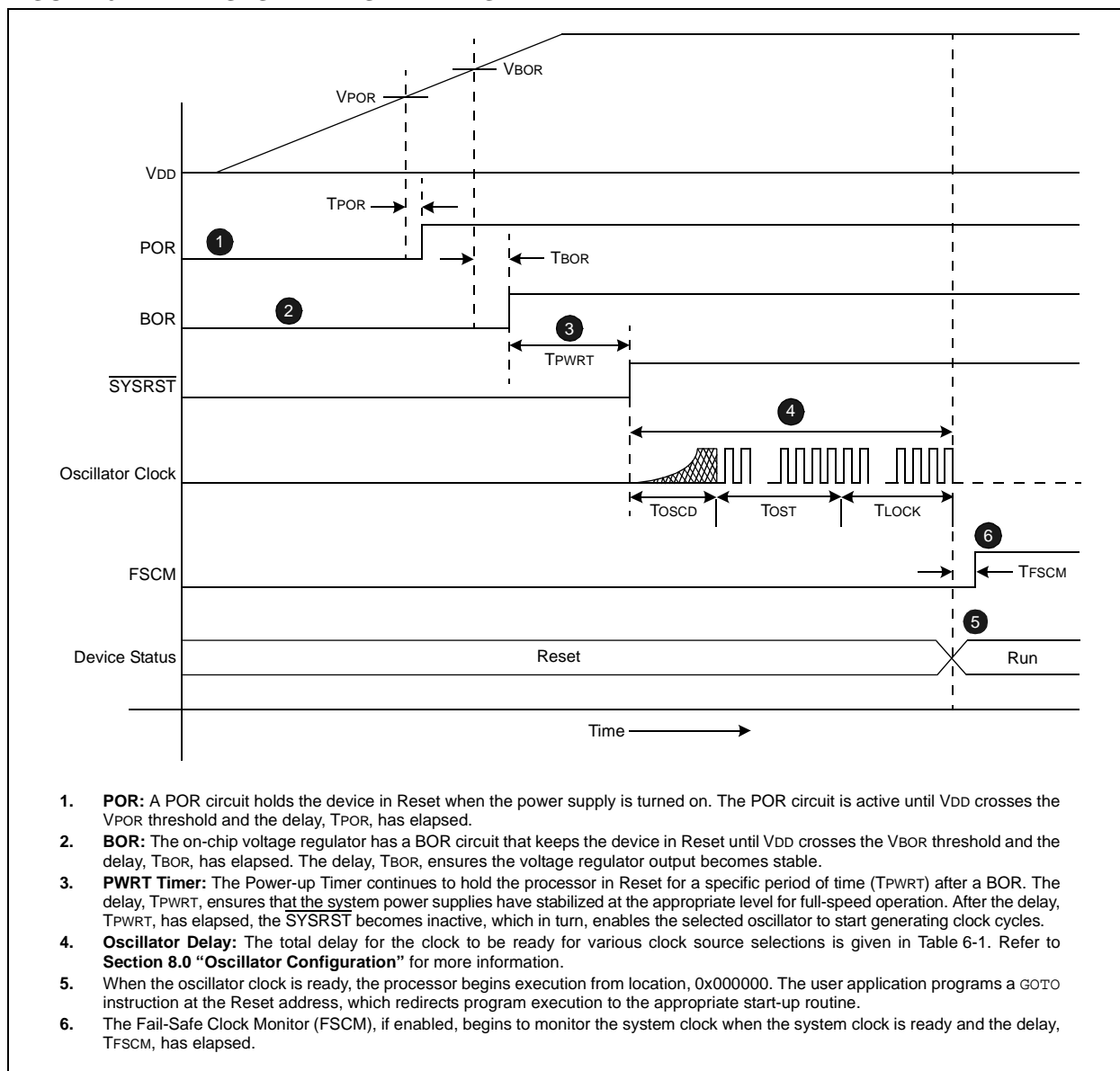


TABLE 6-2: OSCILLATOR PARAMETERS

Symbol	Parameter	Value
VPOR	POR Threshold	1.8V nominal
TPOR	POR Extension Time	30 μ s maximum
VBOR	BOR Threshold	2.5V nominal
TBOR	BOR Extension Time	100 μ s maximum
TPWRT	Power-up Time Delay	64 ms nominal
TFSCM	Fail-Safe Clock Monitor Delay	900 μ s maximum

Note: When the device exits the Reset condition (begins normal operation), the device operating parameters (voltage, frequency, temperature, etc.) must be within their operating ranges; otherwise, the device may not function correctly. The user application must ensure that the delay between the time power is first applied, and the time SYSRST becomes inactive, is long enough to get all operating parameters within specification.

dsPIC33FJ16(GP/MC)101/102 AND dsPIC33FJ32(GP/MC)101/102/104

REGISTER 8-3: OSCTUN: FRC OSCILLATOR TUNING REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15						bit 8	

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	TUN<5:0>					
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-6

Unimplemented: Read as '0'

bit 5-0

TUN<5:0>: FRC Oscillator Tuning bits

011111 = Maximum frequency deviation of 1.453% (7.477 MHz)

011110 = Center frequency + 1.406% (7.474 MHz)

•

•

•

000001 = Center frequency + 0.047% (7.373 MHz)

000000 = Center frequency (7.37 MHz nominal)

111111 = Center frequency – 0.047% (7.367 MHz)

•

•

•

100001 = Center frequency – 1.453% (7.263 MHz)

100000 = Minimum frequency deviation of -1.5% (7.259 MHz)

dsPIC33FJ16(GP/MC)101/102 AND dsPIC33FJ32(GP/MC)101/102/104

REGISTER 9-1: PMD1: PERIPHERAL MODULE DISABLE CONTROL REGISTER 1 (CONTINUED)

- bit 3 **SPI1MD:** SPI1 Module Disable bit
1 = SPI1 module is disabled
0 = SPI1 module is enabled
- bit 2-1 **Unimplemented:** Read as '0'
- bit 0 **AD1MD:** ADC1 Module Disable bit⁽²⁾
1 = ADC1 module is disabled
0 = ADC1 module is enabled

Note 1: These bits are available in dsPIC33FJ32(GP/MC)10X devices only.

2: PCFGx bits have no effect if the ADC module is disabled by setting this bit. When the bit is set, all port pins that have been multiplexed with ANx will be in Digital mode.

REGISTER 9-2: PMD2: PERIPHERAL MODULE DISABLE CONTROL REGISTER 2

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	IC3MD	IC2MD	IC1MD
bit 15					bit 8		

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	OC2MD	OC1MD
bit 7						bit 0	

Legend:

R = Readable bit
-n = Value at POR

W = Writable bit
'1' = Bit is set

U = Unimplemented bit, read as '0'
'0' = Bit is cleared
x = Bit is unknown

- bit 15-11 **Unimplemented:** Read as '0'
- bit 10 **IC3MD:** Input Capture 3 Module Disable bit
1 = Input Capture 3 module is disabled
0 = Input Capture 3 module is enabled
- bit 9 **IC2MD:** Input Capture 2 Module Disable bit
1 = Input Capture 2 module is disabled
0 = Input Capture 2 module is enabled
- bit 8 **IC1MD:** Input Capture 1 Module Disable bit
1 = Input Capture 1 module is disabled
0 = Input Capture 1 module is enabled
- bit 7-2 **Unimplemented:** Read as '0'
- bit 1 **OC2MD:** Output Compare 2 Module Disable bit
1 = Output Compare 2 module is disabled
0 = Output Compare 2 module is enabled
- bit 0 **OC1MD:** Output Compare 1 Module Disable bit
1 = Output Compare 1 module is disabled
0 = Output Compare 1 module is enabled

10.4 Peripheral Pin Select (PPS)

Peripheral Pin Select configuration enables peripheral set selection and placement on a wide range of I/O pins. By increasing the pinout options available on a particular device, programmers can better tailor the microcontroller to their entire application, rather than trimming the application to fit the device.

The Peripheral Pin Select configuration feature operates over a fixed subset of digital I/O pins. Programmers can independently map the input and/or output of most digital peripherals to any one of these I/O pins. Peripheral Pin Select is performed in software and generally does not require the device to be reprogrammed. Hardware safeguards are included that prevent accidental or spurious changes to the peripheral mapping, once it has been established.

10.4.1 AVAILABLE PINS

The Peripheral Pin Select feature is used with a range of up to 16 pins. The number of available pins depends on the particular device and its pin count. Pins that support the Peripheral Pin Select feature include the designation “RPn” in their full pin designation, where “RP” designates a remappable peripheral and “n” is the remappable pin number.

10.4.2 CONTROLLING PERIPHERAL PIN SELECT

Peripheral Pin Select features are controlled through two sets of Special Function Registers: one to map peripheral inputs and one to map outputs. Because they are separately controlled, a particular peripheral's input and output (if the peripheral has both) can be placed on any selectable function pin without constraint.

The association of a peripheral to a peripheral selectable pin is handled in two different ways, depending on whether an input or output is being mapped.

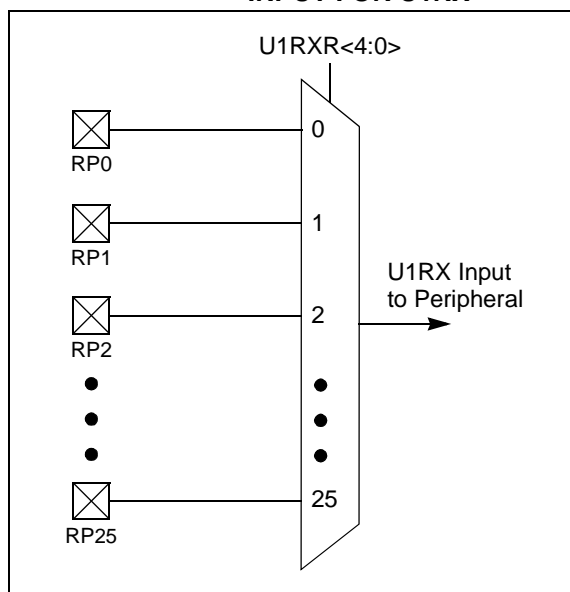
10.4.2.1 Input Mapping

The inputs of the Peripheral Pin Select options are mapped on the basis of the peripheral. A control register associated with a peripheral dictates the pin it will be mapped to. The RPNR_x registers are used to configure peripheral input mapping (see Register 10-1 through Register 10-10). Each register contains sets of 5-bit fields, with each set associated with one of the remappable peripherals. Programming a given peripheral's bit field with an appropriate 5-bit value maps the RP_n pin with that value to that peripheral. For any given device, the valid range of values for any bit field corresponds to the maximum number of Peripheral Pin Selections supported by the device.

Figure 10-2 Illustrates remappable pin selection for U1RX input.

Note: For input mapping only, the Peripheral Pin Select (PPS) functionality does not have priority over the TRIS_x settings. Therefore, when configuring the RP_x pin for input, the corresponding bit in the TRIS_x register must also be configured for input (i.e., set to '1').

FIGURE 10-2: REMAPPABLE MUX INPUT FOR U1RX



REGISTER 18-2: UxSTA: UARTx STATUS AND CONTROL REGISTER

R/W-0	R/W-0	R/W-0	U-0	R/W-0, HC	R/W-0	R-0	R-1
UTXISEL1	UTXINV	UTXISEL0	—	UTXBRK	UTXEN ⁽¹⁾	UTXBF	TRMT
bit 15							bit 8

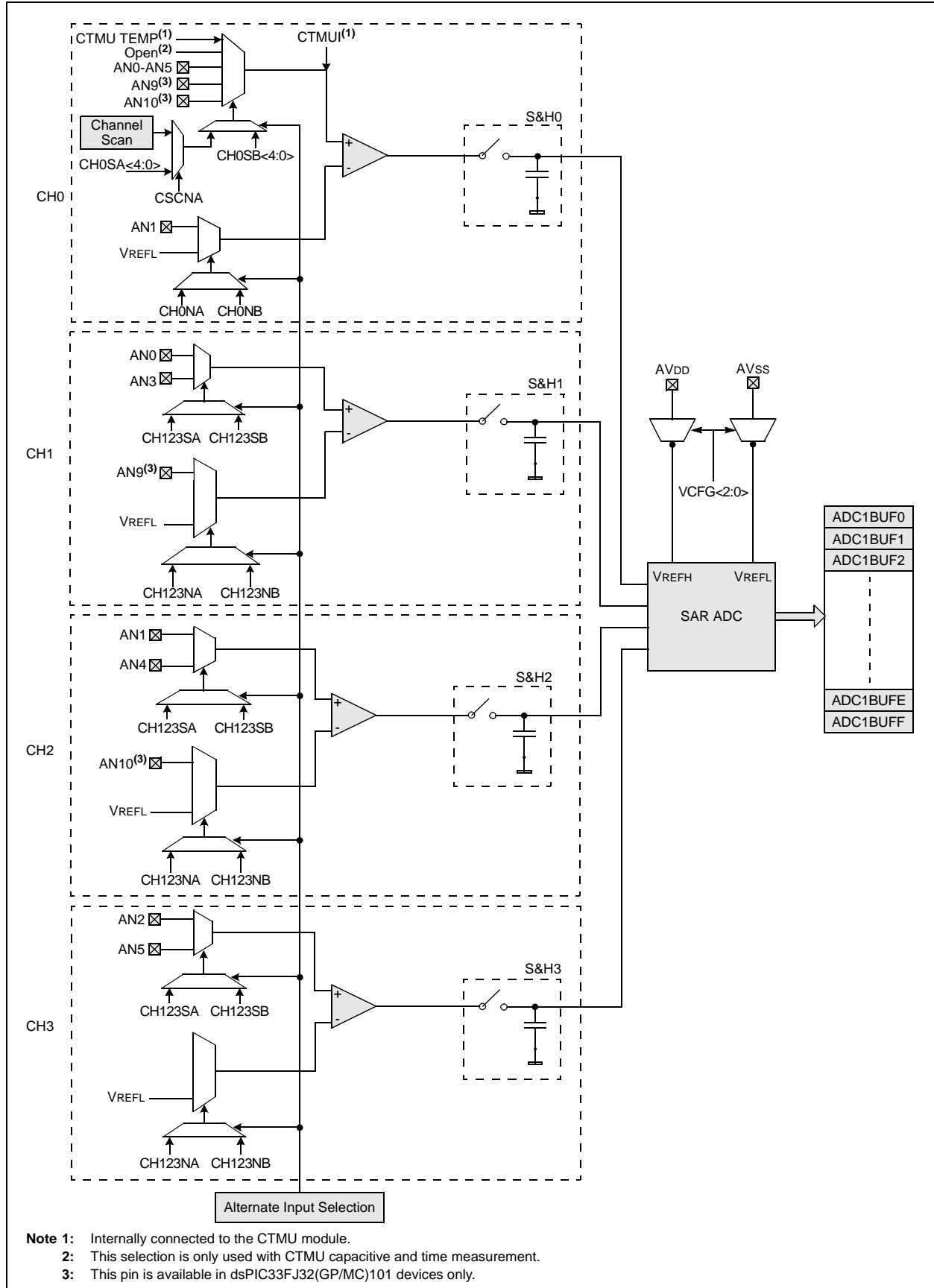
R/W-0	R/W-0	R/W-0	R-1	R-0	R-0	R/C-0	R-0
URXISEL1	URXISEL0	ADDEN	RIDL	PERR	FERR	OERR	URXDA
bit 7							bit 0

Legend:	C = Clearable bit	HC = Hardware Clearable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

- bit 15,13 **UTXISEL<1:0>:** UARTx Transmission Interrupt Mode Selection bits
- 11 = Reserved; do not use
 - 10 = Interrupt when a character is transferred to the Transmit Shift Register (TSR) and as a result, the transmit buffer becomes empty
 - 01 = Interrupt when the last character is shifted out of the Transmit Shift Register; all transmit operations are completed
 - 00 = Interrupt when a character is transferred to the Transmit Shift Register (this implies there is at least one character open in the transmit buffer)
- bit 14 **UTXINV:** UARTx Transmit Polarity Inversion bit
- If IREN = 0:
- 1 = UxTX Idle state is '0'
 - 0 = UxTX Idle state is '1'
- If IREN = 1:
- 1 = IrDA encoded, UxTX Idle state is '1'
 - 0 = IrDA encoded, UxTX Idle state is '0'
- bit 12 **Unimplemented:** Read as '0'
- bit 11 **UTXBRK:** UARTx Transmit Break bit
- 1 = Sends Sync Break on next transmission – Start bit, followed by twelve '0' bits, followed by Stop bit; cleared by hardware upon completion
 - 0 = Sync Break transmission is disabled or completed
- bit 10 **UTXEN:** UARTx Transmit Enable bit⁽¹⁾
- 1 = Transmit is enabled, UxTX pin is controlled by UARTx
 - 0 = Transmit is disabled, any pending transmission is aborted and the buffer is reset; UxTX pin is controlled by port
- bit 9 **UTXBF:** UARTx Transmit Buffer Full Status bit (read-only)
- 1 = Transmit buffer is full
 - 0 = Transmit buffer is not full, at least one more character can be written
- bit 8 **TRMT:** Transmit Shift Register Empty bit (read-only)
- 1 = Transmit Shift Register is empty and transmit buffer is empty (the last transmission has completed)
 - 0 = Transmit Shift Register is not empty, a transmission is in progress or queued
- bit 7-6 **URXISEL<1:0>:** UARTx Receive Interrupt Mode Selection bits
- 11 = Interrupt is set on UxRSR transfer, making the receive buffer full (i.e., has 4 data characters)
 - 10 = Interrupt is set on UxRSR transfer, making the receive buffer 3/4 full (i.e., has 3 data characters)
 - 0x = Interrupt is set when any character is received and transferred from the UxRSR to the receive buffer; receive buffer has one or more characters

Note 1: Refer to “UART” (DS70188) in the “dsPIC33/PIC24 Family Reference Manual” for information on enabling the UART module for transmit operation.

FIGURE 19-2: ADC1 BLOCK DIAGRAM FOR dsPIC33FJXX(GP/MC)102 DEVICES



REGISTER 19-3: AD1CON3: ADC1 CONTROL REGISTER 3

R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADRC	—	—	SAMC4 ⁽¹⁾	SAMC3 ⁽¹⁾	SAMC2 ⁽¹⁾	SAMC1 ⁽¹⁾	SAMC0 ⁽¹⁾
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADCS7 ⁽²⁾	ADCS6 ⁽²⁾	ADCS5 ⁽²⁾	ADCS4 ⁽²⁾	ADCS3 ⁽²⁾	ADCS2 ⁽²⁾	ADCS1 ⁽²⁾	ADCS0 ⁽²⁾
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **ADRC:** ADC1 Conversion Clock Source bit

1 = ADC1 internal RC clock

0 = Clock derived from system clock

bit 14-13 **Unimplemented:** Read as '0'

bit 12-8 **SAMC<4:0>:** Auto-Sample Time bits⁽¹⁾

11111 = 31 TAD

•

•

•

00001 = 1 TAD

00000 = 0 TAD

bit 7-0 **ADCS<7:0>:** ADC1 Conversion Clock Select bits⁽²⁾

11111111 = Reserved

•

•

•

•

01000000 = Reserved

00111111 = T_{CY} • (ADCS<7:0> + 1) = 64 • T_{CY} = TAD

•

•

•

00000010 = T_{CY} • (ADCS<7:0> + 1) = 3 • T_{CY} = TAD

00000001 = T_{CY} • (ADCS<7:0> + 1) = 2 • T_{CY} = TAD

00000000 = T_{CY} • (ADCS<7:0> + 1) = 1 • T_{CY} = TAD

Note 1: This bit is only used if SSRC<2:0> (AD1CON1<7:5>) = 1.

2: This bit is not used if ADRC (AD1CON3<15>) = 1.

20.1 Comparator Control Registers

REGISTER 20-1: CMSTAT: COMPARATOR STATUS REGISTER

R/W-0	U-0	U-0	U-0	U-0	R-0	R-0	R-0
CMSIDL	—	—	—	—	C3EVT	C2EVT	C1EVT
bit 15				bit 8			

U-0	U-0	U-0	U-0	U-0	R-0	R-0	R-0
—	—	—	—	—	C3OUT	C2OUT	C1OUT
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15 **CMSIDL:** Comparator Stop in Idle Mode bit
 1 = Discontinues operation of all comparators when device enters Idle mode
 0 = Continues operation of all comparators in Idle mode
- bit 14-11 **Unimplemented:** Read as '0'
- bit 10 **C3EVT:** Comparator 3 Event Status bit
 1 = Comparator event occurred
 0 = Comparator event did not occur
- bit 9 **C2EVT:** Comparator 2 Event Status bit
 1 = Comparator event occurred
 0 = Comparator event did not occur
- bit 8 **C1EVT:** Comparator 1 Event Status bit
 1 = Comparator event occurred
 0 = Comparator event did not occur
- bit 7-3 **Unimplemented:** Read as '0'
- bit 2 **C3OUT:** Comparator 3 Output Status bit
When CPOL = 0:
 1 = $V_{IN+} > V_{IN-}$
 0 = $V_{IN+} < V_{IN-}$
When CPOL = 1:
 1 = $V_{IN+} < V_{IN-}$
 0 = $V_{IN+} > V_{IN-}$
- bit 1 **C2OUT:** Comparator 2 Output Status bit
When CPOL = 0:
 1 = $V_{IN+} > V_{IN-}$
 0 = $V_{IN+} < V_{IN-}$
When CPOL = 1:
 1 = $V_{IN+} < V_{IN-}$
 0 = $V_{IN+} > V_{IN-}$
- bit 0 **C1OUT:** Comparator 1 Output Status bit
When CPOL = 0:
 1 = $V_{IN+} > V_{IN-}$
 0 = $V_{IN+} < V_{IN-}$
When CPOL = 1:
 1 = $V_{IN+} < V_{IN-}$
 0 = $V_{IN+} > V_{IN-}$

REGISTER 20-2: CMxCON: COMPARATOR x CONTROL REGISTER

R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0
CON	COE	CPOL	—	—	—	CEVT	COUT
bit 15						bit 8	

R/W-0	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0
EVPOL1	EVPOL0	—	CREF	—	—	CCH1	CCH0
bit 7						bit 0	

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15 **CON:** Comparator x Enable bit
 1 = Comparator x is enabled
 0 = Comparator x is disabled
- bit 14 **COE:** Comparator x Output Enable bit
 1 = Comparator output is present on the CxOUT pin
 0 = Comparator output is internal only
- bit 13 **CPOL:** Comparator x Output Polarity Select bit
 1 = Comparator x output is inverted
 0 = Comparator x output is not inverted
- bit 12-10 **Unimplemented:** Read as '0'
- bit 9 **CEVT:** Comparator x Event bit
 1 = Comparator x event according to EVPOL<1:0> settings occurred; disables future triggers and interrupts until the bit is cleared
 0 = Comparator x event did not occur
- bit 8 **COUT:** Comparator x Output bit
 When CPOL = 0 (non-inverted polarity):
 1 = $V_{IN+} > V_{IN-}$
 0 = $V_{IN+} < V_{IN-}$
 When CPOL = 1 (inverted polarity):
 1 = $V_{IN+} < V_{IN-}$
 0 = $V_{IN+} > V_{IN-}$
- bit 7-6 **EVPOL<1:0>:** Trigger/Event/Interrupt Polarity Select bits
 11 = Trigger/event/interrupt is generated on any change of the comparator output (while CEVT = 0)
 10 = Trigger/event/interrupt is generated only on high-to-low transition of the polarity selected comparator output (while CEVT = 0)
 If CPOL = 1 (inverted polarity):
 Low-to-high transition of the comparator output.
 If CPOL = 0 (non-inverted polarity):
 High-to-low transition of the comparator output.
 01 = Trigger/event/interrupt is generated only on low-to-high transition of the polarity selected comparator output (while CEVT = 0)
 If CPOL = 1 (inverted polarity):
 High-to-low transition of the comparator output.
 If CPOL = 0 (non-inverted polarity):
 Low-to-high transition of the comparator output.
 00 = Trigger/event/interrupt generation is disabled
- bit 5 **Unimplemented:** Read as '0'

21.2 RTCC Control Registers

REGISTER 21-1: RCFGAL: RTCC CALIBRATION AND CONFIGURATION REGISTER⁽¹⁾

R/W-0	U-0	R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-0
RTCEN ⁽²⁾	—	RTCWREN	RTCSYNC	HALFSEC ⁽³⁾	RTCOE	RTCPTR1	RTCPTR0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CAL7	CAL6	CAL5	CAL4	CAL3	CAL2	CAL1	CAL0
bit 7							bit 0

Legend:

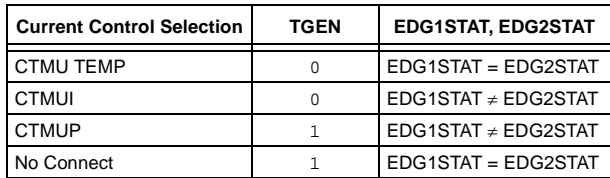
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15 **RTCEN:** RTCC Enable bit⁽²⁾
 1 = RTCC module is enabled
 0 = RTCC module is disabled
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **RTCWREN:** RTCC Value Registers Write Enable bit
 1 = RTCVALH and RTCVALL registers can be written to by the user
 0 = RTCVALH and RTCVALL registers are locked out from being written to by the user
- bit 12 **RTCSYNC:** RTCC Value Registers Read Synchronization bit
 1 = RTCVALH, RTCVALL and ALCFGRPT registers can change while reading, due to a rollover ripple, resulting in an invalid data read. If the register is read twice and the results are the same data, the data can be assumed to be valid.
 0 = RTCVALH, RTCVALL or ALCFGRPT registers can be read without concern over a rollover ripple
- bit 11 **HALFSEC:** Half-Second Status bit⁽³⁾
 1 = Second half period of a second
 0 = First half period of a second
- bit 10 **RTCOE:** RTCC Output Enable bit
 1 = RTCC output is enabled
 0 = RTCC output is disabled
- bit 9-8 **RTCPTR<1:0>:** RTCC Value Register Window Pointer bits
 Points to the corresponding RTCC Value registers when reading RTCVALH and RTCVALL registers; the RTCPTR<1:0> value decrements on every read or write of RTCVALH until it reaches '00'.
 RTCVAL<15:8>:
 00 = MINUTES
 01 = WEEKDAY
 10 = MONTH
 11 = Reserved
 RTCVAL<7:0>:
 00 = SECONDS
 01 = HOURS
 10 = DAY
 11 = YEAR

Note 1: The RCFGAL register is only affected by a POR.

2: A write to the RTCEN bit is only allowed when RTCWREN = 1.

3: This bit is read-only; it is cleared to '0' on a write to the lower half of the MINSEC register.



dsPIC33FJ16(GP/MC)101/102 AND dsPIC33FJ32(GP/MC)101/102/104

TABLE 26-6: DC CHARACTERISTICS: OPERATING CURRENT (IDD)

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended		
Parameter No.	Typical ⁽¹⁾	Max	Units	Conditions	
Operating Current (IDD) ⁽²⁾ – dsPIC33FJ16(GP/MC)10X Devices					
DC20d	0.7	1.7	mA	-40°C	3.3V LPRC (32.768 kHz) ⁽³⁾
DC20a	0.7	1.7	mA	+25°C	
DC20b	1.0	1.7	mA	+85°C	
DC20c	1.3	1.7	mA	+125°C	
DC21d	1.9	2.6	mA	-40°C	3.3V 1 MIPS ⁽³⁾
DC21a	1.9	2.6	mA	+25°C	
DC21b	1.9	2.6	mA	+85°C	
DC21c	2.0	2.6	mA	+125°C	
DC22d	6.5	8.5	mA	-40°C	3.3V 4 MIPS ⁽³⁾
DC22a	6.5	8.5	mA	+25°C	
DC22b	6.5	8.5	mA	+85°C	
DC22c	6.5	8.5	mA	+125°C	
DC23d	12.2	16	mA	-40°C	3.3V 10 MIPS ⁽³⁾
DC23a	12.2	16	mA	+25°C	
DC23b	12.2	16	mA	+85°C	
DC23c	12.2	16	mA	+125°C	
DC24d	16	21	mA	-40°C	3.3V 16 MIPS
DC24a	16	21	mA	+25°C	
DC24b	16	21	mA	+85°C	
DC24c	16	21	mA	+125°C	

Note 1: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

2: IDD is primarily a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. The test conditions for all IDD measurements are as follows:

- Oscillator is configured in EC mode, OSC1 is driven with external square wave from rail-to-rail
- CLKO is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as inputs and pulled to VSS
- MCLR = VDD, WDT and FSCM are disabled
- CPU, SRAM, program memory and data memory are operational
- No peripheral modules are operating; however, every peripheral is being clocked (PMDx bits are all zeroed)
- CPU executing `while(1)` statement

3: These parameters are characterized, but not tested in manufacturing.

dsPIC33FJ16(GP/MC)101/102 AND dsPIC33FJ32(GP/MC)101/102/104

TABLE 26-7: DC CHARACTERISTICS: IDLE CURRENT (I_{IDLE})

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended		
Parameter No.	Typical ⁽¹⁾	Max	Units	Conditions	
Idle Current (IDLE): Core Off, Clock On Base Current ⁽²⁾ – dsPIC33FJ16(GP/MC)10X Devices					
DC40d	0.4	1.0	mA	-40°C	3.3V LPRC (32.768 kHz) ⁽³⁾
DC40a	0.4	1.0	mA	+25°C	
DC40b	0.4	1.0	mA	+85°C	
DC40c	0.5	1.0	mA	+125°C	
DC41d	0.5	1.1	mA	-40°C	3.3V 1 MIPS ⁽³⁾
DC41a	0.5	1.1	mA	+25°C	
DC41b	0.5	1.1	mA	+85°C	
DC41c	0.8	1.1	mA	+125°C	
DC42d	0.9	1.6	mA	-40°C	3.3V 4 MIPS ⁽³⁾
DC42a	0.9	1.6	mA	+25°C	
DC42b	1.0	1.6	mA	+85°C	
DC42c	1.2	1.6	mA	+125°C	
DC43a	1.6	2.6	mA	+25°C	3.3V 10 MIPS ⁽³⁾
DC43d	1.6	2.6	mA	-40°C	
DC43b	1.7	2.6	mA	+85°C	
DC43c	2	2.6	mA	+125°C	
DC44d	2.4	3.8	mA	-40°C	3.3V 16 MIPS ⁽³⁾
DC44a	2.4	3.8	mA	+25°C	
DC44b	2.6	3.8	mA	+85°C	
DC44c	2.9	3.8	mA	+125°C	

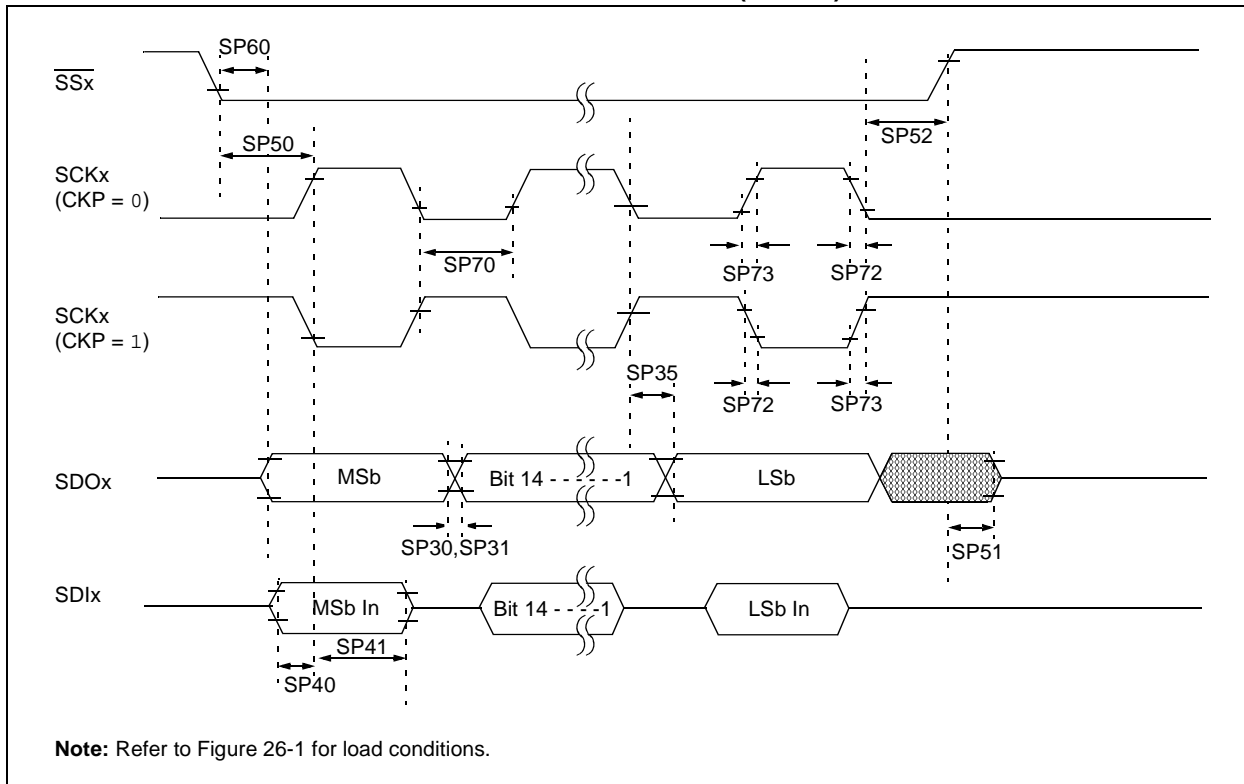
Note 1: Data in “Typical” column is at 3.3V, +25°C unless otherwise stated.

2: Base Idle current is measured as follows:

- CPU core is off, oscillator is configured in EC mode, OSC1 is driven with external square wave from rail-to-rail
- CLKO is configured as an I/O input pin in the Configuration Word
- External Secondary Oscillator (SOSC) is disabled (i.e., SOSCO and SOSCI pins are configured as digital I/O inputs)
- All I/O pins are configured as inputs and pulled to V_{SS}
- MCLR = V_{DD}, WDT and FSCM are disabled
- No peripheral modules are operating; however, every peripheral is being clocked (PMDx bits are all zeroed)

3: These parameters are characterized, but not tested in manufacturing.

FIGURE 26-15: SPIx SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0) TIMING CHARACTERISTICS FOR dsPIC33FJ16(GP/MC)10X



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