Microchip Technology - DSPIC33FJ16MC101T-I/SS Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	16 MIPs
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, Motor Control PWM, POR, PWM, WDT
Number of I/O	15
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj16mc101t-i-ss

TABLE 2: dsPIC33FJ32(GP/MC)101/102/104 DEVICE FEATURES

Device	Pins	Program Flash (Kbyte)	RAM (Kbytes)	Remappable Peripherals							Motor Control PWM	PWM Faults	10-Bit, 1.1 Msps ADC	RTCC	I^2C™	Comparators	CTMU	I/O Pins	Packages
				Remappable Pins	16-bit Timer(1,2)	Input Capture	Output Compare	UART	External Interrupts(3)	SPI									
dsPIC33FJ32GP101	18	32	2	8	5	3	2	1	3	1	—	—	1 ADC, 6-ch	Y	1	3	Y	13	PDIP, SOIC
	20	32	2	8	5	3	2	1	3	1	—	—	1 ADC, 6-ch	Y	1	3	Y	15	SSOP
dsPIC33FJ32GP102	28	32	2	16	5	3	2	1	3	1	—	—	1 ADC, 8-ch	Y	1	3	Y	21	SPDIP, SOIC, SSOP, QFN
	36	32	2	16	5	3	2	1	3	1	—	—	1 ADC, 8-ch	Y	1	3	Y	21	VTLA
dsPIC33FJ32GP104	44	32	2	26	5	3	2	1	3	1	—	—	1 ADC, 14-ch	Y	1	3	Y	35	TQFP, QFN, VTLA
dsPIC33FJ32MC101	20	32	2	10	5	3	2	1	3	1	6-ch	1	1 ADC, 6-ch	Y	1	3	Y	15	PDIP, SOIC, SSOP
dsPIC33FJ32MC102	28	32	2	16	5	3	2	1	3	1	6-ch	2	1 ADC, 8-ch	Y	1	3	Y	21	SPDIP, SOIC, SSOP, QFN
	36	32	2	16	5	3	2	1	3	1	6-ch	2	1 ADC, 8-ch	Y	1	3	Y	21	VTLA
dsPIC33FJ32MC104	44	32	2	26	5	3	2	1	3	1	6-ch	2	1 ADC, 14-ch	Y	1	3	Y	35	TQFP, QFN, VTLA

Note 1: Four out of five timers are remappable.
2: Two pairs can be combined to have up to two 32-bit timers.
3: Two out of three interrupts are remappable.

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Type	Buffer Type	PPS	Description
SCL1	I/O	ST	No	Synchronous serial clock input/output for I2C1.
SDA1	I/O	ST	No	Synchronous serial data input/output for I2C1.
ASCL1	I/O	ST	No	Alternate synchronous serial clock input/output for I2C1.
ASDA1	I/O	ST	No	Alternate synchronous serial data input/output for I2C1.
$\overline{\text{FLTA1}}$(1,2,4)	I	ST	No	PWM1 Fault A input.
$\overline{\text{FLTB1}}$(3,4)	I	ST	No	PWM1 Fault B input.
PWM1L1	O	—	No	PWM1 Low Output 1.
PWM1H1	O	—	No	PWM1 High Output 1.
PWM1L2	O	—	No	PWM1 Low Output 2.
PWM1H2	O	—	No	PWM1 High Output 2.
PWM1L3	O	—	No	PWM1 Low Output 3.
PWM1H3	O	—	No	PWM1 High Output 3.
RTCC	O	Digital	No	RTCC Alarm output.
CTPLS	O	Digital	Yes	CTMU pulse output.
CTED1	I	Digital	No	CTMU External Edge Input 1.
CTED2	I	Digital	No	CTMU External Edge Input 2.
CVREFIN	I	Analog	No	Comparator Voltage Positive Reference Input.
CVREFOUT	O	Analog	No	Comparator Voltage Positive Reference Output.
C1INA	I	Analog	No	Comparator 1 Positive Input A.
C1INB	I	Analog	No	Comparator 1 Negative Input B.
C1INC	I	Analog	No	Comparator 1 Negative Input C.
C1IND	I	Analog	No	Comparator 1 Negative Input D.
C1OUT	O	Digital	Yes	Comparator 1 Output.
C2INA	I	Analog	No	Comparator 2 Positive Input A.
C2INB	I	Analog	No	Comparator 2 Negative Input B.
C2INC	I	Analog	No	Comparator 2 Negative Input C.
C2IND	I	Analog	No	Comparator 2 Negative Input D.
C2OUT	O	Digital	Yes	Comparator 2 Output.
C3INA	I	Analog	No	Comparator 3 Positive Input A.
C3INB	I	Analog	No	Comparator 3 Negative Input B.
C3INC	I	Analog	No	Comparator 3 Negative Input C.
C3IND	I	Analog	No	Comparator 3 Negative Input D.
C3OUT	O	Digital	Yes	Comparator 3 Output.
PGED1	I/O	ST	No	Data I/O pin for Programming/Debugging Communication Channel 1.
PGEC1	I	ST	No	Clock input pin for Programming/Debugging Communication Channel 1.
PGED2	I/O	ST	No	Data I/O pin for Programming/Debugging Communication Channel 2.
PGEC2	I	ST	No	Clock input pin for Programming/Debugging Communication Channel 2.
PGED3	I/O	ST	No	Data I/O pin for Programming/Debugging Communication Channel 3.
PGEC3	I	ST	No	Clock input pin for Programming/Debugging Communication Channel 3.
$\overline{\text{MCLR}}$	I/P	ST	No	Master Clear (Reset) input. This pin is an active-low Reset to the device.

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
PPS = Peripheral Pin Select

Note 1: An external pull-down resistor is required for the $\overline{\text{FLTA1}}$ pin in dsPIC33FJXXMC101 (20-pin) devices.

2: The $\overline{\text{FLTA1}}$ pin and the PWM1Lx/PWM1Hx pins are available in dsPIC(16/32)MC10X devices only.

3: The $\overline{\text{FLTB1}}$ pin is available in dsPIC(16/32)MC102/104 devices only.

4: The PWM Fault pins are enabled during any Reset event. Refer to **Section 15.2 "PWM Faults"** for more information on the PWM Faults.

5: Not all pins are available on all devices. Refer to the specific device in the **"Pin Diagrams"** section for availability.

6: These pins are available in dsPIC33FJ32(GP/MC)104 (44-pin) devices only.

FIGURE 3-2: dsPIC33FJ16(GP/MC)101/102 AND dsPIC33FJ32(GP/MC)101/102/104 PROGRAMMER'S MODEL

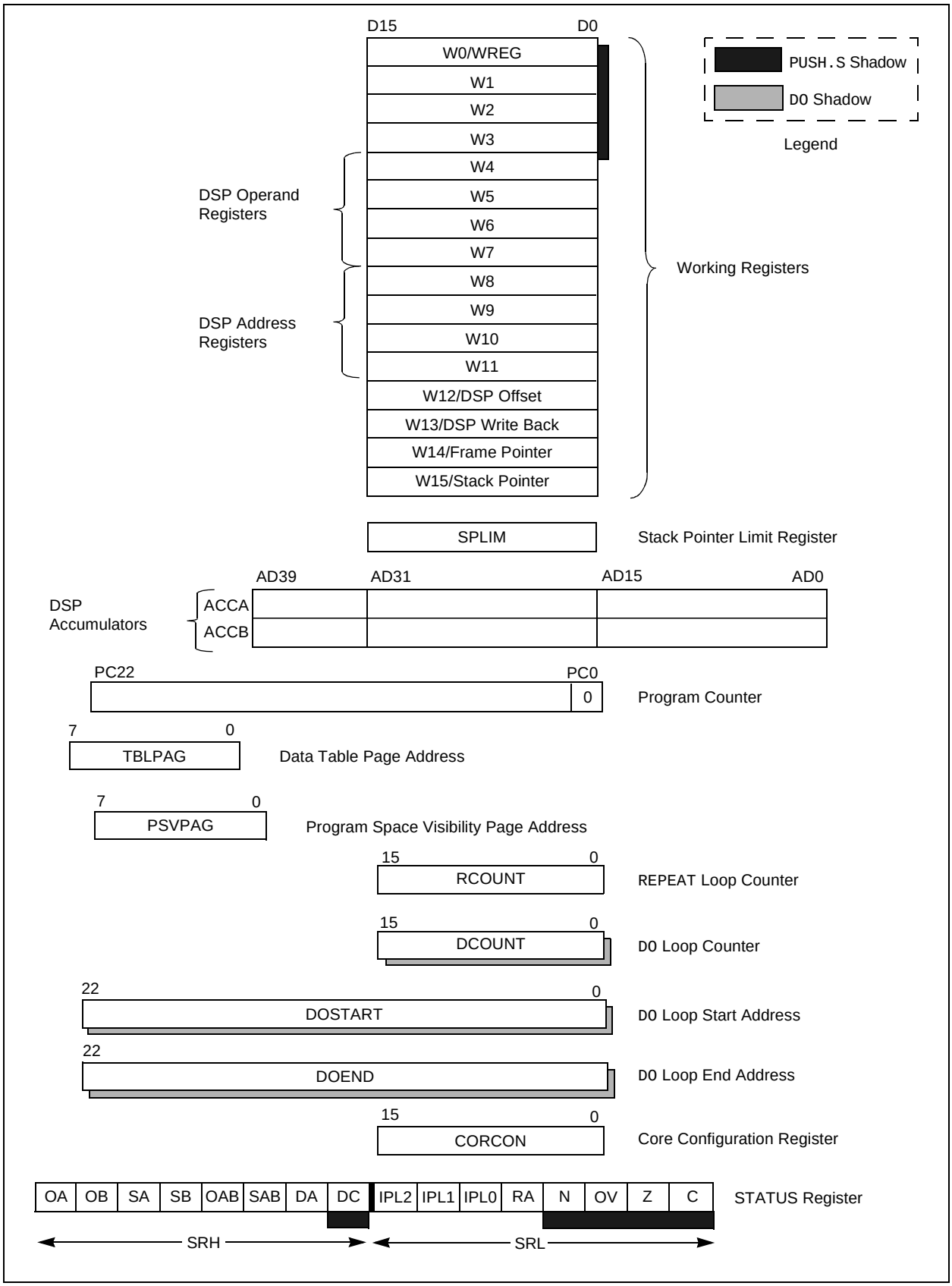


TABLE 4-29: PORTA REGISTER MAP FOR dsPIC33FJ32(GP/MC)104 DEVICES

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISA	02C0	—	—	—	—	—	TRISA<10:7>				—	—	TRISA<4:0>					001F
PORTA	02C2	—	—	—	—	—	RA<10:7>				—	—	RA<4:0>					xxxx
LATA	02C4	—	—	—	—	—	LATA<10:7>				—	—	LATA<4:0>					xxxx
ODCA	02C6	—	—	—	—	—	ODCA<10:7>				—	—	—	ODCA<3:2>		—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-30: PORTB REGISTER MAP FOR dsPIC33FJ16GP101 DEVICES

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISB	02C8	TRISB<15:14>		—	—	—	—	TRISB<9:7>			—	—	TRISB4	—	—	TRISB<1:0>		C393
PORTB	02CA	RB<15:14>		—	—	—	—	RB<9:7>			—	—	RB4	—	—	RB<1:0>		xxxx
LATB	02CC	LATB<15:14>		—	—	—	—	LATB<9:7>			—	—	LATB4	—	—	LATB<1:0>		xxxx
ODCB	02CE	ODCB<15:14>		—	—	—	—	ODCB<9:7>			—	—	ODCB4	—	—	—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-31: PORTB REGISTER MAP FOR dsPIC33FJ16MC101 DEVICES

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISB	02C8	TRISB<15:12>				—	—	TRISB<9:7>			—	—	TRISB4	—	—	TRISB<1:0>		F393
PORTB	02CA	RB<15:12>				—	—	RB<9:7>			—	—	RB4	—	—	RB<1:0>		xxxx
LATB	02CC	LATB<15:12>				—	—	LATB<9:7>			—	—	LATB4	—	—	LATB<1:0>		xxxx
ODCB	02CE	ODCB<15:12>				—	—	ODCB<9:7>			—	—	ODCB4	—	—	—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-32: PORTB REGISTER MAP FOR dsPIC33FJ16(GP/MC)102 DEVICES

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISB	02C8	TRISB<15:0>																FFFF
PORTB	02CA	RB<15:0>																xxxx
LATB	02CC	LATB<15:0>																xxxx
ODCB	02CE	ODCB<15:4>												—	—	—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

5.0 FLASH PROGRAM MEMORY

Note 1: This data sheet summarizes the features of the dsPIC33FJ16(GP/MC)101/102 and dsPIC33FJ32(GP/MC)101/102/104 family devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Flash Programming"** (DS70191) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33FJ16(GP/MC)101/102 and dsPIC33FJ32(GP/MC)101/102/104 devices contain internal Flash program memory for storing and executing application code. The memory is readable, writable and erasable during normal operation over the entire VDD range.

Flash memory can be programmed in two ways:

- In-Circuit Serial Programming™ (ICSP™) programming capability
- Run-Time Self-Programming (RTSP)

ICSP allows a device to be serially programmed while in the end application circuit. This is done with two lines for programming clock and programming data (one of the alternate programming pin pairs: PGECx/PGEDx), and three other lines for power (VDD), ground (VSS) and Master Clear ($\overline{MCLR}$). This allows users to manufacture boards with unprogrammed devices and then program the Digital Signal Controller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

RTSP is accomplished using TBLRD (Table Read) and TBLWT (Table Write) instructions. With RTSP, the user application can write program memory data in a single program memory word and erase program memory in blocks or 'pages' of 512 instructions (1536 bytes).

5.1 Table Instructions and Flash Programming

Regardless of the method used, all programming of Flash memory is done with the Table Read and Table Write instructions. These allow direct read and write access to the program memory space, from the data memory, while the device is in normal operating mode. The 24-bit target address in the program memory is formed using bits<7:0> of the TBLPAG register and the Effective Address (EA) from a W register specified in the table instruction, as shown in Figure 5-1.

The TBLRDL and the TBLWTL instructions are used to read or write to bits<15:0> of program memory. TBLRDL and TBLWTL can access program memory in both Word and Byte modes.

The TBLRDH and TBLWTH instructions are used to read or write to bits<23:16> of program memory. TBLRDH and TBLWTH can also access program memory in Word or Byte mode.

FIGURE 5-1: ADDRESSING FOR TABLE REGISTERS

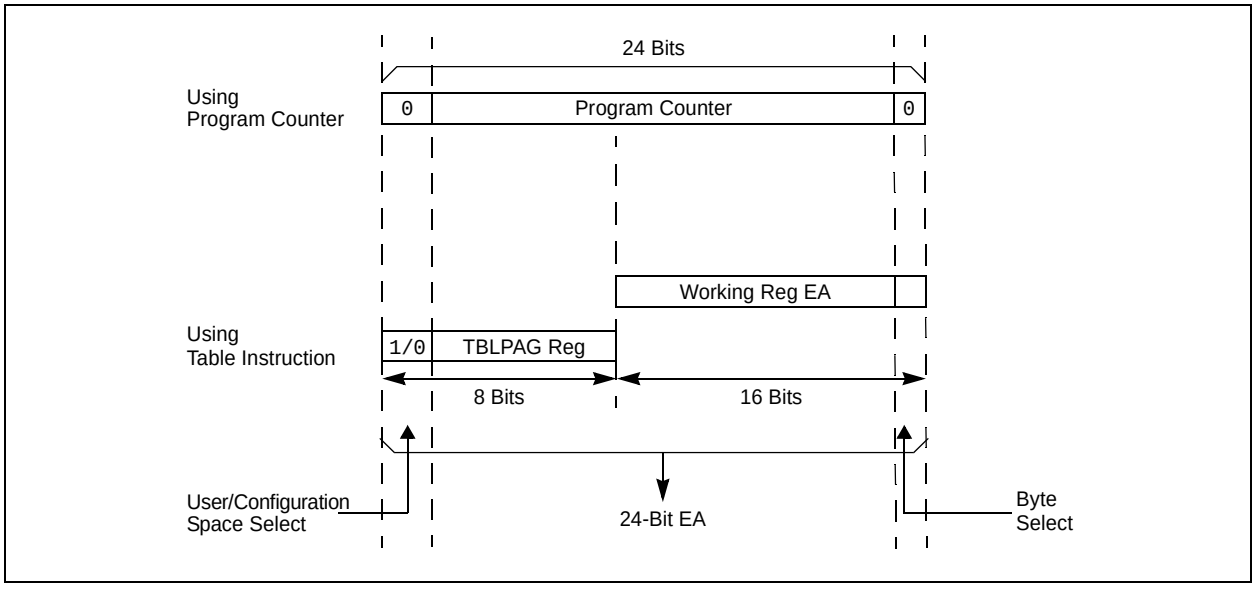
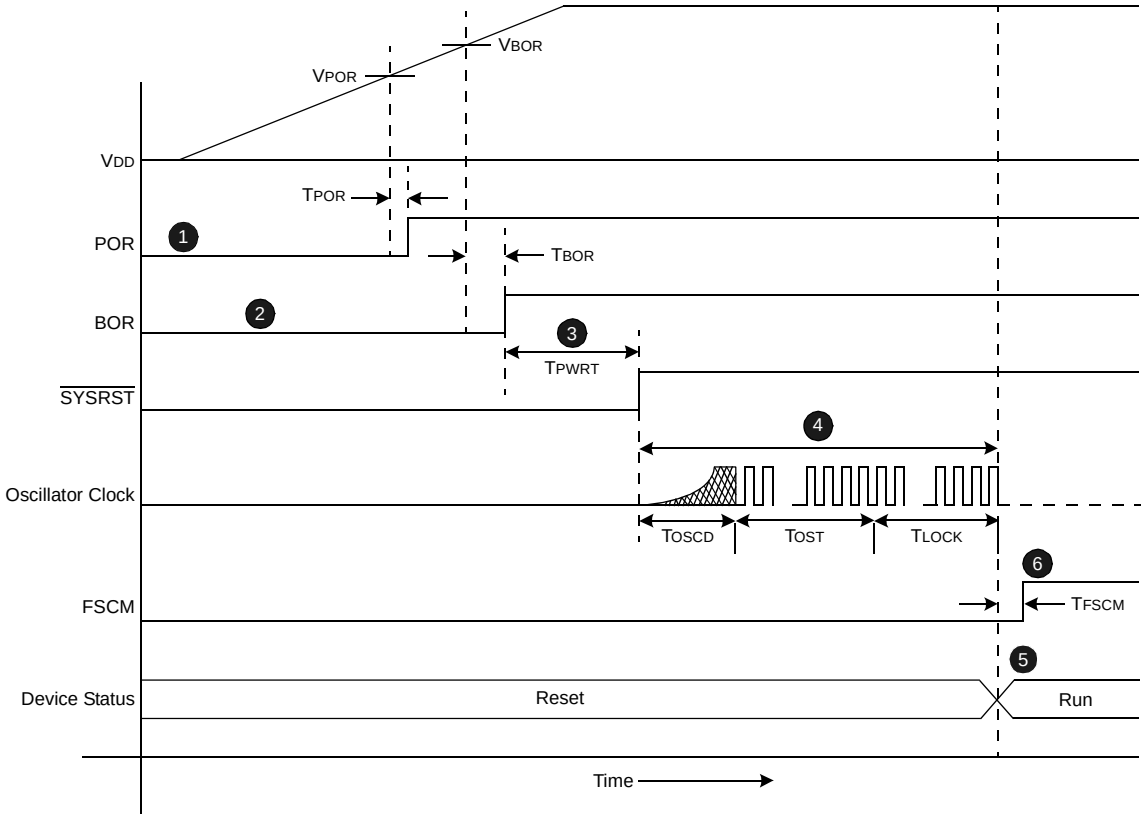


FIGURE 6-2: SYSTEM RESET TIMING



1. **POR:** A POR circuit holds the device in Reset when the power supply is turned on. The POR circuit is active until VDD crosses the VPOR threshold and the delay, TPOR, has elapsed.
2. **BOR:** The on-chip voltage regulator has a BOR circuit that keeps the device in Reset until VDD crosses the VBOR threshold and the delay, TBOR, has elapsed. The delay, TBOR, ensures the voltage regulator output becomes stable.
3. **PWRT Timer:** The Power-up Timer continues to hold the processor in Reset for a specific period of time (TPWRT) after a BOR. The delay, TPWRT, ensures that the system power supplies have stabilized at the appropriate level for full-speed operation. After the delay, TPWRT, has elapsed, the SYSRST becomes inactive, which in turn, enables the selected oscillator to start generating clock cycles.
4. **Oscillator Delay:** The total delay for the clock to be ready for various clock source selections is given in Table 6-1. Refer to **Section 8.0 "Oscillator Configuration"** for more information.
5. When the oscillator clock is ready, the processor begins execution from location, 0x000000. The user application programs a GOTO instruction at the Reset address, which redirects program execution to the appropriate start-up routine.
6. The Fail-Safe Clock Monitor (FSCM), if enabled, begins to monitor the system clock when the system clock is ready and the delay, TFSCM, has elapsed.

TABLE 6-2: OSCILLATOR PARAMETERS

Symbol	Parameter	Value
VPOR	POR Threshold	1.8V nominal
TPOR	POR Extension Time	30 μs maximum
VBOR	BOR Threshold	2.5V nominal
TBOR	BOR Extension Time	100 μs maximum
TPWRT	Power-up Time Delay	64 ms nominal
TFSCM	Fail-Safe Clock Monitor Delay	900 μs maximum

Note: When the device exits the Reset condition (begins normal operation), the device operating parameters (voltage, frequency, temperature, etc.) must be within their operating ranges; otherwise, the device may not function correctly. The user application must ensure that the delay between the time power is first applied, and the time SYSRST becomes inactive, is long enough to get all operating parameters within specification.

TABLE 7-1: INTERRUPT VECTORS

Vector Number	Interrupt Request (IRQ) Number	IVT Address	AIVT Address	Interrupt Source
8	0	0x000014	0x000114	INT0 – External Interrupt 0
9	1	0x000016	0x000116	IC1 – Input Capture 1
10	2	0x000018	0x000118	OC1 – Output Compare 1
11	3	0x00001A	0x00011A	T1 – Timer1
12	4	0x00001C	0x00011C	Reserved
13	5	0x00001E	0x00011E	IC2 – Input Capture 2
14	6	0x000020	0x000120	OC2 – Output Compare 2
15	7	0x000022	0x000122	T2 – Timer2
16	8	0x000024	0x000124	T3 – Timer3
17	9	0x000026	0x000126	SPI1E – SPI1 Error
18	10	0x000028	0x000128	SPI1 – SPI1 Transfer Done
19	11	0x00002A	0x00012A	U1RX – UART1 Receiver
20	12	0x00002C	0x00012C	U1TX – UART1 Transmitter
21	13	0x00002E	0x00012E	ADC1 – ADC1
22-23	14-15	0x000030-0x000032	0x000130-0x000132	Reserved
24	16	0x000034	0x000134	SI2C1 – I2C1 Slave Events
25	17	0x000036	0x000136	MI2C1 – I2C1 Master Events
26	18	0x000038	0x000138	CMP – Comparator Interrupt
27	19	0x00003A	0x00013A	Change Notification Interrupt
28	20	0x00003C	0x00013C	INT1 – External Interrupt 1
29-34	21-26	0x00003E-0x000038	0x00013E-0x000138	Reserved
35	27	0x00004A	0x00014A	T4 – Timer4(2)
36	28	0x00004C	0x00014C	T5 – Timer5(2)
37	29	0x00004E	0x00014E	INT2 – External Interrupt 2
38-44	30-36	0x000050-0x00005C	0x000150-0x00015C	Reserved
45	37	0x00005E	0x00015E	IC3 – Input Capture 3
46-64	38-56	0x000060-0x000084	0x000160-0x000184	Reserved
65	57	0x000086	0x000186	PWM1 – PWM1 Period Match(1)
66-69	58-61	0x000088-0x00008E	0x000188-0x00018E	Reserved
70	62	0x000090	0x000190	RTCC – Real-Time Clock and Calendar
71	63	0x000092	0x000192	$\overline{\text{FLTA1}}$ – PWM1 Fault A(1)
72	64	0x000094	0x000194	$\overline{\text{FLTB1}}$ – PWM1 Fault B(3)
73	65	0x000096	0x000196	U1E – UART1 Error
74-84	66-76	0x000098-0x0000AC	0x000198-0x0001AC	Reserved
85	77	0x0000AE	0x0001AE	CTMU – Charge Time Measurement Unit
86-125	78-117	0x0000B0-0x0000FE	0x0001B0-0x0001FE	Reserved

Note 1: This interrupt vector is available in dsPIC33FJ(16/32)MC10X devices only.

2: This interrupt vector is available in dsPIC33FJ32(GP/MC)10X devices only.

3: This interrupt vector is available in dsPIC33FJ(16/32)MC102/104 devices only.

REGISTER 7-14: IEC4: INTERRUPT ENABLE CONTROL REGISTER 4

U-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
—	—	CTMUIE	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	U1EIE	FLTB1IE(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **CTMUIE:** CTMU Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 12-2 **Unimplemented:** Read as '0'

bit 1 **U1EIE:** UART1 Error Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 0 **FLTB1IE:** PWM1 Fault B Interrupt Enable bit(1)
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

Note 1: This bit is available in dsPIC(16/32)MC102/104 devices only.

10.0 I/O PORTS

Note 1: This data sheet summarizes the features of the dsPIC33FJ16(GP/MC)101/102 and dsPIC33FJ32(GP/MC)101/102/104 family devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"I/O Ports"** (DS70193) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

All of the device pins (except VDD, VSS, $\overline{\text{MCLR}}$ and OSC1/CLKI) are shared among the peripherals and the parallel I/O ports. All I/O input ports feature Schmitt Trigger inputs for improved noise immunity.

10.1 Parallel I/O (PIO) Ports

Generally a parallel I/O port that shares a pin with a peripheral is subservient to the peripheral. The peripheral's output buffer data and control signals are provided to a pair of multiplexers. The multiplexers select whether the peripheral or the associated port has ownership of the output data and control signals of the I/O pin. The logic also prevents "loop through," in which a port's digital output can drive the input of a peripheral that shares the same pin. Figure 10-1 shows how ports are shared with other peripherals and the associated I/O pin to which they are connected.

When a peripheral is enabled and the peripheral is actively driving an associated pin, the use of the pin as a general purpose output pin is disabled. The I/O pin can be read, but the output driver for the parallel port bit is disabled. If a peripheral is enabled, but the peripheral is not actively driving a pin, that pin can be driven by a port.

All port pins have three registers directly associated with their operation as digital I/O. The Data Direction register (TRISx) determines whether the pin is an input or an output. If the data direction bit is a '1', the pin is an input. All port pins are defined as inputs after a Reset. Reads from the Output Latch (LATx) register read the latch. Writes to the Output Latch register write the latch. Reads from the port (PORTx) read the port pins, while writes to the port pins write the latch.

Any bit and its associated data and control registers that is not valid for a particular device will be disabled. This means the corresponding LATx and TRISx registers and the port pin will read as zeros.

When a pin is shared with another peripheral or function that is defined as an input only, it is nevertheless regarded as a dedicated port because there is no other competing source of outputs.

REGISTER 10-9: RPINR20: PERIPHERAL PIN SELECT INPUT REGISTER 20

U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	—	SCK1R4(1)	SCK1R3(1)	SCK1R2(1)	SCK1R1(1)	SCK1R0(1)
bit 15							bit 8

U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	—	SDI1R4(1)	SDI1R3(1)	SDI1R2(1)	SDI1R1(1)	SDI1R0(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **SCK1R<4:0>:** Assign SPI1 Clock Input (SCK1IN) to the Corresponding RPn Pin bits(1)

11111 = Input tied to Vss
11110 = Reserved
.
.
.
11010 = Reserved
11001 = Input tied to RP25
.
.
.
00001 = Input tied to RP1
00000 = Input tied to RP0

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **SDI1R<4:0>:** Assign SPI1 Data Input (SDI1) to the Corresponding RPn Pin bits(1)

11111 = Input tied to Vss
11110 = Reserved
.
.
.
11010 = Reserved
11001 = Input tied to RP25
.
.
.
00001 = Input tied to RP1
00000 = Input tied to RP0

Note 1: These bits are available in dsPIC33FJ32(GP/MC)10X devices only.

REGISTER 12-4: T5CON: TIMER5 CONTROL REGISTER(1)

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
TON(3)	—	TSIDL(2)	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	U-0
—	TGATE(3)	TCKPS1(3)	TCKPS0(3)	—	—	TCS(3)	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **TON:** Timer5 On bit(3)
1 = Starts 16-bit Timer3
0 = Stops 16-bit Timer3

bit 14 **Unimplemented:** Read as '0'

bit 13 **TSIDL:** Timer5 Stop in Idle Mode bit(2)
1 = Discontinues timer operation when device enters Idle mode
0 = Continues timer operation in Idle mode

bit 12-7 **Unimplemented:** Read as '0'

bit 6 **TGATE:** Timer5 Gated Time Accumulation Enable bit(3)
When TCS = 1:
This bit is ignored.
When TCS = 0:
1 = Gated time accumulation is enabled
0 = Gated time accumulation is disabled

bit 5-4 **TCKPS<1:0>:** Timer5 Input Clock Prescale Select bits(3)
11 = 1:256 prescale value
10 = 1:64 prescale value
01 = 1:8 prescale value
00 = 1:1 prescale value

bit 3-2 **Unimplemented:** Read as '0'

bit 1 **TCS:** Timer5 Clock Source Select bit(3)
1 = External clock from T5CK pin
0 = Internal clock (FOSC/2)

bit 0 **Unimplemented:** Read as '0'

Note 1: This register is available in dsPIC33FJ32(GP/MC)10X devices only.

2: When 32-bit timer operation is enabled (T32 = 1) in the Timer4 Control register (T4CON<3>), the TSIDL bit must be cleared to operate the 32-bit timer in Idle mode.

3: When the 32-bit timer operation is enabled (T32 = 1) in the Timer4 Control register (T4CON<3>), these bits have no effect.

13.0 INPUT CAPTURE

Note 1: This data sheet summarizes the features of the dsPIC33FJ16(GP/MC)101/102 and dsPIC33FJ32(GP/MC)101/102/104 family devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Input Capture"** (DS70198) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The input capture module is useful in applications requiring frequency (period) and pulse measurement. The dsPIC33FJ16(GP/MC)101/102 and dsPIC33FJ32(GP/MC)101/102/104 devices support up to three input capture channels.

The input capture module captures the 16-bit value of the selected Time Base register when an event occurs on the ICx pin. The events that cause a capture event are listed below in three categories:

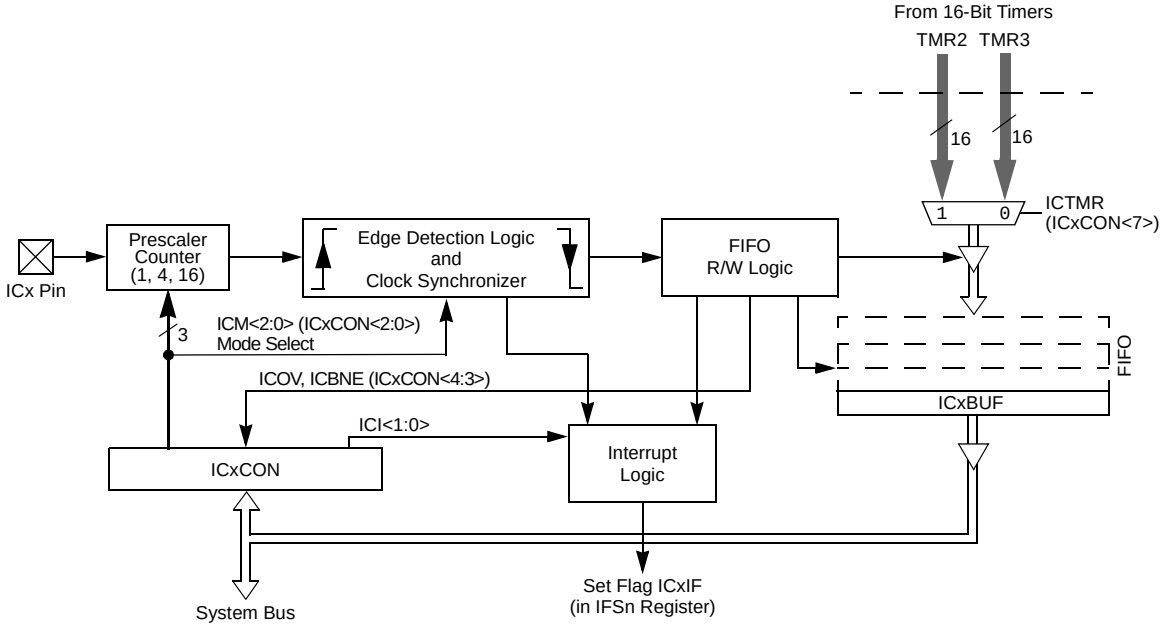
1. Simple Capture Event modes:
   - Capture timer value on every falling edge of input at ICx pin
   - Capture timer value on every rising edge of input at ICx pin
2. Capture timer value on every edge (rising and falling).
3. Prescaler Capture Event modes:
   - Capture timer value on every 4th rising edge of input at ICx pin
   - Capture timer value on every 16th rising edge of input at ICx pin

Each input capture channel can select one of two 16-bit timers (Timer2 or Timer3) for the time base. The selected timer can use either an internal or external clock.

Other operational features include:

- Device wake-up from capture pin during CPU Sleep and Idle modes
- Interrupt on input capture event
- 4-word FIFO buffer for capture values:
  - Interrupt optionally generated after 1, 2, 3 or 4 buffer locations are filled
- Use of input capture to provide additional sources of external interrupts

FIGURE 13-1: INPUT CAPTURE x BLOCK DIAGRAM



Note: An 'x' in a signal, register or bit name denotes the number of the input capture channel.

REGISTER 15-5: PWMxCON1: PWMx CONTROL REGISTER 1(1)

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	PMOD3	PMOD2	PMOD1
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
—	PEN3H(2)	PEN2H(2)	PEN1H(2)	—	PEN3L(2)	PEN2L(2)	PEN1L(2)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-11 **Unimplemented:** Read as '0'

bit 10-8 **PMOD<3:1>:** PWMx I/O Pair Mode bits
1 = PWMx I/O pin pair is in the Independent PWM Output mode
0 = PWMx I/O pin pair is in the Complementary Output mode

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **PEN3H:PEN1H:** PWMxH I/O Enable bits(2)
1 = PWMxH pin is enabled for PWMx output
0 = PWMxH pin is disabled, I/O pin becomes a general purpose I/O

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **PEN3L:PEN1L:** PWMxL I/O Enable bits(2)
1 = PWMxL pin is enabled for PWMx output
0 = PWMxL pin is disabled, I/O pin becomes a general purpose I/O

Note 1: The PWMxCON1 register is a write-protected register. Refer to **Section 15.3 "Write-Protected Registers"** for more information on the unlock sequence.

2: The Reset status for these bits depends on the setting of the PWMPIN Configuration bit (FPOR<7>):
- If PWMPIN = 1 (default), the PWM pins are controlled by the PORT register at Reset, meaning they are initially programmed as inputs (i.e., tri-stated).
- If PWMPIN = 0, the PWM pins are controlled by the PWM module at Reset and are therefore, initially programmed as output pins.

REGISTER 15-9: PxFLTACON: PWMx FAULT A CONTROL REGISTER(1,2,3,4)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	FAOV3H	FAOV3L	FAOV2H	FAOV2L	FAOV1H	FAOV1L
bit 15							bit 8

R/W-0	U-0	U-0	U-0	U-0	R/W-1	R/W-1	R/W-1
FLTAM	—	—	—	—	FAEN3	FAEN2	FAEN1
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **FAOV<3:1>H:FAOV<3:1>L:** Fault Input A PWMx Override Value bits
1 = The PWMx output pin is driven active on an external Fault input event
0 = The PWMx output pin is driven inactive on an external Fault input event

bit 7 **FLTAM:** Fault A Mode bit
1 = The Fault A input pin functions in the Cycle-by-Cycle mode
0 = The Fault A input pin latches all control pins to the programmed states in PxFLTACON<13:8>

bit 6-3 **Unimplemented:** Read as '0'

bit 2 **FAEN3:** Fault Input A Enable bit
1 = PWMxH3/PWMxL3 pin pair is controlled by Fault Input A
0 = PWMxH3/PWMxL3 pin pair is not controlled by Fault Input A

bit 1 **FAEN2:** Fault Input A Enable bit
1 = PWMxH2/PWMxL2 pin pair is controlled by Fault Input A
0 = PWMxH2/PWMxL2 pin pair is not controlled by Fault Input A

bit 0 **FAEN1:** Fault Input A Enable bit
1 = PWMxH1/PWMxL1 pin pair is controlled by Fault Input A
0 = PWMxH1/PWMxL1 pin pair is not controlled by Fault Input A

Note 1: Comparator outputs are not internally connected to the PWM Fault control logic. If using the comparator modules for Fault generation, the user must externally connect the desired comparator output pin to the dedicated $\overline{\text{FLTA1}}$ or $\overline{\text{FLTB1}}$ input pin.

2: Refer to Table 15-1 for $\overline{\text{FLTA1}}$ implementation details.

3: The PxFLTACON register is a write-protected register. Refer to **Section 15.3 "Write-Protected Registers"** for more information on the unlock sequence.

4: During any Reset event, $\overline{\text{FLTA1}}$ is enabled by default and must be cleared as described in **Section 15.2 "PWM Faults"**.

16.1 SPI Helpful Tips

1. In Frame mode, if there is a possibility that the master may not be initialized before the slave:
   a) If FRMPOL (SPIxCON2<13>) = 1, use a pull-down resistor on $\overline{SSx}$.
   b) If FRMPOL = 0, use a pull-up resistor on $\overline{SSx}$.

Note:	This insures that the first frame transmission after initialization is not shifted or corrupted.

2. In Non-Framed 3-Wire mode (i.e., not using $\overline{SSx}$ from a master):
   a) If CKP (SPIxCON1<6>) = 1, always place a pull-up resistor on $\overline{SSx}$.
   b) If CKP = 0, always place a pull-down resistor on $\overline{SSx}$.

Note:	This will insure that during power-up and initialization, the master/slave will not lose sync due to an errant SCK transition that would cause the slave to accumulate data shift errors for both transmit and receive, appearing as corrupted data.

3. FRMEN (SPIxCON2<15>) = 1 and SSEN (SPIxCON1<7>) = 1 are exclusive and invalid. In Frame mode, SCKx is continuous and the Frame Sync pulse is active on the $\overline{SSx}$ pin, which indicates the start of a data frame.

Note:	Not all third-party devices support Frame mode timing. Refer to the SPI electrical characteristics for details.

4. In Master mode only, set the SMP bit (SPIxCON1<9>) to a '1' for the fastest SPI data rate possible. The SMP bit can only be set at the same time or after the MSTEN bit (SPIxCON1<5>) is set.
5. To avoid invalid slave read data to the master, the user's master software must ensure enough time for slave software to fill its write buffer before the user application initiates a master write/read cycle. It is always advisable to pre-load the SPIxBUF Transmit register in advance of the next master transaction cycle. SPIxBUF is transferred to the SPIx Shift register and is empty once the data transmission begins.
6. The SPI related pins (SDI1, SDO1, SCK1) are located at fixed positions in the dsPIC33FJ16(GP/MC)10X devices. The same pins are remappable in the dsPIC33FJ32(GP/MC)10X devices.

16.2 SPI Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en554109

16.2.1 KEY RESOURCES

- **"Serial Peripheral Interface (SPI)"** (DS70206) in the "*dsPIC33/PIC24 Family Reference Manual*".
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related "*dsPIC33/PIC24 Family Reference Manual*" sections
- Development Tools

22.1 CTMU Control Registers

REGISTER 22-1: CTMUCON1: CTMU CONTROL REGISTER 1

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CTMUEN	—	CTMUSIDL	TGEN(1)	EDGEN	EDGSEQEN	IDISSEN(2)	CTTRIG
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CTMUEN:** CTMU Enable bit
1 = Module is enabled
0 = Module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **CTMUSIDL:** CTMU Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12 **TGEN:** Time Generation Enable bit(1)
1 = Enables edge delay generation
0 = Disables edge delay generation

bit 11 **EDGEN:** Edge Enable bit
1 = Edges are not blocked
0 = Edges are blocked

bit 10 **EDGSEQEN:** Edge Sequence Enable bit
1 = Edge 1 event must occur before Edge 2 event can occur
0 = No edge sequence is needed

bit 9 **IDISSEN:** Analog Current Source Control bit(2)
1 = Analog current source output is grounded
0 = Analog current source output is not grounded

bit 8 **CTTRIG:** CTMU Trigger Control bit
1 = Trigger output is enabled
0 = Trigger output is disabled

bit 7-0 **Unimplemented:** Read as '0'

Note 1: If TGEN = 1, the peripheral inputs and outputs must be configured to an available RPn pin. For more information, see **Section 10.4 "Peripheral Pin Select (PPS)"**.

2: The ADC module S&H capacitor is not automatically discharged between sample/conversion cycles. Software using the ADC as part of a capacitance measurement must discharge the ADC capacitor before conducting the measurement. The IDISSEN bit, when set to '1', performs this function. The ADC must be sampling while the IDISSEN bit is active to connect the discharge sink to the capacitor array.

25.11 Demonstration/Development Boards, Evaluation Kits and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

25.12 Third-Party Development Tools

Microchip also offers a great collection of tools from third-party vendors. These tools are carefully selected to offer good value and unique functionality.

- Device Programmers and Gang Programmers from companies, such as SoftLog and CCS
- Software Tools from companies, such as Gimpel and Trace Systems
- Protocol Analyzers from companies, such as Saleae and Total Phase
- Demonstration Boards from companies, such as MikroElektronika, Digilent® and Olimex
- Embedded Ethernet Solutions from companies, such as EZ Web Lynx, WIZnet and IPLogika®

TABLE 26-35: SPIx SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0) TIMING REQUIREMENTS FOR dsPIC33FJ16(GP/MC)10X

AC CHARACTERISTICS			Standard Operating Conditions: 2.4V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic(1)**	**Min**	**Typ(2)**	**Max**	**Units**	**Conditions**
SP70	TscP	Maximum SCKx Input Frequency	—	—	15	MHz	See **Note 3**
SP72	TscF	SCKx Input Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP73	TscR	SCKx Input Rise Time	—	—	—	ns	See Parameter DO31 and **Note 4**
SP30	TdoF	SDOx Data Output Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP31	TdoR	SDOx Data Output Rise Time	—	—	—	ns	See Parameter DO31 and **Note 4**
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SSx}$ ↓ to SCKx ↑ or SCKx Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{SSx}$ ↑ to SDOx Output High-Impedance	10	—	50	ns	See **Note 4**
SP52	TscH2ssH TscL2ssH	$\overline{SSx}$ after SCKx Edge	1.5 TCY + 40	—	—	ns	See **Note 4**

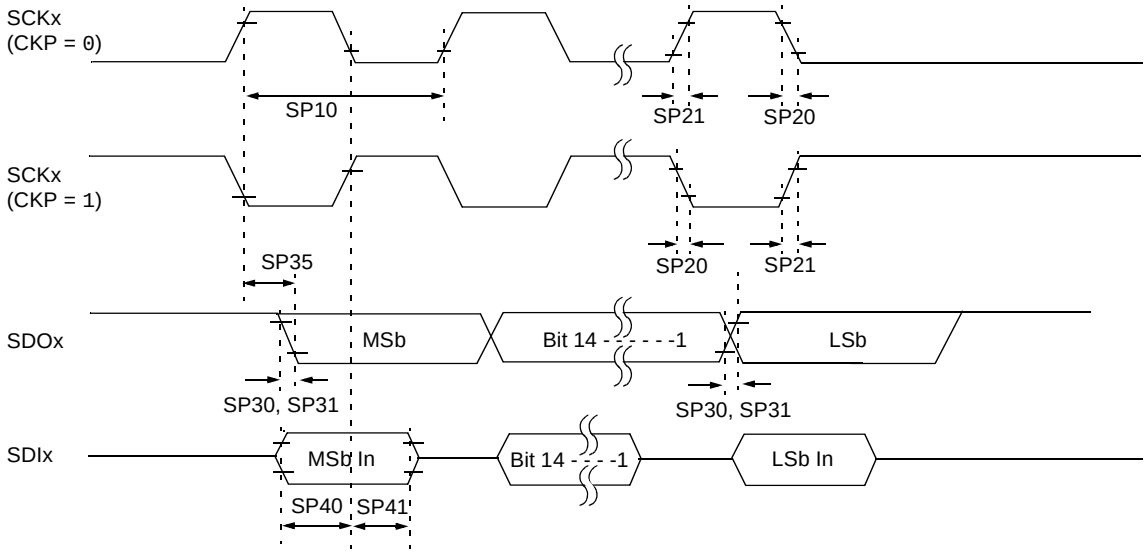
Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCKx is 66.7 ns. Therefore, the SCKx clock generated by the Master must not violate this specification.

4: Assumes 50 pF load on all SPIx pins.

FIGURE 26-22: SPIx MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1) TIMING CHARACTERISTICS FOR dsPIC33FJ32(GP/MC)10X



Note: Refer to Figure 26-1 for load conditions.

TABLE 26-40: SPIx MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1) TIMING REQUIREMENTS FOR dsPIC33FJ32(GP/MC)10X

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic(1)**	**Min**	**Typ(2)**	**Max**	**Units**	**Conditions**
SP10	TscP	Maximum SCKx Frequency	—	—	9	MHz	-40°C to +125°C, see **Note 3**
SP20	TscF	SCKx Output Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP21	TscR	SCKx Output Rise Time	—	—	—	ns	See Parameter DO31 and **Note 4**
SP30	TdoF	SDOx Data Output Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP31	TdoR	SDOx Data Output Rise Time	—	—	—	ns	See Parameter DO31 and **Note 4**
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	—	—	ns	

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCKx is 111 ns. The clock generated in Master mode must not violate this specification.

4: Assumes 50 pF load on all SPIx pins.

TABLE 26-45: I2Cx BUS DATA TIMING REQUIREMENTS (MASTER MODE)

AC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Param No.	**Symbol**	**Characteristic**		**Min(1)**	**Max**	**Units**	**Conditions**
IM10	TLO:SCL	Clock Low Time	100 kHz mode	TCY/2 (BRG + 1)	—	µs	
			400 kHz mode	TCY/2 (BRG + 1)	—	µs	
			1 MHz mode(2)	TCY/2 (BRG + 1)	—	µs	
IM11	THI:SCL	Clock High Time	100 kHz mode	TCY/2 (BRG + 1)	—	µs	
			400 kHz mode	TCY/2 (BRG + 1)	—	µs	
			1 MHz mode(2)	TCY/2 (BRG + 1)	—	µs	
IM20	TF:SCL	SDAx and SCLx Fall Time	100 kHz mode	—	300	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
			1 MHz mode(2)	—	100	ns	
IM21	TR:SCL	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
			1 MHz mode(2)	—	300	ns	
IM25	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	ns	
			400 kHz mode	100	—	ns	
			1 MHz mode(2)	40	—	ns	
IM26	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	µs	
			400 kHz mode	0	0.9	µs	
			1 MHz mode(2)	0.2	—	µs	
IM30	TSU:STA	Start Condition Setup Time	100 kHz mode	TCY/2 (BRG + 1)	—	µs	Only relevant for Repeated Start condition
			400 kHz mode	TCY/2 (BRG + 1)	—	µs	
			1 MHz mode(2)	TCY/2 (BRG + 1)	—	µs	
IM31	THD:STA	Start Condition Hold Time	100 kHz mode	TCY/2 (BRG + 1)	—	µs	After this period the first clock pulse is generated
			400 kHz mode	TCY/2 (BRG + 1)	—	µs	
			1 MHz mode(2)	TCY/2 (BRG + 1)	—	µs	
IM33	TSU:STO	Stop Condition Setup Time	100 kHz mode	TCY/2 (BRG + 1)	—	µs	
			400 kHz mode	TCY/2 (BRG + 1)	—	µs	
			1 MHz mode(2)	TCY/2 (BRG + 1)	—	µs	
IM34	THD:STO	Stop Condition Hold Time	100 kHz mode	TCY/2 (BRG + 1)	—	ns	
			400 kHz mode	TCY/2 (BRG + 1)	—	ns	
			1 MHz mode(2)	TCY/2 (BRG + 1)	—	ns	
IM40	TAA:SCL	Output Valid from Clock	100 kHz mode	—	3500	ns	
			400 kHz mode	—	1000	ns	
			1 MHz mode(2)	—	400	ns	
IM45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	µs	Time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	µs	
			1 MHz mode(2)	0.5	—	µs	
IM50	CB	Bus Capacitive Loading		—	400	pF	
IM51	TPGD	Pulse Gobbler Delay		65	390	ns	See **Note 3**

Note 1: BRG is the value of the I2C™ Baud Rate Generator. Refer to **"Inter-Integrated Circuit (I2C™)"** (DS70195) in the "*dsPIC33/PIC24 Family Reference Manual*". Please see the Microchip web site for the latest "*dsPIC33/PIC24 Family Reference Manual*" sections.

2: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

3: Typical value for this parameter is 130 ns.