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Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	16 MIPS
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, Motor Control PWM, POR, PWM, WDT
Number of I/O	21
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj16mc102-e-ss

REGISTER 3-1: SR: CPU STATUS REGISTER (CONTINUED)

bit 7-5	IPL<2:0> : CPU Interrupt Priority Level Status bits ^(2,3) 111 = CPU Interrupt Priority Level is 7 (15), user interrupts are disabled 110 = CPU Interrupt Priority Level is 6 (14) 101 = CPU Interrupt Priority Level is 5 (13) 100 = CPU Interrupt Priority Level is 4 (12) 011 = CPU Interrupt Priority Level is 3 (11) 010 = CPU Interrupt Priority Level is 2 (10) 001 = CPU Interrupt Priority Level is 1 (9) 000 = CPU Interrupt Priority Level is 0 (8)
bit 4	RA : REPEAT Loop Active bit 1 = REPEAT loop is in progress 0 = REPEAT loop is not in progress
bit 3	N : MCU ALU Negative bit 1 = Result was negative 0 = Result was non-negative (zero or positive)
bit 2	OV : MCU ALU Overflow bit This bit is used for signed arithmetic (2's complement). It indicates an overflow of a magnitude that causes the sign bit to change state. 1 = Overflow occurred for signed arithmetic (in this arithmetic operation) 0 = No overflow occurred
bit 1	Z : MCU ALU Zero bit 1 = An operation that affects the Z bit has set it at some time in the past 0 = The most recent operation that affects the Z bit has cleared it (i.e., a non-zero result)
bit 0	C : MCU ALU Carry/Borrow bit 1 = A carry-out from the Most Significant bit of the result occurred 0 = No carry-out from the Most Significant bit of the result occurred

- Note 1:** This bit can be read or cleared (not set).
- 2:** The IPL<2:0> bits are concatenated with the IPL<3> bit (CORCON<3>) to form the CPU Interrupt Priority Level. The value in parentheses indicates the IPL if IPL<3> = 1. User interrupts are disabled when IPL<3> = 1.
- 3:** The IPL<2:0> Status bits are read-only when NSTDIS = 1 (INTCON1<15>).

4.0 MEMORY ORGANIZATION

Note: This data sheet summarizes the features of the dsPIC33FJ16(GP/MC)101/102 and dsPIC33FJ32(GP/MC)101/102/104 family devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “Data Memory” (DS70202) and “Program Memory” (DS70203) in the “dsPIC33/PIC24 Family Reference Manual”, which are available from the Microchip web site (www.microchip.com).

The device architecture features separate program and data memory spaces and buses. This architecture also allows the direct access of program memory from the data space during code execution.

4.1 Program Address Space

The program address memory space of the dsPIC33FJ16(GP/MC)101/102 and dsPIC33FJ32(GP/MC)101/102/104 devices is 4M instructions. The space is addressable by a 24-bit value derived either from the 23-bit Program Counter (PC) during program execution, or from table operation or data space remapping as described in **Section 4.6 “Interfacing Program and Data Memory Spaces”**.

User application access to the program memory space is restricted to the lower half of the address range (0x000000 to 0x7FFFFFFF). The exception is the use of TBLRD/TBLWT operations, which use TBLPAG<7> to permit access to the Configuration bits and Device ID sections of the configuration memory space.

The memory maps for the dsPIC33FJ16(GP/MC)101/102 and dsPIC33FJ32(GP/MC)101/102/104 family of devices are shown in Figure 4-1 and Figure 4-2.

FIGURE 4-1: PROGRAM MEMORY MAP FOR dsPIC33FJ16(GP/MC)101/102 DEVICES

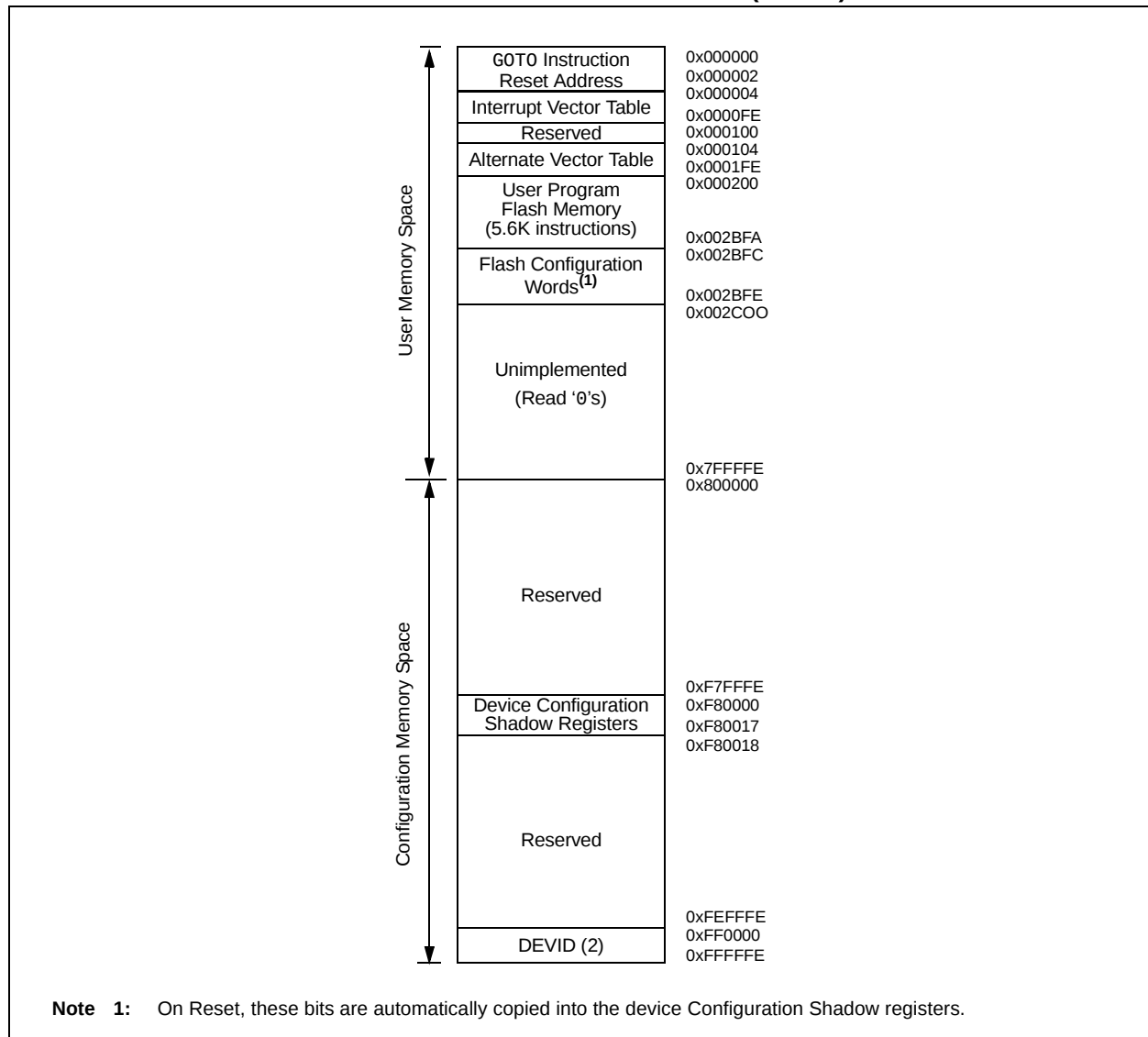


FIGURE 4-2: PROGRAM MEMORY MAP FOR dsPIC33FJ32(GP/MC)101/102/104 DEVICES

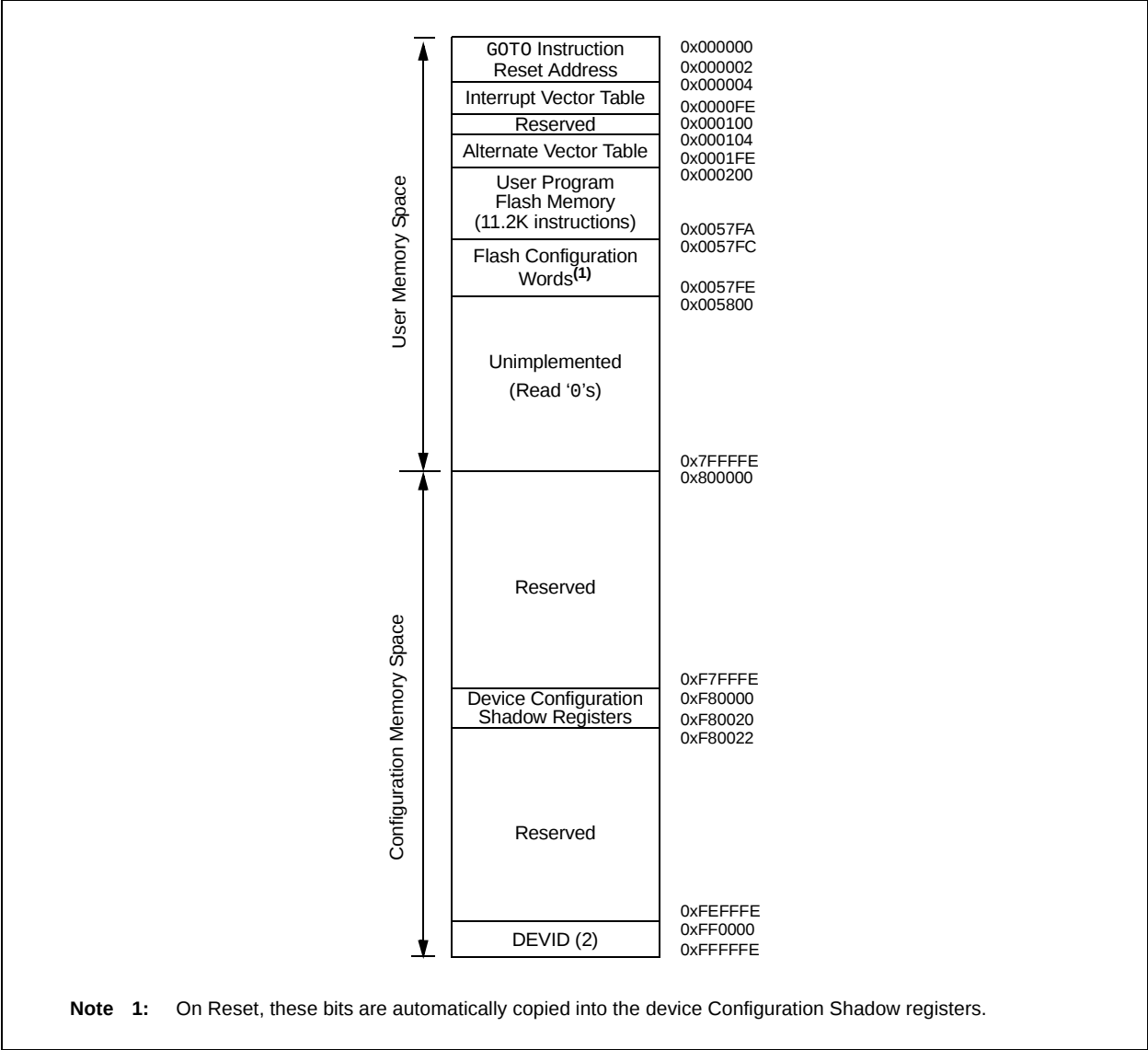


TABLE 4-1: CPU CORE REGISTER MAP (CONTINUED)

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets	
CORCON	0044	—	—	—	US	EDT	DL2	DL1	DL0	SATA	SATB	SATDW	ACCSAT	IPL3	PSV	RND	IF	0020	
MODCON	0046	XMODEN	YMODEN	—	—	BWM3	BWM2	BWM1	BWM0	YWM3	YWM2	YWM1	YWM0	XWM3	XWM2	XWM1	XWM0	0000	
XMODSRT	0048	XS<15:1>																0	xxxx
XMODEND	004A	XE<15:1>																1	xxxx
YMODSRT	004C	YS<15:1>																0	xxxx
YMODEND	004E	YE<15:1>																1	xxxx
XBREV	0050	BREN	XB<14:0>															xxxx	
DISICNT	0052	—	—	Disable Interrupts Counter Register														0000	

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

dsPIC33FJ16(GP/MC)101/102 AND dsPIC33FJ32(GP/MC)101/102/104

REGISTER 10-21: RPOR10: PERIPHERAL PIN SELECT OUTPUT REGISTER 10

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	RP21R<4:0> ⁽¹⁾				
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	RP20R<4:0> ⁽¹⁾				
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **RP21R<4:0>:** Peripheral Output Function is Assigned to RP21 Output Pin bits⁽¹⁾
(see Table 10-2 for peripheral function numbers)

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **RP20R<4:0>:** Peripheral Output Function is Assigned to RP20 Output Pin bits⁽¹⁾
(see Table 10-2 for peripheral function numbers)

Note 1: These bits are available in dsPIC33FJ32(GP/MC)104 devices only.

REGISTER 10-22: RPOR11: PERIPHERAL PIN SELECT OUTPUT REGISTER 11

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	RP23R<4:0> ⁽¹⁾				
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	RP22R<4:0> ⁽¹⁾				
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **RP23R<4:0>:** Peripheral Output Function is Assigned to RP23 Output Pin bits⁽¹⁾
(see Table 10-2 for peripheral function numbers)

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **RP22R<4:0>:** Peripheral Output Function is Assigned to RP22 Output Pin bits⁽¹⁾
(see Table 10-2 for peripheral function numbers)

Note 1: These bits are available in dsPIC33FJ32(GP/MC)104 devices only.

NOTES:

REGISTER 15-15: PWMxKEY: PWMx UNLOCK REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PWMKEY<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PWMKEY<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **PWMKEY<15:0>**: PWMx Unlock bits

If the PWMLOCK Configuration bit is asserted (PWMLOCK = 1), the PWMxCON1, PxFLTACON and PxFLTBCON registers are writable only after the proper sequence is written to the PWMxKEY register. If the PWMLOCK Configuration bit is deasserted (PWMLOCK = 0), the PWMxCON1, PxFLTACON and PxFLTBCON registers are writable at all times. Refer to **“Motor Control PWM”** (DS70187) in the *“dsPIC33/PIC24 Family Reference Manual”* for details on the unlock sequence.

REGISTER 17-2: I2CxSTAT: I2Cx STATUS REGISTER

R-0, HSC	R-0, HSC	U-0	U-0	U-0	R/C-0, HS	R-0, HSC	R-0, HSC
ACKSTAT	TRSTAT	—	—	—	BCL	GCSTAT	ADD10
bit 15						bit 8	

R/C-0, HS	R/C-0, HS	R-0, HSC	R/C-0, HSC	R/C-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC
IWCOL	I2COV	D_A	P	S	R_W	RBF	TBF
bit 7						bit 0	

Legend:	C = Clearable bit	HSC = Hardware Settable/Clearable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
HS = Hardware Settable bit		x = Bit is unknown

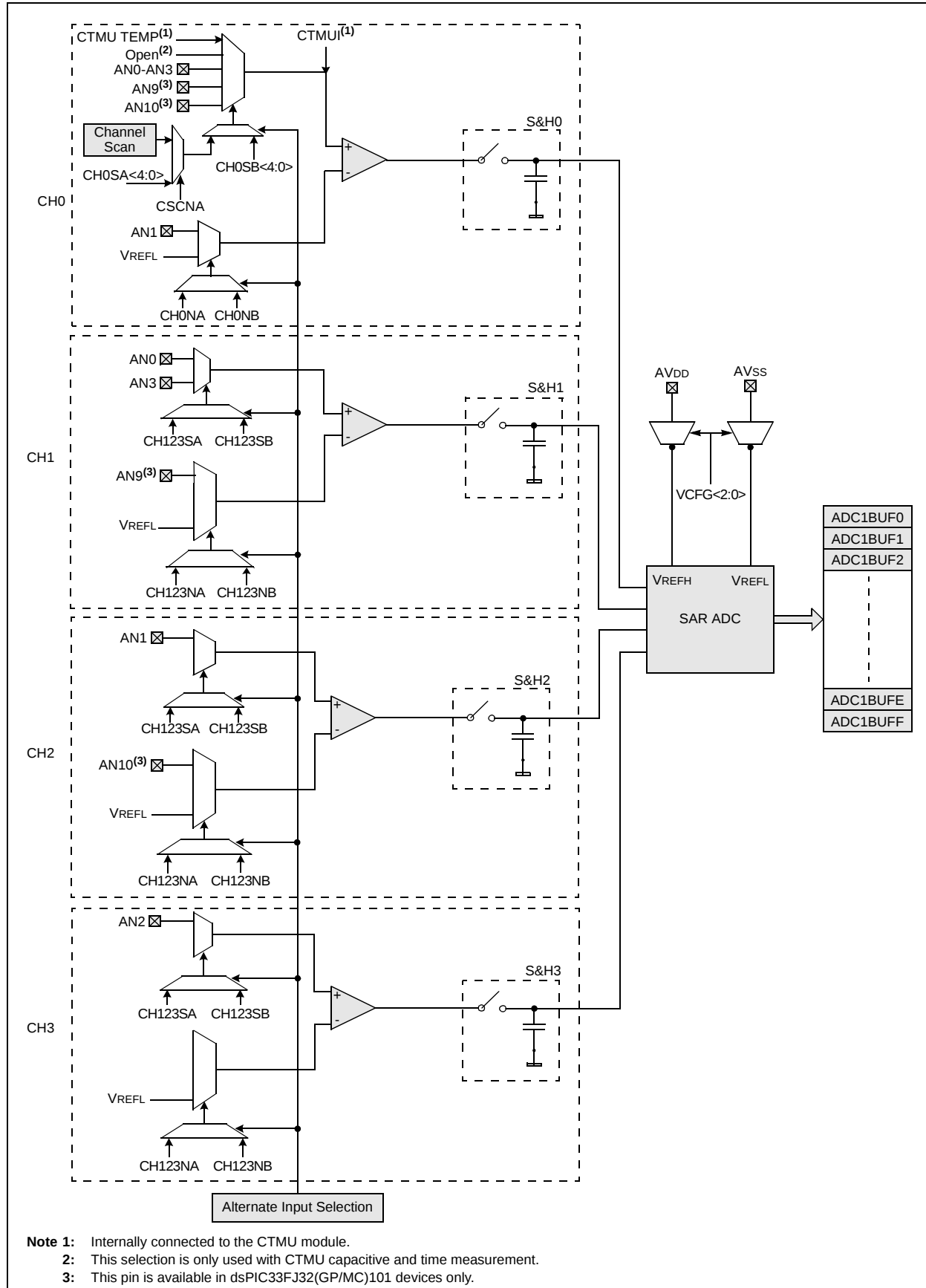
- bit 15 **ACKSTAT:** Acknowledge Status bit
(when operating as I²C™ master, applicable to master transmit operation)
1 = NACK received from slave
0 = ACK received from slave
Hardware sets or clears at end of slave Acknowledge.
- bit 14 **TRSTAT:** Transmit Status bit (when operating as I²C master, applicable to master transmit operation)
1 = Master transmit is in progress (8 bits + ACK)
0 = Master transmit is not in progress
Hardware sets at beginning of master transmission. Hardware clears at end of slave Acknowledge.
- bit 13-11 **Unimplemented:** Read as '0'
- bit 10 **BCL:** Master Bus Collision Detect bit
1 = A bus collision has been detected during a master operation
0 = No collision
Hardware sets at detection of bus collision.
- bit 9 **GCSTAT:** General Call Status bit
1 = General call address was received
0 = General call address was not received
Hardware sets when address matches general call address. Hardware clears at Stop detection.
- bit 8 **ADD10:** 10-Bit Address Status bit
1 = 10-bit address was matched
0 = 10-bit address was not matched
Hardware sets at match of 2nd byte of matched 10-bit address. Hardware clears at Stop detection.
- bit 7 **IWCOL:** Write Collision Detect bit
1 = An attempt to write to the I2CxTRN register failed because the I²C module is busy
0 = No collision
Hardware sets at occurrence of a write to I2CxTRN while busy (cleared by software).
- bit 6 **I2COV:** Receive Overflow Flag bit
1 = A byte was received while the I2CxRCV register is still holding the previous byte
0 = No overflow
Hardware sets at attempt to transfer I2CxRSR to I2CxRCV (cleared by software).
- bit 5 **D_A:** Data/Address bit (when operating as I²C slave)
1 = Indicates that the last byte received was data
0 = Indicates that the last byte received was a device address
Hardware clears at device address match. Hardware sets by reception of a slave byte.

REGISTER 18-2: UxSTA: UARTx STATUS AND CONTROL REGISTER (CONTINUED)

- bit 5 **ADDEN:** Address Character Detect bit (Bit 8 of received data = 1)
1 = Address Detect mode is enabled; if 9-bit mode is not selected, this does not take effect
0 = Address Detect mode is disabled
- bit 4 **RIDLE:** Receiver Idle bit (read-only)
1 = Receiver is Idle
0 = Receiver is active
- bit 3 **PERR:** Parity Error Status bit (read-only)
1 = Parity error has been detected for the current character (character at the top of the receive FIFO)
0 = Parity error has not been detected
- bit 2 **FERR:** Framing Error Status bit (read-only)
1 = Framing error has been detected for the current character (character at the top of the receive FIFO)
0 = Framing error has not been detected
- bit 1 **OERR:** Receive Buffer Overrun Error Status bit (read-only/clear only)
1 = Receive buffer has overflowed
0 = Receive buffer has not overflowed; clearing a previously set OERR bit (1 → 0 transition) will reset the receiver buffer and the UxRSR to the empty state
- bit 0 **URXDA:** UARTx Receive Buffer Data Available bit (read-only)
1 = Receive buffer has data, at least one more character can be read
0 = Receive buffer is empty

Note 1: Refer to “**UART**” (DS70188) in the “*dsPIC33/PIC24 Family Reference Manual*” for information on enabling the UART module for transmit operation.

FIGURE 19-1: ADC1 BLOCK DIAGRAM FOR dsPIC33FJXX(GP/MC)101 DEVICES



21.0 REAL-TIME CLOCK AND CALENDAR (RTCC)

Note 1: This data sheet summarizes the features of the dsPIC33FJ16(GP/MC)101/102 and dsPIC33FJ32(GP/MC)101/102/104 device families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**Real-Time Clock and Calendar (RTCC)**” (DS70310) in the “dsPIC33/PIC24 Family Reference Manual”, which is available on the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

This chapter discusses the Real-Time Clock and Calendar (RTCC) module, available on dsPIC33FJ16(GP/MC)101/102 and dsPIC33FJ32(GP/MC)101/102/104 devices, and its operation.

Some of the key features of the RTCC module are:

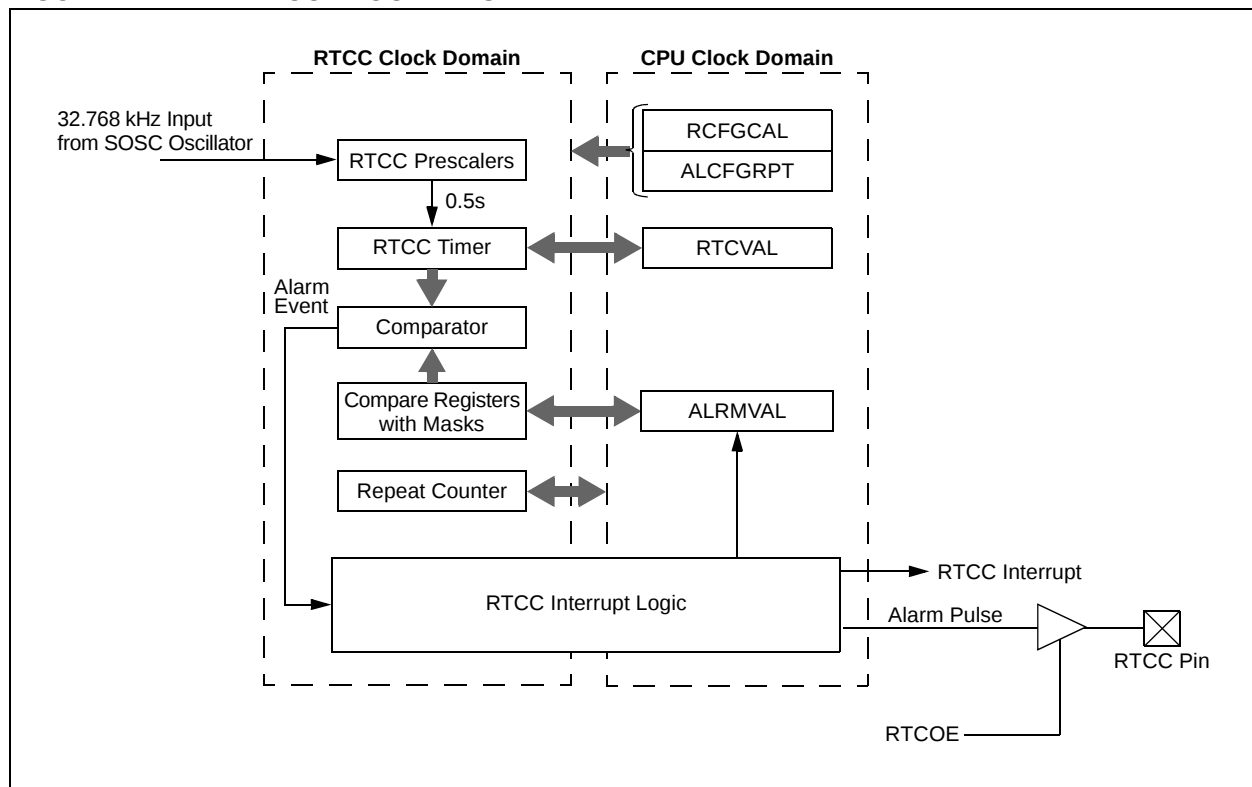
- Time: hours, minutes and seconds
- 24-hour format (military time)
- Calendar: weekday, date, month and year
- Alarm configurable
- Year range: 2000 to 2099
- Leap year correction
- BCD format for compact firmware
- Optimized for low-power operation
- User calibration with auto-adjust
- Calibration range: ± 2.64 seconds error per month
- Requirements: external 32.768 kHz clock crystal
- Alarm pulse or seconds clock output on RTCC pin

The RTCC module is intended for applications where accurate time must be maintained for extended periods of time with minimum to no intervention from the CPU. The RTCC module is optimized for low-power usage to provide extended battery lifetime while keeping track of time.

The RTCC module is a 100-year clock and calendar with automatic leap year detection. The range of the clock is from 00:00:00 (midnight) on January 1, 2000 to 23:59:59 on December 31, 2099.

The hours are available in 24-hour (military time) format. The clock provides a granularity of one second with half-second visibility to the user.

FIGURE 21-1: RTCC BLOCK DIAGRAM



dsPIC33FJ16(GP/MC)101/102 AND dsPIC33FJ32(GP/MC)101/102/104

REGISTER 21-4: RTCVAL (WHEN RTCPTR<1:0> = 11): RTCC YEAR VALUE REGISTER⁽¹⁾

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
YRTEN3	YRTEN2	YRTEN1	YRTEN0	YRONE3	YRONE2	YRONE1	YRONE0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-8 **Unimplemented:** Read as '0'
- bit 7-4 **YRTEN<3:0>:** Binary Coded Decimal Value of Year's Tens Digit bits
Contains a value from 0 to 9.
- bit 3-0 **YRONE<3:0>:** Binary Coded Decimal Value of Year's Ones Digit bits
Contains a value from 0 to 9.

Note 1: A write to this register is only allowed when RTCWREN = 1.

REGISTER 21-5: RTCVAL (WHEN RTCPTR<1:0> = 10): RTCC MONTH AND DAY VALUE REGISTER⁽¹⁾

U-0	U-0	U-0	R-x	R-x	R-x	R-x	R-x
—	—	—	MHTTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0
bit 15							bit 8

U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	DAYTEN1	DAYTEN0	DAYONE3	DAYONE2	DAYONE1	DAYONE0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-13 **Unimplemented:** Read as '0'
- bit 12 **MHTTEN0:** Binary Coded Decimal Value of Month's Tens Digit bit
Contains a value of 0 or 1.
- bit 11-8 **MTHONE<3:0>:** Binary Coded Decimal Value of Month's Ones Digit bits
Contains a value from 0 to 9.
- bit 7-6 **Unimplemented:** Read as '0'
- bit 5-4 **DAYTEN<1:0>:** Binary Coded Decimal Value of Day's Tens Digit bits
Contains a value from 0 to 3.
- bit 3-0 **DAYONE<3:0>:** Binary Coded Decimal Value of Day's Ones Digit bits
Contains a value from 0 to 9.

Note 1: A write to this register is only allowed when RTCWREN = 1.

dsPIC33FJ16(GP/MC)101/102 AND dsPIC33FJ32(GP/MC)101/102/104

REGISTER 21-10: ALRMVAL (WHEN ALRMPTR<1:0> = 00): ALARM MINUTES AND SECONDS VALUE REGISTER

U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0
bit 15							bit 8

U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	SECTEN2	SECTEN1	SECTEN0	SECONE3	SECONE2	SECONE1	SECONE0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **MINTEN<2:0>:** Binary Coded Decimal Value of Minute's Tens Digit bits
Contains a value from 0 to 5.

bit 11-8 **MINONE<3:0>:** Binary Coded Decimal Value of Minute's Ones Digit bits
Contains a value from 0 to 9.

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **SECTEN<2:0>:** Binary Coded Decimal Value of Second's Tens Digit bits
Contains a value from 0 to 5.

bit 3-0 **SECONE<3:0>:** Binary Coded Decimal Value of Second's Ones Digit bits
Contains a value from 0 to 9.

23.2 On-Chip Voltage Regulator

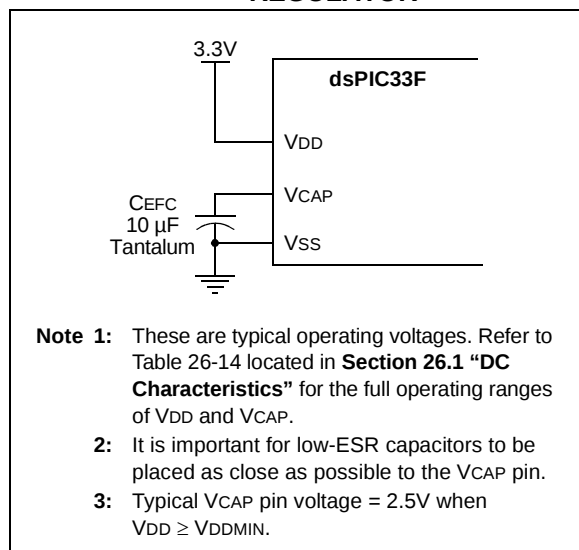
All of the dsPIC33FJ16(GP/MC)101/102 and dsPIC33FJ32(GP/MC)101/102/104 devices power their core digital logic at a nominal 2.5V. This can create a conflict for designs that are required to operate at a higher typical voltage, such as 3.3V. To simplify system design, all devices in the dsPIC33FJ16(GP/MC)101/102 and dsPIC33FJ32(GP/MC)101/102/104 family incorporate an on-chip regulator that allows the device to run its core logic from VDD.

The regulator provides power to the core from the other VDD pins. When the regulator is enabled, a low-ESR (less than 5 ohms) capacitor (such as tantalum or ceramic) must be connected to the VCAP pin (Figure 23-1). This helps to maintain the stability of the regulator. The recommended value for the filter capacitor is provided in Table 26-14 located in **Section 26.1 “DC Characteristics”**.

Note: It is important for low-ESR capacitors to be placed as close as possible to the VCAP pin.

On a POR, it takes approximately 20 μ s for the on-chip voltage regulator to generate an output voltage. During this time, designated as TSTARTUP, code execution is disabled. TSTARTUP is applied every time the device resumes operation after any power-down.

FIGURE 23-1: CONNECTIONS FOR THE ON-CHIP VOLTAGE REGULATOR^(1,2,3)



23.3 BOR: Brown-out Reset

The Brown-out Reset (BOR) module is based on an internal voltage reference circuit that monitors the regulated supply voltage, VCAP. The main purpose of the BOR module is to generate a device Reset when a brown-out condition occurs. Brown-out conditions are generally caused by glitches on the AC mains (for example, missing portions of the AC cycle waveform due to bad power transmission lines or voltage sags due to excessive current draw when a large inductive load is turned on).

A BOR generates a Reset pulse, which resets the device. The BOR selects the clock source, based on the device Configuration bit values (FNOSC<2:0> and POSCMD<1:0>).

If an Oscillator mode is selected, the BOR activates the Oscillator Start-up Timer (OST). The system clock is held until OST expires. If the PLL is used, the clock is held until the LOCK bit (OSCCON<5>) is '1'.

Concurrently, the PWRT Time-out (TPWRT) is applied before the internal Reset is released. If TPWRT = 0 and a crystal oscillator is being used, then a nominal delay of TFSCM = 100 is applied. The total delay in this case is TFSCM.

The BOR status bit (RCON<1>) is set to indicate that a BOR has occurred. The BOR circuit continues to operate while in Sleep or Idle modes and resets the device should VDD fall below the BOR threshold voltage.

TABLE 24-2: INSTRUCTION SET OVERVIEW

Base Instr #	Assembly Mnemonic	Assembly Syntax	Description	# of Words	# of Cycles	Status Flags Affected
1	ADD	ADD Acc	Add Accumulators	1	1	OA,OB,SA,SB
		ADD f	$f = f + \text{WREG}$	1	1	C,DC,N,OV,Z
		ADD f, WREG	$\text{WREG} = f + \text{WREG}$	1	1	C,DC,N,OV,Z
		ADD #lit10, Wn	$\text{Wd} = \text{lit10} + \text{Wd}$	1	1	C,DC,N,OV,Z
		ADD Wb, Ws, Wd	$\text{Wd} = \text{Wb} + \text{Ws}$	1	1	C,DC,N,OV,Z
		ADD Wb, #lit5, Wd	$\text{Wd} = \text{Wb} + \text{lit5}$	1	1	C,DC,N,OV,Z
		ADD Wso, #Slit4, Acc	16-bit Signed Add to Accumulator	1	1	OA,OB,SA,SB
2	ADDC	ADDC f	$f = f + \text{WREG} + (C)$	1	1	C,DC,N,OV,Z
		ADDC f, WREG	$\text{WREG} = f + \text{WREG} + (C)$	1	1	C,DC,N,OV,Z
		ADDC #lit10, Wn	$\text{Wd} = \text{lit10} + \text{Wd} + (C)$	1	1	C,DC,N,OV,Z
		ADDC Wb, Ws, Wd	$\text{Wd} = \text{Wb} + \text{Ws} + (C)$	1	1	C,DC,N,OV,Z
		ADDC Wb, #lit5, Wd	$\text{Wd} = \text{Wb} + \text{lit5} + (C)$	1	1	C,DC,N,OV,Z
3	AND	AND f	$f = f \text{ .AND. } \text{WREG}$	1	1	N,Z
		AND f, WREG	$\text{WREG} = f \text{ .AND. } \text{WREG}$	1	1	N,Z
		AND #lit10, Wn	$\text{Wd} = \text{lit10} \text{ .AND. } \text{Wd}$	1	1	N,Z
		AND Wb, Ws, Wd	$\text{Wd} = \text{Wb} \text{ .AND. } \text{Ws}$	1	1	N,Z
		AND Wb, #lit5, Wd	$\text{Wd} = \text{Wb} \text{ .AND. } \text{lit5}$	1	1	N,Z
4	ASR	ASR f	$f = \text{Arithmetic Right Shift } f$	1	1	C,N,OV,Z
		ASR f, WREG	$\text{WREG} = \text{Arithmetic Right Shift } f$	1	1	C,N,OV,Z
		ASR Ws, Wd	$\text{Wd} = \text{Arithmetic Right Shift } \text{Ws}$	1	1	C,N,OV,Z
		ASR Wb, Wns, Wnd	$\text{Wnd} = \text{Arithmetic Right Shift } \text{Wb by } \text{Wns}$	1	1	N,Z
		ASR Wb, #lit5, Wnd	$\text{Wnd} = \text{Arithmetic Right Shift } \text{Wb by } \text{lit5}$	1	1	N,Z
5	BCLR	BCLR f, #bit4	Bit Clear f	1	1	None
		BCLR Ws, #bit4	Bit Clear Ws	1	1	None
6	BRA	BRA C, Expr	Branch if Carry	1	1 (2)	None
		BRA GE, Expr	Branch if greater than or equal	1	1 (2)	None
		BRA GEU, Expr	Branch if unsigned greater than or equal	1	1 (2)	None
		BRA GT, Expr	Branch if greater than	1	1 (2)	None
		BRA GTU, Expr	Branch if unsigned greater than	1	1 (2)	None
		BRA LE, Expr	Branch if less than or equal	1	1 (2)	None
		BRA LEU, Expr	Branch if unsigned less than or equal	1	1 (2)	None
		BRA LT, Expr	Branch if less than	1	1 (2)	None
		BRA LTU, Expr	Branch if unsigned less than	1	1 (2)	None
		BRA N, Expr	Branch if Negative	1	1 (2)	None
		BRA NC, Expr	Branch if Not Carry	1	1 (2)	None
		BRA NN, Expr	Branch if Not Negative	1	1 (2)	None
		BRA NOV, Expr	Branch if Not Overflow	1	1 (2)	None
		BRA NZ, Expr	Branch if Not Zero	1	1 (2)	None
		BRA OA, Expr	Branch if Accumulator A overflow	1	1 (2)	None
		BRA OB, Expr	Branch if Accumulator B overflow	1	1 (2)	None
		BRA OV, Expr	Branch if Overflow	1	1 (2)	None
		BRA SA, Expr	Branch if Accumulator A saturated	1	1 (2)	None
		BRA SB, Expr	Branch if Accumulator B saturated	1	1 (2)	None
		BRA Expr	Branch Unconditionally	1	2	None
		BRA Z, Expr	Branch if Zero	1	1 (2)	None
		BRA Wn	Computed Branch	1	2	None
7	BSET	BSET f, #bit4	Bit Set f	1	1	None
		BSET Ws, #bit4	Bit Set Ws	1	1	None
8	BSW	BSW.C Ws, Wb	Write C bit to Ws<Wb>	1	1	None
		BSW.Z Ws, Wb	Write Z bit to Ws<Wb>	1	1	None

FIGURE 26-2: EXTERNAL CLOCK TIMING

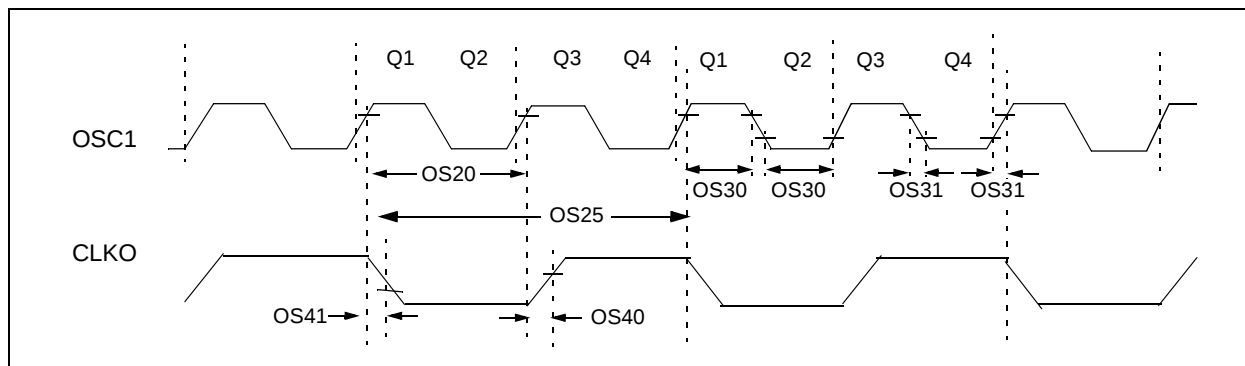


TABLE 26-16: EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symb	Characteristic	Min	Typ ⁽¹⁾	Max	Units	Conditions
OS10	FIN	External CLKI Frequency (External clocks allowed only in EC and ECPLL modes)	DC	—	32	MHz	EC
		Oscillator Crystal Frequency	3.0	—	10	MHz	MS
			10	—	32	MHz	HS
			31	—	33	kHz	SOSC
OS20	Tosc	Tosc = 1/Fosc	31.25	—	DC	ns	
OS25	Tcy	Instruction Cycle Time ^(2,4)	62.5	—	DC	ns	
OS30	TosL, TosH	External Clock in (OSC1) ⁽⁵⁾ High or Low Time	0.45 x Tosc	—	—	ns	EC
OS31	TosR, TosF	External Clock in (OSC1) ⁽⁵⁾ Rise or Fall Time	—	—	20	ns	EC
OS40	TckR	CLKO Rise Time ^(3,5)	—	6	10	ns	
OS41	TckF	CLKO Fall Time ^(3,5)	—	6	10	ns	
OS42	GM	External Oscillator Transconductance ⁽⁴⁾	14	16	18	mA/V	VDD = 3.3V, TA = +25°C

Note 1: Data in “Typ” column is at 3.3V, +25°C unless otherwise stated.

2: Instruction cycle period (Tcy) equals two times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type, under standard operating conditions, with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at “min.” values with an external clock applied to the OSC1/CLKI pin. When an external clock input is used, the “max.” cycle time limit is “DC” (no clock) for all devices.

3: Measurements are taken in EC mode. The CLKO signal is measured on the OSC2 pin.

4: These parameters are characterized by similarity, but are tested in manufacturing at FIN = 32 MHz only.

5: These parameters are characterized by similarity, but are not tested in manufacturing.

FIGURE 26-21: SPIx MASTER MODE (FULL-DUPLEX, CKE = 1, CKP = x, SMP = 1) TIMING CHARACTERISTICS FOR dsPIC33FJ32(GP/MC)10X

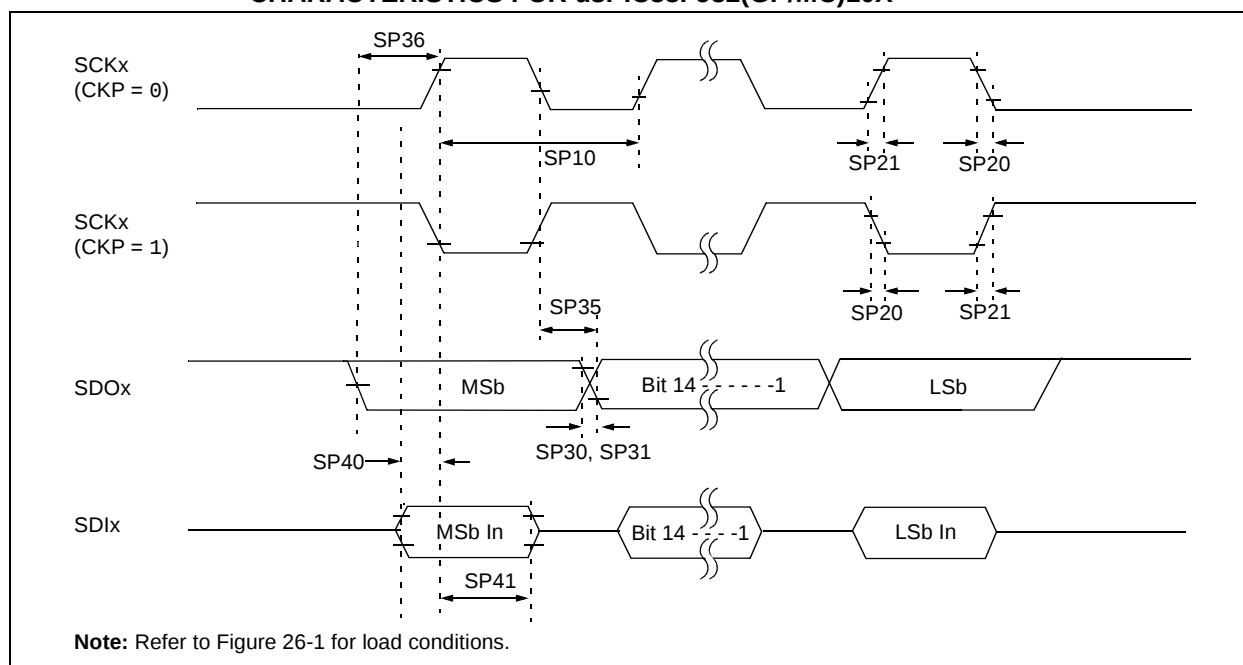


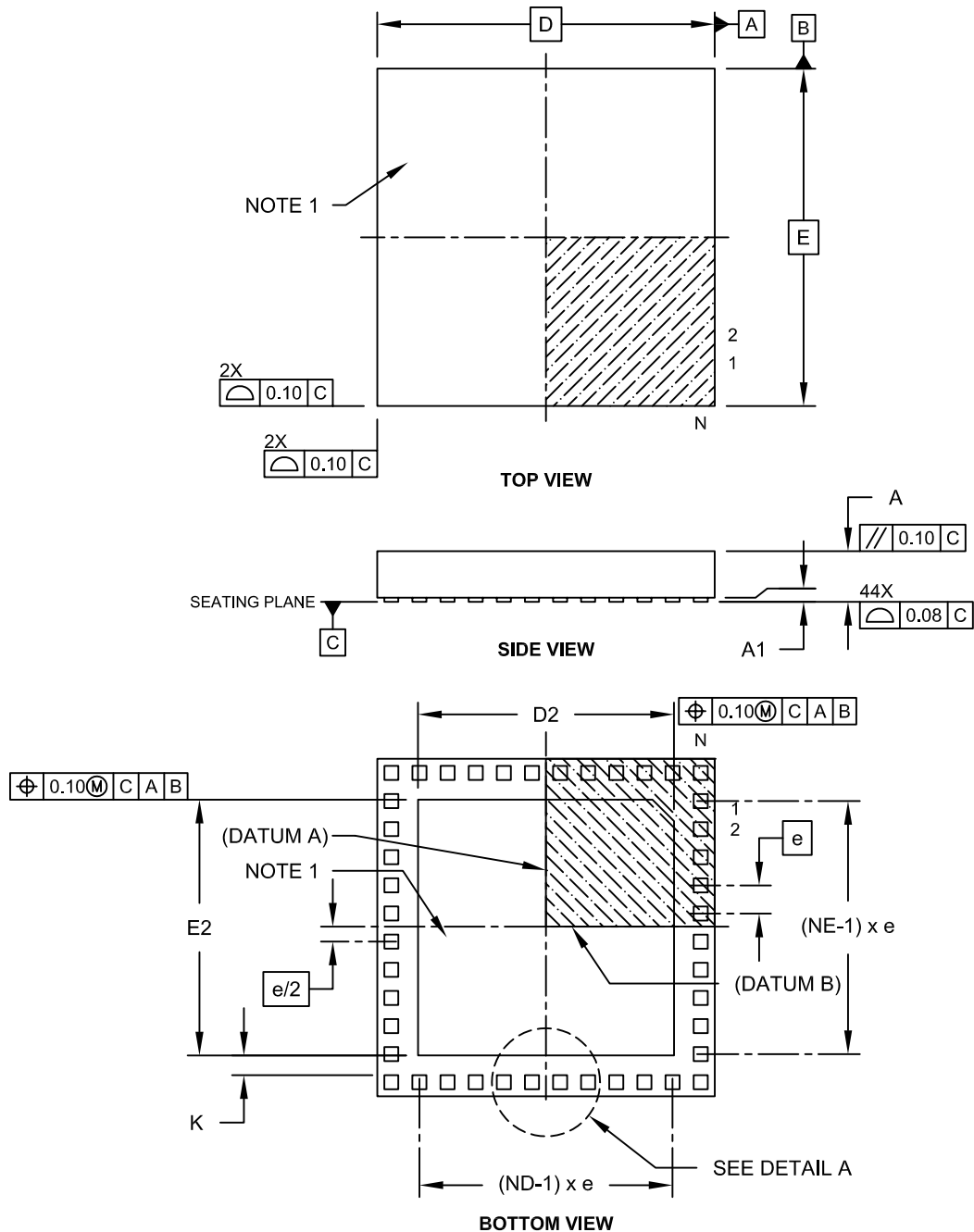
TABLE 26-39: SPIx MASTER MODE (FULL-DUPLEX, CKE = 1, CKP = x, SMP = 1) TIMING REQUIREMENTS FOR dsPIC33FJ32(GP/MC)10X

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic ⁽¹⁾	Min	Typ ⁽²⁾	Max	Units	Conditions
SP10	TscP	Maximum SCKx Frequency	—	—	9	MHz	See Note 3
SP20	TscF	SCKx Output Fall Time	—	—	—	ns	See Parameter DO32 and Note 4
SP21	TscR	SCKx Output Rise Time	—	—	—	ns	See Parameter DO31 and Note 4
SP30	TdoF	SDOx Data Output Fall Time	—	—	—	ns	See Parameter DO32 and Note 4
SP31	TdoR	SDOx Data Output Rise Time	—	—	—	ns	See Parameter DO31 and Note 4
SP35	Tsch2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	6	20	ns	
SP36	TdoV2sc, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	—	—	ns	
SP40	TdiV2sch, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	—	—	ns	
SP41	Tsch2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	—	—	ns	

- Note 1:** These parameters are characterized, but are not tested in manufacturing.
Note 2: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.
Note 3: The minimum clock period for SCKx is 111 ns. The clock generated in Master mode must not violate this specification.
Note 4: Assumes 50 pF load on all SPIx pins.

**44-Terminal Very Thin Leadless Array Package (TL) – 6x6x0.9 mm Body
With Exposed Pad [VTLA]**

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-157C Sheet 1 of 2

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