Microchip Technology - DSPIC33FJ32GP101-E/SS Datasheet

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Details	
Product Status	Obsolete
Core Processor	dsPIC
Core Size	16-Bit
Speed	16 MIPs
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	15
Program Memory Size	32KB (11K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj32gp101-e-ss

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Referenced Sources

This device data sheet is based on the following individual chapters of the *"dsPIC33/PIC24 Family Reference Manual"*. These documents should be considered as the primary reference for the operation of a particular module or device feature.

Note 1: To access the documents listed below, browse to the documentation section of the dsPIC33FJ16MC102 product page of the Microchip Web site (www.microchip.com).

In addition to parameters, features and other documentation, the resulting page provides links to the related family reference manual sections.

- **"CPU"** (DS70204)
- **"Data Memory"** (DS70202)
- **"Program Memory"** (DS70203)
- **"Flash Programming"** (DS70191)
- **"Reset"** (DS70192)
- **"Watchdog Timer and Power-Saving Modes"** (DS70196)
- **"Timers"** (DS70205)
- **"Input Capture"** (DS70198)
- **"Output Compare"** (DS70209)
- **"Motor Control PWM"** (DS70187)
- **"Analog-to-Digital Converter (ADC)"** (DS70183)
- **"UART"** (DS70188)
- **"Serial Peripheral Interface (SPI)"** (DS70206)
- **"Inter-Integrated Circuit™ (I^2C™)"** (DS70195)
- **"CodeGuard Security"** (DS70199)
- **"Programming and Diagnostics"** (DS70207)
- **"Device Configuration"** (DS70194)
- **"I/O Ports with Peripheral Pin Select (PPS)"** (DS70190)
- **"Real-Time Clock and Calendar (RTCC)"** (DS70301)
- **"Introduction (Part VI)"** (DS70655)
- **"Oscillator (Part VI)"** (DS70644)
- **"Interrupts (Part VI)"** (DS70633)
- **"Comparator with Blanking"** (DS70647)
- **"Charge Time Measurement Unit (CTMU)"** (DS70635)

NOTES:

3.4 CPU Control Registers

REGISTER 3-1: SR: CPU STATUS REGISTER

R-0	R-0	R/C-0	R/C-0	R-0	R/C-0	R-0	R/W-0
OA	OB	SA(1)	SB(1)	OAB	SAB	DA	DC
bit 15							bit 8

R/W-0(3)	R/W-0(3)	R/W-0(3)	R-0	R/W-0	R/W-0	R/W-0	R/W-0
IPL2(2)	IPL1(2)	IPL0(2)	RA	N	OV	Z	C
bit 7							bit 0

Legend:	C = Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **OA:** Accumulator A Overflow Status bit
1 = Accumulator A has overflowed
0 = Accumulator A has not overflowed

bit 14 **OB:** Accumulator B Overflow Status bit
1 = Accumulator B has overflowed
0 = Accumulator B has not overflowed

bit 13 **SA:** Accumulator A Saturation 'Sticky' Status bit(1)
1 = Accumulator A is saturated or has been saturated at some time
0 = Accumulator A is not saturated

bit 12 **SB:** Accumulator B Saturation 'Sticky' Status bit(1)
1 = Accumulator B is saturated or has been saturated at some time
0 = Accumulator B is not saturated

bit 11 **OAB:** OA || OB Combined Accumulator Overflow Status bit
1 = Accumulators A or B have overflowed
0 = Neither Accumulators A or B have overflowed

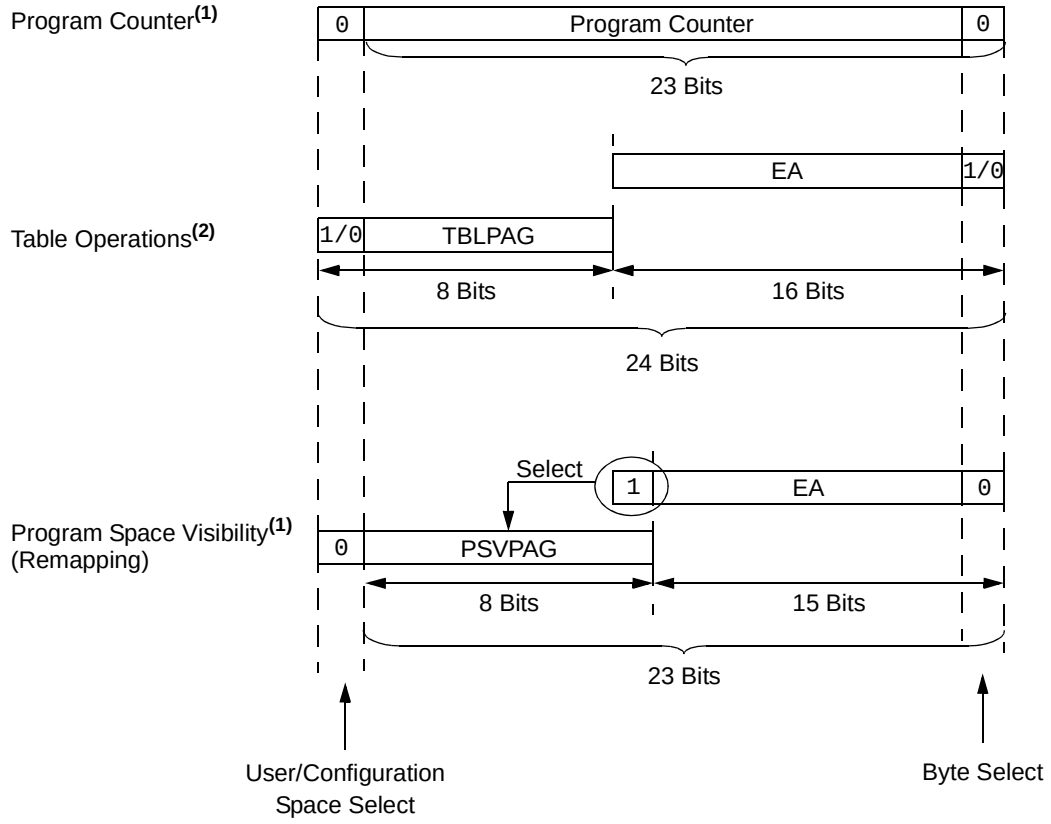
bit 10 **SAB:** SA || SB Combined Accumulator 'Sticky' Status bit
1 = Accumulators A or B are saturated or have been saturated at some time in the past
0 = Neither Accumulator A or B are saturated
This bit may be read or cleared (not set). *Clearing this bit will clear SA and SB*.

bit 9 **DA:** DO Loop Active bit
1 = DO loop is in progress
0 = DO loop is not in progress

bit 8 **DC:** MCU ALU Half Carry/$\overline{\text{Borrow}}$ bit
1 = A carry-out from the 4th low-order bit (for byte-sized data) or 8th low-order bit (for word-sized data) of the result occurred
0 = No carry-out from the 4th low-order bit (for byte-sized data) or 8th low-order bit (for word-sized data) of the result occurred

Note 1: This bit can be read or cleared (not set).
2: The IPL<2:0> bits are concatenated with the IPL<3> bit (CORCON<3>) to form the CPU Interrupt Priority Level. The value in parentheses indicates the IPL if IPL<3> = 1. User interrupts are disabled when IPL<3> = 1.
3: The IPL<2:0> Status bits are read-only when NSTDIS = 1 (INTCON1<15>).

FIGURE 4-9: DATA ACCESS FROM PROGRAM SPACE ADDRESS GENERATION



Note 1: The Least Significant bit of program space addresses is always fixed as '0' to maintain word alignment of data in the program and data spaces.

2: Table operations are not required to be word-aligned. Table read operations are permitted in the configuration memory space.

REGISTER 7-7: IFS2: INTERRUPT FLAG STATUS REGISTER 2

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
—	—	IC3IF	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-6 **Unimplemented:** Read as '0'

bit 5 **IC3IF:** Input Capture Channel 3 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 4-0 **Unimplemented:** Read as '0'

REGISTER 7-8: IFS3: INTERRUPT FLAG STATUS REGISTER 3

R/W-0	R/W-0	U-0	U-0	U-0	U-0	R/W-0	U-0
FLTA1IF(1)	RTCIF	—	—	—	—	PWM1IF(1)	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **FLTA1IF:** PWM1 Fault A Interrupt Flag Status bit(1)
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 14 **RTCIF:** RTCC Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 13-10 **Unimplemented:** Read as '0'

bit 9 **PWM1IF:** PWM1 Interrupt Flag Status bit(1)
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 8-0 **Unimplemented:** Read as '0'

Note 1: These bits are available in dsPIC(16/32)MC10X devices only.

REGISTER 10-5: RPINR7: PERIPHERAL PIN SELECT INPUT REGISTER 7

U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	—	IC2R4	IC2R3	IC2R2	IC2R1	IC2R0
bit 15							bit 8

U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	—	IC1R4	IC1R3	IC1R2	IC1R1	IC1R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **IC2R<4:0>:** Assign Input Capture 2 (IC2) to the Corresponding RPn Pin bits

11111 = Input tied to Vss
11110 = Reserved
.
.
.
11010 = Reserved
11001 = Input tied to RP25
.
.
.
00001 = Input tied to RP1
00000 = Input tied to RP0

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **IC1R<4:0>:** Assign Input Capture 1 (IC1) to the Corresponding RPn Pin bits

11111 = Input tied to Vss
11110 = Reserved
.
.
.
11010 = Reserved
11001 = Input tied to RP25
.
.
.
00001 = Input tied to RP1
00000 = Input tied to RP0

REGISTER 10-6: RPINR8: PERIPHERAL PIN SELECT INPUT REGISTER 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	—	IC3R4	IC3R3	IC3R2	IC3R1	IC3R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-5 **Unimplemented:** Read as ‘0’

bit 4-0 **IC3R<4:0>:** Assign Input Capture 3 (IC3) to the Corresponding RPn Pin bits

11111 = Input tied to Vss
11110 = Reserved
.
.
.
11010 = Reserved
11001 = Input tied to RP25
.
.
.
00001 = Input tied to RP1
00000 = Input tied to RP0

REGISTER 10-13: RPOR2: PERIPHERAL PIN SELECT OUTPUT REGISTER 2

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	RP5R<4:0>(1)				
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	RP4R<4:0>				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **RP5R<4:0>:** Peripheral Output Function is Assigned to RP5 Output Pin bits(1)
(see Table 10-2 for peripheral function numbers)

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **RP4R<4:0>:** Peripheral Output Function is Assigned to RP4 Output Pin bits
(see Table 10-2 for peripheral function numbers)

Note 1: These bits are not available in dsPIC33FJ(16/32)(GP/MC)101 devices.

REGISTER 10-14: RPOR3: PERIPHERAL PIN SELECT OUTPUT REGISTER 3

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	RP7R<4:0>				
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	RP6R<4:0>(1)				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **RP7R<4:0>:** Peripheral Output Function is Assigned to RP7 Output Pin bits
(see Table 10-2 for peripheral function numbers)

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **RP6R<4:0>:** Peripheral Output Function is Assigned to RP6 Output Pin bits(1)
(see Table 10-2 for peripheral function numbers)

Note 1: These bits are not available in dsPIC33FJ(16/32)(GP/MC)101 devices.

REGISTER 10-21: RPOR10: PERIPHERAL PIN SELECT OUTPUT REGISTER 10

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	RP21R<4:0>(1)				
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	RP20R<4:0>(1)				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **RP21R<4:0>:** Peripheral Output Function is Assigned to RP21 Output Pin bits(1)
(see Table 10-2 for peripheral function numbers)

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **RP20R<4:0>:** Peripheral Output Function is Assigned to RP20 Output Pin bits(1)
(see Table 10-2 for peripheral function numbers)

Note 1: These bits are available in dsPIC33FJ32(GP/MC)104 devices only.

REGISTER 10-22: RPOR11: PERIPHERAL PIN SELECT OUTPUT REGISTER 11

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	RP23R<4:0>(1)				
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	RP22R<4:0>(1)				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **RP23R<4:0>:** Peripheral Output Function is Assigned to RP23 Output Pin bits(1)
(see Table 10-2 for peripheral function numbers)

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **RP22R<4:0>:** Peripheral Output Function is Assigned to RP22 Output Pin bits(1)
(see Table 10-2 for peripheral function numbers)

Note 1: These bits are available in dsPIC33FJ32(GP/MC)104 devices only.

REGISTER 15-7: PxDTCON1: PWMx DEAD-TIME CONTROL REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DTBPS1	DTBPS0	DTB5	DTB4	DTB3	DTB2	DTB1	DTB0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DTAPS1	DTAPS0	DTA5	DTA4	DTA3	DTA2	DTA1	DTA0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **DTBPS<1:0>:** Dead-Time Unit B Prescale Select bits
11 = Clock period for Dead-Time Unit B is 8 TCY
10 = Clock period for Dead-Time Unit B is 4 TCY
01 = Clock period for Dead-Time Unit B is 2 TCY
00 = Clock period for Dead-Time Unit B is TCY

bit 13-8 **DTB<5:0>:** Unsigned 6-Bit Dead-Time Value for Dead-Time Unit B bits

bit 7-6 **DTAPS<1:0>:** Dead-Time Unit A Prescale Select bits
11 = Clock period for Dead-Time Unit A is 8 TCY
10 = Clock period for Dead-Time Unit A is 4 TCY
01 = Clock period for Dead-Time Unit A is 2 TCY
00 = Clock period for Dead-Time Unit A is TCY

bit 5-0 **DTA<5:0>:** Unsigned 6-Bit Dead-Time Value for Dead-Time Unit A bits

16.0 SERIAL PERIPHERAL INTERFACE (SPI)

Note 1: This data sheet summarizes the features of the dsPIC33FJ16(GP/MC)101/102 and dsPIC33FJ32(GP/MC)101/102/104 family devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Serial Peripheral Interface (SPI)"** (DS70206) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The Serial Peripheral Interface (SPI) module is a synchronous serial interface useful for communicating with other peripheral or microcontroller devices. These peripheral devices can be serial EEPROMs, shift registers, display drivers, Analog-to-Digital Converters, etc. The SPI module is compatible with SPI and SIOP from Motorola®.

Each SPI module consists of a 16-bit shift register, SPIxSR (where x = 1 or 2), used for shifting data in and out, and a buffer register, SPIxBUF. A control register, SPIxCON, configures the module. Additionally, a status register, SPIxSTAT, indicates status conditions.

The serial interface consists of four pins:

- SDIx (serial data input)
- SDOx (serial data output)
- SCKx (shift clock input or output)
- $\overline{SSx}$ (active-low slave select).

In Master mode operation, SCKx is a clock output. In Slave mode, it is a clock input.

FIGURE 16-1: SPIx MODULE BLOCK DIAGRAM

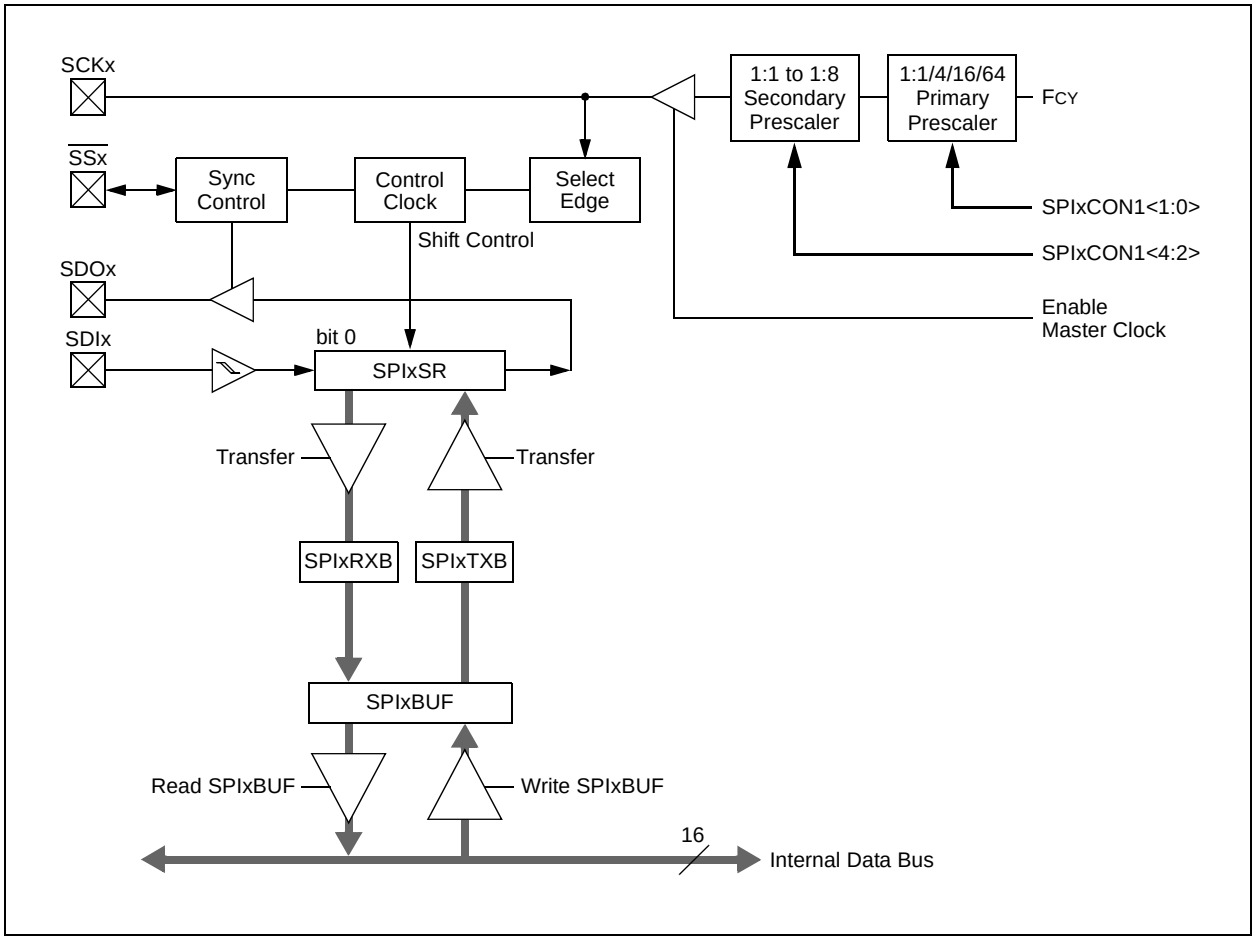
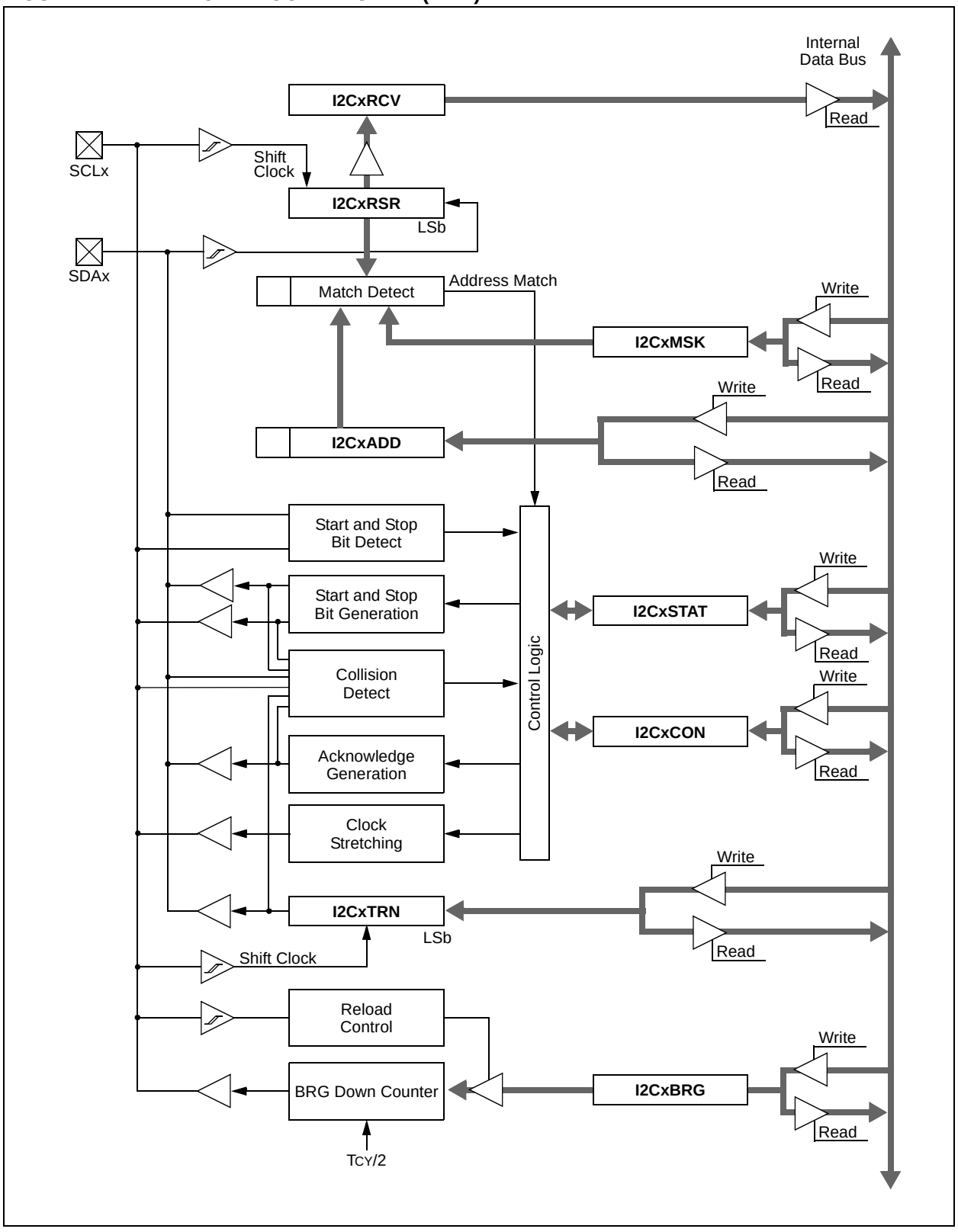


FIGURE 17-1: I²C™ BLOCK DIAGRAM (x = 1)



REGISTER 18-1: UxMODE: UARTx MODE REGISTER (CONTINUED)

bit 4 **URXINV:** UARTx Receive Polarity Inversion bit
1 = UxRX Idle state is '0'
0 = UxRX Idle state is '1'

bit 3 **BRGH:** High Baud Rate Enable bit
1 = BRG generates 4 clocks per bit period (4x baud clock, High-Speed mode)
0 = BRG generates 16 clocks per bit period (16x baud clock, Standard mode)

bit 2-1 **PDSEL<1:0>:** Parity and Data Selection bits
11 = 9-bit data, no parity
10 = 8-bit data, odd parity
01 = 8-bit data, even parity
00 = 8-bit data, no parity

bit 0 **STSEL:** Stop Bit Selection bit
1 = Two Stop bits
0 = One Stop bit

Note 1: Refer to **"UART"** (DS70188) in the *"dsPIC33/PIC24 Family Reference Manual"* for information on enabling the UART module for receive or transmit operation.

2: This feature is available for 16x BRG mode (BRGH = 0) only.

TABLE 23-4: dsPIC33F CONFIGURATION BITS DESCRIPTION (CONTINUED)

Bit Field	Description
WDTPRE	Watchdog Timer Prescaler bit 1 = 1:128 0 = 1:32
WDTPOST<3:0>	Watchdog Timer Postscaler bits 1111 = 1:32,768 1110 = 1:16,384 • • • 0001 = 1:2 0000 = 1:1
PLLKEN	PLL Lock Enable bit 1 = Clock switch to PLL will wait until the PLL lock signal is valid 0 = Clock switch will not wait for the PLL lock signal
ALTI2C	Alternate I^2C™ Pins bit 1 = I^2C is mapped to SDA1/SCL1 pins 0 = I^2C is mapped to ASDA1/ASCL1 pins
ICS<1:0>	ICD Communication Channel Select bits 11 = Communicate on PGEC1 and PGED1 10 = Communicate on PGEC2 and PGED2 01 = Communicate on PGEC3 and PGED3 00 = Reserved, do not use
PWMPIN	Motor Control PWM Module Pin Mode bit 1 = PWM module pins controlled by PORT register at device Reset (tri-stated) 0 = PWM module pins controlled by PWM module at device Reset (configured as output pins)
HPOL	Motor Control PWM High Side Polarity bit 1 = PWM module high side output pins have active-high output polarity 0 = PWM module high side output pins have active-low output polarity
LPOL	Motor Control PWM Low Side Polarity bit 1 = PWM module low side output pins have active-high output polarity 0 = PWM module low side output pins have active-low output polarity

REGISTER 23-1: DEVID: DEVICE ID REGISTER

R	R	R	R	R	R	R	R
DEVID<23:16>(1)							
bit 23							bit 16

R	R	R	R	R	R	R	R
DEVID<15:8>(1)							
bit 15							bit 8

R	R	R	R	R	R	R	R
DEVID<7:0>(1)							
bit 7							bit 0

Legend:	R = Read-Only bit	U = Unimplemented bit

bit 23-0 **DEIDV<23:0>:** Device Identifier bits(1)

Note 1: Refer to the *"dsPIC33F Flash Programming Specification for Devices with Volatile Configuration Bits"* (DS70659) for the list of device ID values.

REGISTER 23-2: DEVREV: DEVICE REVISION REGISTER

R	R	R	R	R	R	R	R
DEVREV<23:16>(1)							
bit 23							bit 16

R	R	R	R	R	R	R	R
DEVREV<15:8>(1)							
bit 15							bit 8

R	R	R	R	R	R	R	R
DEVREV<7:0>(1)							
bit 7							bit 0

Legend:	R = Read-only bit	U = Unimplemented bit

bit 23-0 **DEVREV<23:0>:** Device Revision bits(1)

Note 1: Refer to the *"dsPIC33F Flash Programming Specification for Devices with Volatile Configuration Bits"* (DS70659) for the list of device revision values.

24.0 INSTRUCTION SET SUMMARY

Note: This data sheet summarizes the features of the dsPIC33FJ16(GP/MC)101/102 and dsPIC33FJ32(GP/MC)101/102/104 devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the latest family reference sections of the *"dsPIC33/PIC24 Family Reference Manual"*, which are available from the Microchip web site (www.microchip.com).

The dsPIC33F instruction set is identical to that of the dsPIC30F.

Most instructions are a single program memory word (24 bits). Only three instructions require two program memory locations.

Each single-word instruction is a 24-bit word, divided into an 8-bit opcode, which specifies the instruction type and one or more operands, which further specify the operation of the instruction.

The instruction set is highly orthogonal and is grouped into five basic categories:

- Word or byte-oriented operations
- Bit-oriented operations
- Literal operations
- DSP operations
- Control operations

Table 24-1 shows the general symbols used in describing the instructions.

The dsPIC33F instruction set summary in Table 24-2 lists all the instructions, along with the status flags affected by each instruction.

Most word or byte-oriented W register instructions (including barrel shift instructions) have three operands:

- The first source operand, which is typically a register 'Wb' without any address modifier
- The second source operand, which is typically a register 'Ws' with or without an address modifier
- The destination of the result, which is typically a register 'Wd' with or without an address modifier

However, word or byte-oriented file register instructions have two operands:

- The file register specified by the value 'f'
- The destination, which could be either the file register 'f' or the W0 register, which is denoted as 'WREG'

Most bit-oriented instructions (including simple rotate/shift instructions) have two operands:

- The W register (with or without an address modifier) or file register (specified by the value of 'Ws' or 'f')
- The bit in the W register or file register (specified by a literal value or indirectly by the contents of register 'Wb')

The literal instructions that involve data movement can use some of the following operands:

- A literal value to be loaded into a W register or file register (specified by 'k')
- The W register or file register where the literal value is to be loaded (specified by 'Wb' or 'f')

However, literal instructions that involve arithmetic or logical operations use some of the following operands:

- The first source operand, which is a register 'Wb' without any address modifier
- The second source operand, which is a literal value
- The destination of the result (only if not the same as the first source operand), which is typically a register 'Wd' with or without an address modifier

The MAC class of DSP instructions can use some of the following operands:

- The accumulator (A or B) to be used (required operand)
- The W registers to be used as the two operands
- The X and Y address space prefetch operations
- The X and Y address space prefetch destinations
- The accumulator write-back destination

The other DSP instructions do not involve any multiplication and can include:

- The accumulator to be used (required)
- The source or destination operand (designated as Wso or Wdo, respectively) with or without an address modifier
- The amount of shift specified by a W register 'Wn' or a literal value

The control instructions can use some of the following operands:

- A program memory address
- The mode of the Table Read and Table Write instructions

TABLE 26-33: SPIx SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0) TIMING REQUIREMENTS FOR dsPIC33FJ16(GP/MC)10X

AC CHARACTERISTICS			Standard Operating Conditions: 2.4V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic(1)**	**Min**	**Typ(2)**	**Max**	**Units**	**Conditions**
SP70	TscP	Maximum SCKx Input Frequency	—	—	15	MHz	See **Note 3**
SP72	TscF	SCKx Input Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP73	TscR	SCKx Input Rise Time	—	—	—	ns	See Parameter DO31 and **Note 4**
SP30	TdoF	SDOx Data Output Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP31	TdoR	SDOx Data Output Rise Time	—	—	—	ns	See Parameter DO31 and **Note 4**
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SSx}$ ↓ to SCKx ↑ or SCKx Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{SSx}$ ↑ to SDOx Output High-Impedance	10	—	50	ns	See **Note 4**
SP52	TscH2ssH TscL2ssH	$\overline{SSx}$ after SCKx Edge	1.5 TCY + 40	—	—	ns	See **Note 4**
SP60	TssL2doV	SDOx Data Output Valid after $\overline{SSx}$ Edge	—	—	50	ns	

Note 1: These parameters are characterized, but are not tested in manufacturing.

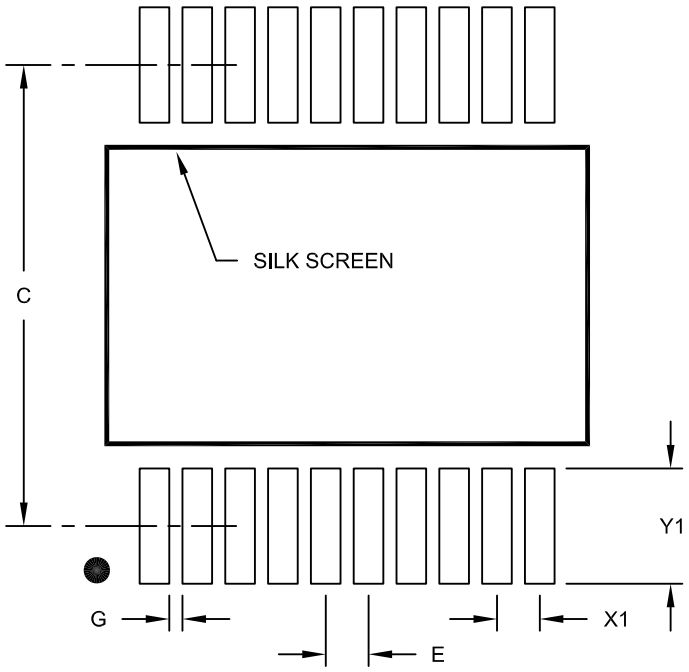
2: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCKx is 66.7 ns. Therefore, the SCKx clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPIx pins.

20-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	C		7.20	
Contact Pad Width (X20)	X1			0.45
Contact Pad Length (X20)	Y1			1.75
Distance Between Pads	G	0.20		

Notes:

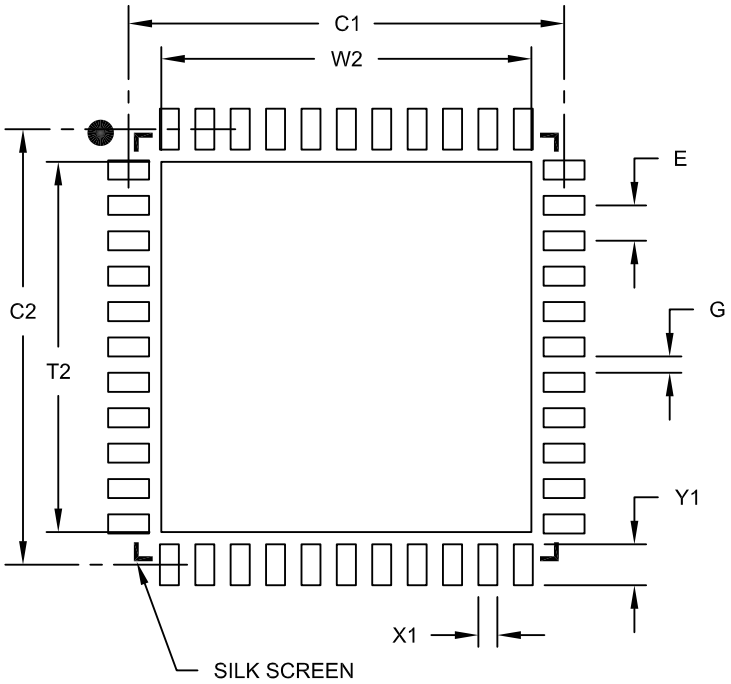
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2072A

44-Lead Plastic Quad Flat, No Lead Package (ML) – 8x8 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Optional Center Pad Width	W2			6.80
Optional Center Pad Length	T2			6.80
Contact Pad Spacing	C1		8.00	
Contact Pad Spacing	C2		8.00	
Contact Pad Width (X44)	X1			0.35
Contact Pad Length (X44)	Y1			0.80
Distance Between Pads	G	0.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2103A