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Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	16 MIPS
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	21
Program Memory Size	32KB (11K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	36-VFTLA Exposed Pad
Supplier Device Package	36-VTLA (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj32gp102-e-tl

dsPIC33FJ16(GP/MC)101/102 AND dsPIC33FJ32(GP/MC)101/102/104

dsPIC33FJ16(GP/MC)101/102 AND dsPIC33FJ32(GP/MC)101/102/104 PRODUCT FAMILIES

The device names, pin counts, memory sizes and peripheral availability of each device are listed in Table 1. The following pages show their pinout diagrams.

TABLE 1: dsPIC33FJ16(GP/MC)101/102 DEVICE FEATURES

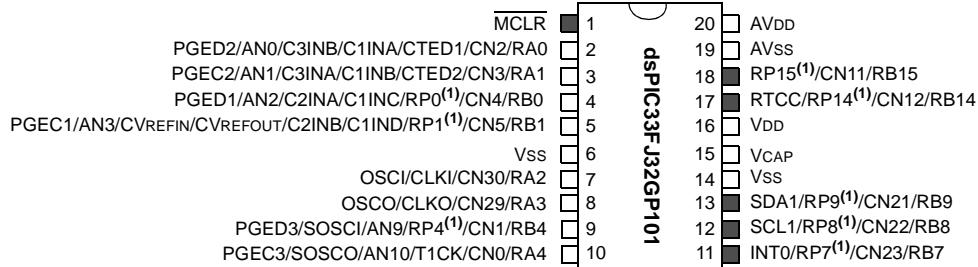
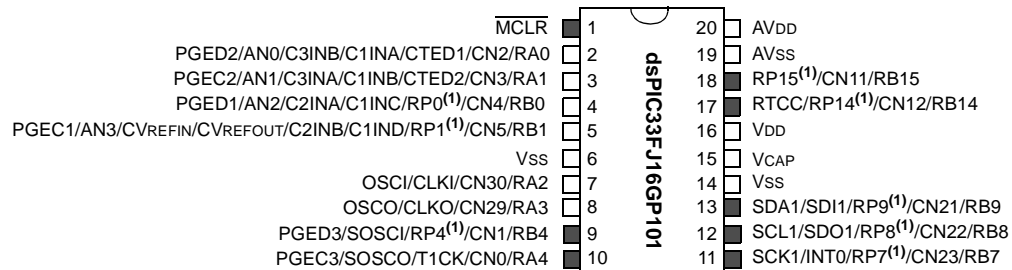
Device	Pins	Program Flash (Kbyte)	RAM (Kbytes)	Remappable Peripherals							Motor Control PWM	PWM Faults	10-Bit, 1.1 Msps ADC	RTCC	I ² C™	Comparators	CTMU	I/O Pins	Packages
				Remappable Pins	16-bit Timer ^(1,2)	Input Capture	Output Compare	UART	External Interrupts ⁽³⁾	SPI									
dsPIC33FJ16GP101	18	16	1	8	3	3	2	1	3	1	—	—	1 ADC, 4-ch	Y	1	3	Y	13	PDIP, SOIC
	20	16	1	8	3	3	2	1	3	1	—	—	1 ADC, 4-ch	Y	1	3	Y	15	SSOP
dsPIC33FJ16GP102	28	16	1	16	3	3	2	1	3	1	—	—	1 ADC, 6-ch	Y	1	3	Y	21	SPDIP, SOIC, SSOP, QFN
	36	16	1	16	3	3	2	1	3	1	—	—	1 ADC, 6-ch	Y	1	3	Y	21	VTLA
dsPIC33FJ16MC101	20	16	1	10	3	3	2	1	3	1	6-ch	1	1 ADC, 4-ch	Y	1	3	Y	15	PDIP, SOIC, SSOP
dsPIC33FJ16MC102	28	16	1	16	3	3	2	1	3	1	6-ch	2	1 ADC, 6-ch	Y	1	3	Y	21	SPDIP, SOIC, SSOP, QFN
	36	16	1	16	3	3	2	1	3	1	6-ch	2	1 ADC, 6-ch	Y	1	3	Y	21	VTLA

- Note** 1: Two out of three timers are remappable.
2: One pair can be combined to create one 32-bit timer.
3: Two out of three interrupts are remappable.

Pin Diagrams (Continued)

20-Pin SSOP

■ = Pins are up to 5V tolerant



Note 1: The RPN pins can be used by any remappable peripheral. See Table 1 for the list of available peripherals.

TABLE 4-9: INPUT CAPTURE REGISTER MAP

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IC1BUF	0140	Input Capture 1 Register																xxxx
IC1CON	0142	—	—	ICSIDL	—	—	—	—	—	ICTMR	IC1	IC10	ICOV	ICBNE	ICM2	ICM1	ICM0	0000
IC2BUF	0144	Input Capture 2 Register																xxxx
IC2CON	0146	—	—	ICSIDL	—	—	—	—	—	ICTMR	IC1	IC10	ICOV	ICBNE	ICM2	ICM1	ICM0	0000
IC3BUF	0148	Input Capture 3 Register																xxxx
IC3CON	014A	—	—	ICSIDL	—	—	—	—	—	ICTMR	IC1	IC10	ICOV	ICBNE	ICM2	ICM1	ICM0	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-10: OUTPUT COMPARE REGISTER MAP

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
OC1RS	0180	Output Compare 1 Secondary Register																xxxx
OC1R	0182	Output Compare 1 Register																xxxx
OC1CON	0184	—	—	OCSIDL	—	—	—	—	—	—	—	—	OCFLT	OCTSEL	OCM2	OCM1	OCM0	0000
OC2RS	0186	Output Compare 2 Secondary Register																xxxx
OC2R	0188	Output Compare 2 Register																xxxx
OC2CON	018A	—	—	OCSIDL	—	—	—	—	—	—	—	—	OCFLT	OCTSEL	OCM2	OCM1	OCM0	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-11: 6-OUTPUT PWM1 REGISTER MAP FOR dsPIC33FJXXMC10X DEVICES

SFR Name	SFR Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
P1TCON	01C0	PTEN	—	PTSIDL	—	—	—	—	—	PTOPS3	PTOPS2	PTOPS1	PTOPS0	PTCKPS1	PTCKPS0	PTMOD1	PTMOD0	0000 0000 0000 0000
P1TMR	01C2	PTDIR	PWM1 Timer Count Value Register															0000 0000 0000 0000
P1TPER	01C4	—	PWM1 Time Base Period Register															0111 1111 1111 1111
P1SECMP	01C6	SEVTDIR	PWM1 Special Event Compare Register															0000 0000 0000 0000
PWM1CON1	01C8	—	—	—	—	—	PMOD3	PMOD2	PMOD1	—	PEN3H	PEN2H	PEN1H	—	PEN3L	PEN2L	PEN1L	0000 0000 0000 0000
PWM1CON2	01CA	—	—	—	—	SEVOPS3	SEVOPS2	SEVOPS1	SEVOPS0	—	—	—	—	—	IUE	OSYNC	UDIS	0000 0000 0000 0000
P1DTCON1	01CC	DTBPS1	DTBPS0	DTB5	DTB4	DTB3	DTB2	DTB1	DTB0	DTAPS1	DTAPS0	DTA5	DTA4	DTA3	DTA2	DTA1	DTA0	0000 0000 0000 0000
P1DTCON2	01CE	—	—	—	—	—	—	—	—	—	—	DTS3A	DTS3I	DTS2A	DTS2I	DTS1A	DTS1I	0000 0000 0000 0000
P1FLTACON	01D0	—	—	FAOV3H	FAOV3L	FAOV2H	FAOV2L	FAOV1H	FAOV1L	FLTAM	—	—	—	—	FAEN3	FAEN2	FAEN1	0000 0000 0000 0111
P1FLTBCON	01D2	—	—	FBOV3H	FBOV3L	FBOV2H	FBOV2L	FBOV1H	FBOV1L	FLTBM	—	—	—	—	FBEN3	FBEN2	FBEN1	0000 0000 0000 0111
P1OVDCON	01D4	—	—	POVD3H	POVD3L	POVD2H	POVD2L	POVD1H	POVD1L	—	—	POUT3H	POUT3L	POUT2H	POUT2L	POUT1H	POUT1L	0011 1111 0000 0000
P1DC1	01D6	PWM1 Duty Cycle 1 Register																0000 0000 0000 0000
P1DC2	01D8	PWM1 Duty Cycle 2 Register																0000 0000 0000 0000
P1DC3	01DA	PWM1 Duty Cycle 3 Register																0000 0000 0000 0000
PWM1KEY	01DE	PWMKEY<15:0>																0000 0000 0000 0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

dsPIC33FJ16(GP/MC)101/102 AND dsPIC33FJ32(GP/MC)101/102/104

REGISTER 7-22: IPC7: INTERRUPT PRIORITY CONTROL REGISTER 7

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	INT2IP2	INT2IP1	INT2IP0	—	T5IP2 ⁽¹⁾	T5IP1 ⁽¹⁾	T5IP0 ⁽¹⁾
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-7 **Unimplemented:** Read as '0'

bit 6-4 **INT2IP<2:0>:** External Interrupt 2 Priority bits

111 = Interrupt is Priority 7 (highest priority interrupt)

•

•

•

001 = Interrupt is Priority 1

000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **T5IP<2:0>:** Timer5 Interrupt Priority bits⁽¹⁾

111 = Interrupt is Priority 7 (highest priority interrupt)

•

•

•

001 = Interrupt is Priority 1

000 = Interrupt source is disabled

Note 1: These bits are available in dsPIC33FJ32(GP/MC)10X devices only.

dsPIC33FJ16(GP/MC)101/102 AND dsPIC33FJ32(GP/MC)101/102/104

REGISTER 9-3: PMD3: PERIPHERAL MODULE DISABLE CONTROL REGISTER 3

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	U-0
—	—	—	—	—	CMPMD	RTCCMD	—
bit 15						bit 8	

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15-11 **Unimplemented:** Read as '0'
- bit 10 **CMPMD:** Comparator Module Disable bit
1 = Comparator module is disabled
0 = Comparator module is enabled
- bit 9 **RTCCMD:** RTCC Module Disable bit
1 = RTCC module is disabled
0 = RTCC module is enabled
- bit 8-0 **Unimplemented:** Read as '0'

REGISTER 9-4: PMD4: PERIPHERAL MODULE DISABLE CONTROL REGISTER 4

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15						bit 8	

U-0	U-0	U-0	U-0	U-0	R/W-0	U-0	U-0
—	—	—	—	—	CTMUMD	—	—
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15-3 **Unimplemented:** Read as '0'
- bit 2 **CTMUMD:** CTMU Module Disable bit
1 = CTMU module is disabled
0 = CTMU module is enabled
- bit 1-0 **Unimplemented:** Read as '0'

dsPIC33FJ16(GP/MC)101/102 AND dsPIC33FJ32(GP/MC)101/102/104

REGISTER 10-21: RPOR10: PERIPHERAL PIN SELECT OUTPUT REGISTER 10

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	RP21R<4:0> ⁽¹⁾				
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	RP20R<4:0> ⁽¹⁾				
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **RP21R<4:0>:** Peripheral Output Function is Assigned to RP21 Output Pin bits⁽¹⁾
(see Table 10-2 for peripheral function numbers)

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **RP20R<4:0>:** Peripheral Output Function is Assigned to RP20 Output Pin bits⁽¹⁾
(see Table 10-2 for peripheral function numbers)

Note 1: These bits are available in dsPIC33FJ32(GP/MC)104 devices only.

REGISTER 10-22: RPOR11: PERIPHERAL PIN SELECT OUTPUT REGISTER 11

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	RP23R<4:0> ⁽¹⁾				
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	RP22R<4:0> ⁽¹⁾				
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **RP23R<4:0>:** Peripheral Output Function is Assigned to RP23 Output Pin bits⁽¹⁾
(see Table 10-2 for peripheral function numbers)

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **RP22R<4:0>:** Peripheral Output Function is Assigned to RP22 Output Pin bits⁽¹⁾
(see Table 10-2 for peripheral function numbers)

Note 1: These bits are available in dsPIC33FJ32(GP/MC)104 devices only.

REGISTER 10-23: RPOR12: PERIPHERAL PIN SELECT OUTPUT REGISTER 12

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	RP25R<4:0> ⁽¹⁾				
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	RP24R<4:0> ⁽¹⁾				
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **RP25R<4:0>:** Peripheral Output Function is Assigned to RP25 Output Pin bits⁽¹⁾
(see Table 10-2 for peripheral function numbers)

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **RP24R<4:0>:** Peripheral Output Function is Assigned to RP24 Output Pin bits⁽¹⁾
(see Table 10-2 for peripheral function numbers)

Note 1: These bits are available in dsPIC33FJ32(GP/MC)104 devices only.

16.0 SERIAL PERIPHERAL INTERFACE (SPI)

Note 1: This data sheet summarizes the features of the dsPIC33FJ16(GP/MC)101/102 and dsPIC33FJ32(GP/MC)101/102/104 family devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**Serial Peripheral Interface (SPI)**” (DS70206) in the “*dsPIC33/PIC24 Family Reference Manual*”, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The Serial Peripheral Interface (SPI) module is a synchronous serial interface useful for communicating with other peripheral or microcontroller devices. These peripheral devices can be serial EEPROMs, shift registers, display drivers, Analog-to-Digital Converters, etc. The SPI module is compatible with SPI and SIOP from Motorola®.

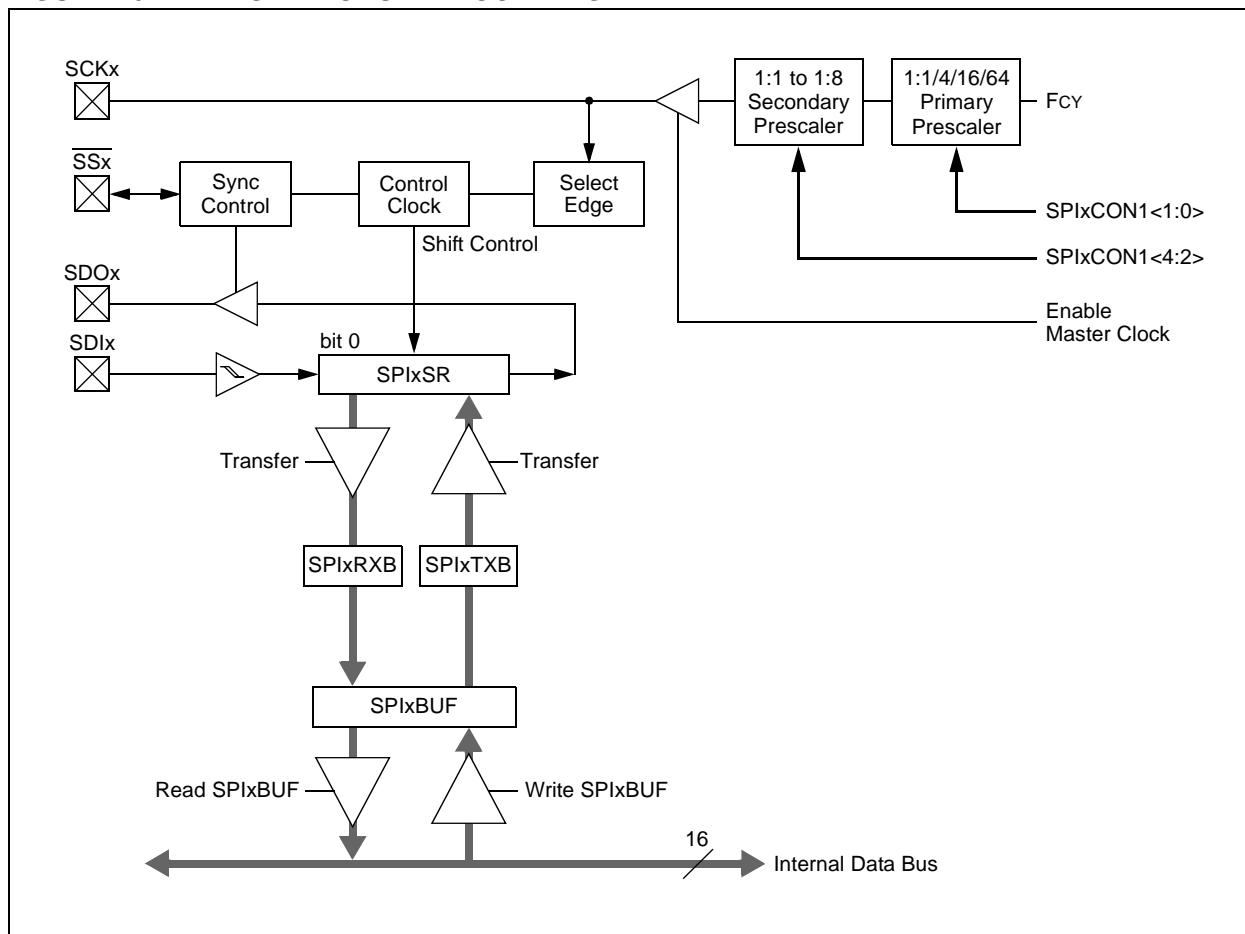
Each SPI module consists of a 16-bit shift register, SPIxSR (where x = 1 or 2), used for shifting data in and out, and a buffer register, SPIxBUF. A control register, SPIxCON, configures the module. Additionally, a status register, SPIxSTAT, indicates status conditions.

The serial interface consists of four pins:

- SDIx (serial data input)
- SDOx (serial data output)
- SCKx (shift clock input or output)
- SSx (active-low slave select).

In Master mode operation, SCKx is a clock output. In Slave mode, it is a clock input.

FIGURE 16-1: SPIx MODULE BLOCK DIAGRAM



REGISTER 17-2: I2CxSTAT: I2Cx STATUS REGISTER

R-0, HSC	R-0, HSC	U-0	U-0	U-0	R/C-0, HS	R-0, HSC	R-0, HSC
ACKSTAT	TRSTAT	—	—	—	BCL	GCSTAT	ADD10
bit 15						bit 8	

R/C-0, HS	R/C-0, HS	R-0, HSC	R/C-0, HSC	R/C-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC
IWCOL	I2COV	D_A	P	S	R_W	RBF	TBF
bit 7						bit 0	

Legend:	C = Clearable bit	HSC = Hardware Settable/Clearable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
HS = Hardware Settable bit		x = Bit is unknown

- bit 15 **ACKSTAT:** Acknowledge Status bit
(when operating as I²C™ master, applicable to master transmit operation)
1 = NACK received from slave
0 = ACK received from slave
Hardware sets or clears at end of slave Acknowledge.
- bit 14 **TRSTAT:** Transmit Status bit (when operating as I²C master, applicable to master transmit operation)
1 = Master transmit is in progress (8 bits + ACK)
0 = Master transmit is not in progress
Hardware sets at beginning of master transmission. Hardware clears at end of slave Acknowledge.
- bit 13-11 **Unimplemented:** Read as '0'
- bit 10 **BCL:** Master Bus Collision Detect bit
1 = A bus collision has been detected during a master operation
0 = No collision
Hardware sets at detection of bus collision.
- bit 9 **GCSTAT:** General Call Status bit
1 = General call address was received
0 = General call address was not received
Hardware sets when address matches general call address. Hardware clears at Stop detection.
- bit 8 **ADD10:** 10-Bit Address Status bit
1 = 10-bit address was matched
0 = 10-bit address was not matched
Hardware sets at match of 2nd byte of matched 10-bit address. Hardware clears at Stop detection.
- bit 7 **IWCOL:** Write Collision Detect bit
1 = An attempt to write to the I2CxTRN register failed because the I²C module is busy
0 = No collision
Hardware sets at occurrence of a write to I2CxTRN while busy (cleared by software).
- bit 6 **I2COV:** Receive Overflow Flag bit
1 = A byte was received while the I2CxRCV register is still holding the previous byte
0 = No overflow
Hardware sets at attempt to transfer I2CxRSR to I2CxRCV (cleared by software).
- bit 5 **D_A:** Data/Address bit (when operating as I²C slave)
1 = Indicates that the last byte received was data
0 = Indicates that the last byte received was a device address
Hardware clears at device address match. Hardware sets by reception of a slave byte.

dsPIC33FJ16(GP/MC)101/102 AND dsPIC33FJ32(GP/MC)101/102/104

REGISTER 19-2: AD1CON2: ADC1 CONTROL REGISTER 2

R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
VCFG2	VCFG1	VCFG0	—	—	CSCNA	CHPS1	CHPS0
bit 15						bit 8	

R-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
BUFS	—	SMPI3	SMPI2	SMPI1	SMPI0	BUFM	ALTS
bit 7						bit 0	

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-13 **VCFG<2:0>**: Converter Voltage Reference Configuration bits

	ADREF+	ADREF-
xxx	AVDD	AVSS

bit 12-11 **Unimplemented**: Read as '0'

bit 10 **CSCNA**: Scan Input Selections for CH0+ During Sample A bit

1 = Scans inputs
0 = Does not scan inputs

bit 9-8 **CHPS<1:0>**: Select Channels Utilized bits

1x = Converts CH0, CH1, CH2 and CH3
01 = Converts CH0 and CH1
00 = Converts CH0

bit 7 **BUFS**: Buffer Fill Status bit (valid only when BUFM = 1)

1 = ADC1 is currently filling second half of buffer, user should access data in the first half
0 = ADC1 is currently filling first half of buffer, user application should access data in the second half

bit 6 **Unimplemented**: Read as '0'

bit 5-2 **SMPI<3:0>**: Sample/Convert Sequences Per Interrupt Selection bits

1111 = Interrupts at the completion of conversion for each 16th sample/convert sequence
1110 = Interrupts at the completion of conversion for each 15th sample/convert sequence

•
•
•

0001 = Interrupts at the completion of conversion for each 2nd sample/convert sequence
0000 = Interrupts at the completion of conversion for each sample/convert sequence

bit 1 **BUFM**: Buffer Fill Mode Select bit

1 = Starts filling first half of buffer on first interrupt and the second half of buffer on next interrupt
0 = Always starts filling buffer from the beginning

bit 0 **ALTS**: Alternate Input Sample Mode Select bit

1 = Uses channel input selects for Sample A on first sample and Sample B on next sample
0 = Always uses channel input selects for Sample A

TABLE 24-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax	Description	# of Words	# of Cycles	Status Flags Affected
9	BTG	BTG $f, \#bit4$	Bit Toggle f	1	1	None
		BTG $Ws, \#bit4$	Bit Toggle Ws	1	1	None
10	BTSC	BTSC $f, \#bit4$	Bit Test f , Skip if Clear	1	1 (2 or 3)	None
		BTSC $Ws, \#bit4$	Bit Test Ws , Skip if Clear	1	1 (2 or 3)	None
11	BTSS	BTSS $f, \#bit4$	Bit Test f , Skip if Set	1	1 (2 or 3)	None
		BTSS $Ws, \#bit4$	Bit Test Ws , Skip if Set	1	1 (2 or 3)	None
12	BTST	BTST $f, \#bit4$	Bit Test f	1	1	Z
		BTST.C $Ws, \#bit4$	Bit Test Ws to C	1	1	C
		BTST.Z $Ws, \#bit4$	Bit Test Ws to Z	1	1	Z
		BTST.C Ws, Wb	Bit Test $Ws < Wb >$ to C	1	1	C
		BTST.Z Ws, Wb	Bit Test $Ws < Wb >$ to Z	1	1	Z
13	BTSTS	BTSTS $f, \#bit4$	Bit Test then Set f	1	1	Z
		BTSTS.C $Ws, \#bit4$	Bit Test Ws to C, then Set	1	1	C
		BTSTS.Z $Ws, \#bit4$	Bit Test Ws to Z, then Set	1	1	Z
14	CALL	CALL $lit23$	Call subroutine	2	2	None
		CALL Wn	Call indirect subroutine	1	2	None
15	CLR	CLR f	$f = 0x0000$	1	1	None
		CLR $WREG$	$WREG = 0x0000$	1	1	None
		CLR Ws	$Ws = 0x0000$	1	1	None
		CLR $Acc, Wx, Wxd, Wy, Wyd, AWB$	Clear Accumulator	1	1	OA,OB,SA,SB
16	CLRWDT	CLRWDT	Clear Watchdog Timer	1	1	WDTO, Sleep
17	COM	COM f	$f = \bar{f}$	1	1	N,Z
		COM $f, WREG$	$WREG = \bar{f}$	1	1	N,Z
		COM Ws, Wd	$Wd = \bar{Ws}$	1	1	N,Z
18	CP	CP f	Compare f with $WREG$	1	1	C,DC,N,OV,Z
		CP $Wb, \#lit5$	Compare Wb with $lit5$	1	1	C,DC,N,OV,Z
		CP Wb, Ws	Compare Wb with Ws ($Wb - Ws$)	1	1	C,DC,N,OV,Z
19	CP0	CP0 f	Compare f with $0x0000$	1	1	C,DC,N,OV,Z
		CP0 Ws	Compare Ws with $0x0000$	1	1	C,DC,N,OV,Z
20	CPB	CPB f	Compare f with $WREG$, with Borrow	1	1	C,DC,N,OV,Z
		CPB $Wb, \#lit5$	Compare Wb with $lit5$, with Borrow	1	1	C,DC,N,OV,Z
		CPB Wb, Ws	Compare Wb with Ws , with Borrow ($Wb - Ws - C$)	1	1	C,DC,N,OV,Z
21	CPSEQ	CPSEQ Wb, Wn	Compare Wb with Wn , skip if =	1	1 (2 or 3)	None
22	CPSGT	CPSGT Wb, Wn	Compare Wb with Wn , skip if >	1	1 (2 or 3)	None
23	CPSLT	CPSLT Wb, Wn	Compare Wb with Wn , skip if <	1	1 (2 or 3)	None
24	CPSNE	CPSNE Wb, Wn	Compare Wb with Wn , skip if \neq	1	1 (2 or 3)	None
25	DAW	DAW Wn	$Wn = \text{decimal adjust } Wn$	1	1	C
26	DEC	DEC f	$f = f - 1$	1	1	C,DC,N,OV,Z
		DEC $f, WREG$	$WREG = f - 1$	1	1	C,DC,N,OV,Z
		DEC Ws, Wd	$Wd = Ws - 1$	1	1	C,DC,N,OV,Z
27	DEC2	DEC2 f	$f = f - 2$	1	1	C,DC,N,OV,Z
		DEC2 $f, WREG$	$WREG = f - 2$	1	1	C,DC,N,OV,Z
		DEC2 Ws, Wd	$Wd = Ws - 2$	1	1	C,DC,N,OV,Z
28	DISI	DISI $\#lit14$	Disable Interrupts for k instruction cycles	1	1	None

25.2 MPLAB XC Compilers

The MPLAB XC Compilers are complete ANSI C compilers for all of Microchip's 8, 16, and 32-bit MCU and DSC devices. These compilers provide powerful integration capabilities, superior code optimization and ease of use. MPLAB XC Compilers run on Windows, Linux or MAC OS X.

For easy source level debugging, the compilers provide debug information that is optimized to the MPLAB X IDE.

The free MPLAB XC Compiler editions support all devices and commands, with no time or memory restrictions, and offer sufficient code optimization for most applications.

MPLAB XC Compilers include an assembler, linker and utilities. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. MPLAB XC Compiler uses the assembler to produce its object file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

25.3 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code, and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB X IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multipurpose source files
- Directives that allow complete control over the assembly process

25.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

25.5 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC DSC devices. MPLAB XC Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

TABLE 26-10: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS (CONTINUED)

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic	Min	Typ ⁽¹⁾	Max	Units	Conditions
DI60a	IICL	Input Low Injection Current	0	-5 ^(5,8)	—	mA	All pins except VDD, VSS, AVDD, AVSS, MCLR, VCAP, SOSCI, SOSCO and RB14
DI60b	IICH	Input High Injection Current	0	—	+5 ^(6,7,8)	mA	All pins except VDD, VSS, AVDD, AVSS, MCLR, VCAP, SOSCI, SOSCO, RB14 and digital 5V tolerant designated pins
DI60c	Σ IICT	Total Input Injection Current (sum of all I/O and control pins)	-20 ⁽⁹⁾	—	+20 ⁽⁹⁾	mA	Absolute instantaneous sum of all ± input injection currents from all I/O pins (IICL + IICH) ≤ Σ IICT

Note 1: Data in “Typ” column is at 3.3V, +25°C unless otherwise stated.

- 2:** The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current can be measured at different input voltages.
- 3:** Negative current is defined as current sourced by the pin.
- 4:** See the “Pin Diagrams” section for the 5V tolerant I/O pins.
- 5:** VIL source < (VSS – 0.3). Characterized but not tested.
- 6:** Non-5V tolerant pins, VIH source > (VDD + 0.3), 5V tolerant pins, VIH source > 5.5V. Characterized but not tested.
- 7:** Digital 5V tolerant pins cannot tolerate any “positive” input injection current from input sources > 5.5V.
- 8:** Injection currents > | 0 | can affect the ADC results by approximately 4-6 counts.
- 9:** Any number and/or combination of I/O pins, not excluded under IICL or IICH conditions, are permitted provided the mathematical “absolute instantaneous” sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.

TABLE 26-34: SPIx SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0) TIMING REQUIREMENTS FOR dsPIC33FJ16(GP/MC)10X

AC CHARACTERISTICS			Standard Operating Conditions: 2.4V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic ⁽¹⁾	Min	Typ ⁽²⁾	Max	Units	Conditions
SP70	TscP	Maximum SCKx Input Frequency	—	—	11	MHz	See Note 3
SP72	TscF	SCKx Input Fall Time	—	—	—	ns	See Parameter DO32 and Note 4
SP73	TscR	SCKx Input Rise Time	—	—	—	ns	See Parameter DO31 and Note 4
SP30	TdoF	SDOx Data Output Fall Time	—	—	—	ns	See Parameter DO32 and Note 4
SP31	TdoR	SDOx Data Output Rise Time	—	—	—	ns	See Parameter DO31 and Note 4
SP35	Tsch2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	—	—	ns	
SP41	Tsch2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SSx} \downarrow$ to SCKx \uparrow or SCKx Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{SSx} \uparrow$ to SDOx Output High-Impedance	10	—	50	ns	See Note 4
SP52	Tsch2ssH TscL2ssH	\overline{SSx} after SCKx Edge	1.5 TCY + 40	—	—	ns	See Note 4
SP60	TssL2doV	SDOx Data Output Valid after \overline{SSx} Edge	—	—	50	ns	

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in “Typ” column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCKx is 91 ns. Therefore, the SCKx clock generated by the Master must not violate this specification.

4: Assumes 50 pF load on all SPIx pins.

TABLE 26-43: SPIx SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0) TIMING REQUIREMENTS FOR dsPIC33FJ32(GP/MC)10X

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic ⁽¹⁾	Min	Typ ⁽²⁾	Max	Units	Conditions
SP70	TscP	Maximum SCKx Input Frequency	—	—	15	MHz	See Note 3
SP72	TscF	SCKx Input Fall Time	—	—	—	ns	See Parameter DO32 and Note 4
SP73	TscR	SCKx Input Rise Time	—	—	—w	ns	See Parameter DO31 and Note 4
SP30	TdoF	SDOx Data Output Fall Time	—	—	—	ns	See Parameter DO32 and Note 4
SP31	TdoR	SDOx Data Output Rise Time	—	—	—	ns	See Parameter DO31 and Note 4
SP35	Tsch2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	—	—	ns	
SP41	Tsch2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SSx} \downarrow$ to SCKx \uparrow or SCKx Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{SSx} \uparrow$ to SDOx Output High-Impedance	10	—	50	ns	See Note 4
SP52	Tsch2ssH TscL2ssH	\overline{SSx} after SCKx Edge	1.5 TCY + 40	—	—	ns	See Note 4

- Note 1:** These parameters are characterized, but are not tested in manufacturing.
Note 2: Data in “Typ” column is at 3.3V, +25°C unless otherwise stated.
Note 3: The minimum clock period for SCKx is 66.7 ns. Therefore, the SCKx clock generated by the Master must not violate this specification.
Note 4: Assumes 50 pF load on all SPIx pins.

TABLE 26-45: I2Cx BUS DATA TIMING REQUIREMENTS (MASTER MODE)

AC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Param No.	Symbol	Characteristic		Min ⁽¹⁾	Max	Units	Conditions
IM10	TLO:SCL	Clock Low Time	100 kHz mode	Tcy/2 (BRG + 1)	—	μs	
			400 kHz mode	Tcy/2 (BRG + 1)	—	μs	
			1 MHz mode ⁽²⁾	Tcy/2 (BRG + 1)	—	μs	
IM11	THI:SCL	Clock High Time	100 kHz mode	Tcy/2 (BRG + 1)	—	μs	
			400 kHz mode	Tcy/2 (BRG + 1)	—	μs	
			1 MHz mode ⁽²⁾	Tcy/2 (BRG + 1)	—	μs	
IM20	TF:SCL	SDAx and SCLx Fall Time	100 kHz mode	—	300	ns	Cb is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 Cb	300	ns	
			1 MHz mode ⁽²⁾	—	100	ns	
IM21	TR:SCL	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	Cb is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 Cb	300	ns	
			1 MHz mode ⁽²⁾	—	300	ns	
IM25	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	ns	
			400 kHz mode	100	—	ns	
			1 MHz mode ⁽²⁾	40	—	ns	
IM26	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	μs	
			400 kHz mode	0	0.9	μs	
			1 MHz mode ⁽²⁾	0.2	—	μs	
IM30	TSU:STA	Start Condition Setup Time	100 kHz mode	Tcy/2 (BRG + 1)	—	μs	Only relevant for Repeated Start condition
			400 kHz mode	Tcy/2 (BRG + 1)	—	μs	
			1 MHz mode ⁽²⁾	Tcy/2 (BRG + 1)	—	μs	
IM31	THD:STA	Start Condition Hold Time	100 kHz mode	Tcy/2 (BRG + 1)	—	μs	After this period the first clock pulse is generated
			400 kHz mode	Tcy/2 (BRG + 1)	—	μs	
			1 MHz mode ⁽²⁾	Tcy/2 (BRG + 1)	—	μs	
IM33	TSU:STO	Stop Condition Setup Time	100 kHz mode	Tcy/2 (BRG + 1)	—	μs	
			400 kHz mode	Tcy/2 (BRG + 1)	—	μs	
			1 MHz mode ⁽²⁾	Tcy/2 (BRG + 1)	—	μs	
IM34	THD:STO	Stop Condition Hold Time	100 kHz mode	Tcy/2 (BRG + 1)	—	ns	
			400 kHz mode	Tcy/2 (BRG + 1)	—	ns	
			1 MHz mode ⁽²⁾	Tcy/2 (BRG + 1)	—	ns	
IM40	TAA:SCL	Output Valid from Clock	100 kHz mode	—	3500	ns	
			400 kHz mode	—	1000	ns	
			1 MHz mode ⁽²⁾	—	400	ns	
IM45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	μs	Time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	μs	
			1 MHz mode ⁽²⁾	0.5	—	μs	
IM50	Cb	Bus Capacitive Loading		—	400	pF	
IM51	TPGD	Pulse Gobbler Delay		65	390	ns	See Note 3

Note 1: BRG is the value of the I²C™ Baud Rate Generator. Refer to “Inter-Integrated Circuit (I²C™)” (DS70195) in the “dsPIC33/PIC24 Family Reference Manual”. Please see the Microchip web site for the latest “dsPIC33/PIC24 Family Reference Manual” sections.

2: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

3: Typical value for this parameter is 130 ns.

TABLE 26-53: COMPARATOR VOLTAGE REFERENCE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions:3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic	Min.	Typ	Max.	Units	Conditions
VRD310	CVRES	Resolution	CVRSRC/24	—	CVRSRC/32	LSb	
VRD311	CVRAA	Absolute Accuracy	—	—	0.5	LSb	
VRD312	CVRUR	Unit Resistor Value (R)	—	2k	—	Ω	

TABLE 26-54: CTMU CURRENT SOURCE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions:3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic	Min.	Typ	Max.	Units	Conditions
CTMU Current Source							
CTMUI1	IOUT1	Base Range ⁽¹⁾	320	550	980	na	IRNG<1:0> bits (CTMUICON<9:8>) = 0b01
CTMUI2	IOUT2	10x Range ⁽¹⁾	3.2	5.5	9.8	μA	IRNG<1:0> bits (CTMUICON<9:8>) = 0b10
CTMUI3	IOUT3	100x Range ⁽¹⁾	32	55	98	μA	IRNG<1:0> bits (CTMUICON<9:8>) = 0b11
Internal Diode							
CTMUFV1	VF	Forward Voltage ⁽²⁾	—	0.77	—	V	IRNG<1:0> bits (CTMUICON<9:8>) = 0b11 @ +25°C
CTMUFV2	VFVR	Forward Voltage Rate ⁽²⁾	—	-1.38	—	mV/°C	IRNG<1:0> bits (CTMUICON<9:8>) = 0b11

- Note 1:** Nominal value at center point of current trim range (ITRIM<5:0> bits (CTMUICON<15:10>) = 0b000000).
- Note 2:** ADC module configured for conversion speed of 500 kpsps. Parameters are characterized but not tested in manufacturing.

dsPIC33FJ16(GP/MC)101/102 AND dsPIC33FJ32(GP/MC)101/102/104

27.1 High-Temperature DC Characteristics

TABLE 27-1: OPERATING MIPS VS. VOLTAGE

Characteristic	VDD Range (in Volts)	Temperature Range (in °C)	Max MIPS
			dsPIC33FJ16(GP/MC)101/102 and dsPIC33FJ32(GP/MC)101/102/104
HDC5	VBOR – 3.6V ⁽¹⁾	-40°C to +150°C	5

Note 1: Overall functional device operation at $V_{BORMIN} < V_{DD} < V_{DDMIN}$ is tested but not characterized. All device analog modules, such as the ADC, etc., may have degraded performances below V_{DDMIN} .

TABLE 27-2: THERMAL OPERATING CONDITIONS

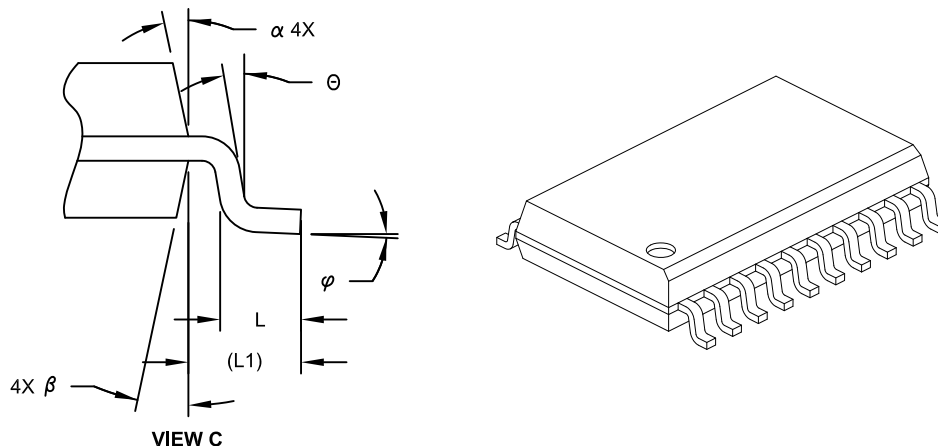
Rating	Symbol	Min	Typ	Max	Unit
High Temperature Devices					
Operating Junction Temperature Range	TJ	-40	—	+155	°C
Operating Ambient Temperature Range	TA	-40	—	+150	°C
Power Dissipation: Internal chip power dissipation: $P_{INT} = V_{DD} \times (I_{DD} - \sum I_{OH})$ I/O Pin Power Dissipation: $I/O = \sum (\{V_{DD} - V_{OH}\} \times I_{OH}) + \sum (V_{OL} \times I_{OL})$	PD	PINT + PI/O			W
Maximum Allowed Power Dissipation	PDMAX	$(T_J - T_A)/\theta_{JA}$			W

TABLE 27-3: DC CHARACTERISTICS: OPERATING CURRENT (IDD)

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +150°C for High Temperature		
Parameter No.	Typical	Max	Units	Conditions	
Operating Current (IDD) – dsPIC33FJ16(GP/MC)10X Devices					
DC20e	1.3	1.7	mA	3.3V	LPRC (32.768 kHz)
DC22e	7.0	8.5	mA	3.3V	5 MIPS

20-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	20		
Pitch	e	1.27 BSC		
Overall Height	A	-	-	2.65
Molded Package Thickness	A2	2.05	-	-
Standoff §	A1	0.10	-	0.30
Overall Width	E	10.30 BSC		
Molded Package Width	E1	7.50 BSC		
Overall Length	D	12.80 BSC		
Chamfer (Optional)	h	0.25	-	0.75
Foot Length	L	0.40	-	1.27
Footprint	L1	1.40 REF		
Lead Angle	θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.20	-	0.33
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

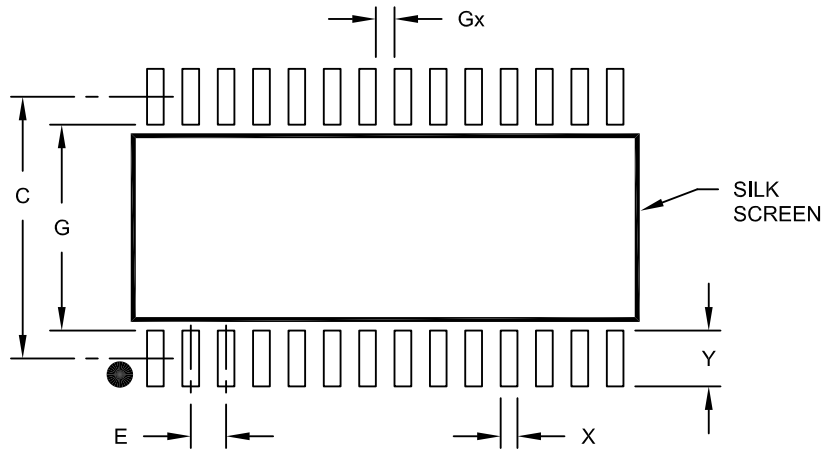
Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic
- Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.
- Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-094C Sheet 2 of 2

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		9.40	
Contact Pad Width (X28)	X			0.60
Contact Pad Length (X28)	Y			2.00
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	7.40		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2052A