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Applications of "**Embedded - Microcontrollers**"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	16 MIPs
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	21
Program Memory Size	32KB (11K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj32gp102-i-so

NOTES:

2.0 GUIDELINES FOR GETTING STARTED WITH 16-BIT DIGITAL SIGNAL CONTROLLERS

Note 1: This data sheet summarizes the features of the dsPIC33FJ16(GP/MC)101/102 and dsPIC33FJ32(GP/MC)101/102/104 family devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"dsPIC33/PIC24 Family Reference Manual"*. Please see the Microchip web site (www.microchip.com) for the latest *"dsPIC33/PIC24 Family Reference Manual"* sections.

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

2.1 Basic Connection Requirements

Getting started with the dsPIC33FJ16(GP/MC)101/102 and dsPIC33FJ32(GP/MC)101/102/104 family of 16-bit Digital Signal Controllers (DSCs) requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names, which must always be connected:

- All V_{DD} and V_{SS} pins
  (see **Section 2.2 "Decoupling Capacitors"**)
- All AV_{DD} and AV_{SS} pins, if present on the device (regardless if ADC module is not used)
  (see **Section 2.2 "Decoupling Capacitors"**)
- V_{CAP}
  (see **Section 2.3 "CPU Logic Filter Capacitor Connection (V_{CAP})"**)
- $\overline{MCLR}$ pin
  (see **Section 2.4 "Master Clear (MCLR) Pin"**)
- PGECx/PGEDx pins used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes
  (see **Section 2.5 "ICSP Pins"**)
- OSC1 and OSC2 pins when external oscillator source is used
  (see **Section 2.6 "External Oscillator Pins"**)

2.2 Decoupling Capacitors

The use of decoupling capacitors on every pair of power supply pins, such as V_{DD}, V_{SS}, AV_{DD} and AV_{SS}, is required.

Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** Recommendation of 0.1 µF (100 nF), 10V-20V. This capacitor should be a low-ESR and have resonance frequency in the range of 20 MHz and higher. It is recommended that ceramic capacitors be used.
- **Placement on the printed circuit board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended to place the capacitors on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch (6 mm) in length.
- **Handling high-frequency noise:** If the board is experiencing high-frequency noise, upward of tens of MHz, add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 µF to 0.001 µF. Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible. For example, 0.1 µF in parallel with 0.001 µF.
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum thereby reducing PCB track inductance.

The SAC and SAC.R instructions store either a truncated (SAC), or rounded (SAC.R) version of the contents of the target accumulator to data memory via the X bus, subject to data saturation (see **Section 3.6.3.2 "Data Space Write Saturation"**). For the MAC class of instructions, the accumulator write-back operation functions in the same manner, addressing combined MCU (X and Y) data space though the X bus. For this class of instructions, the data is always subject to rounding.

3.6.3.2 Data Space Write Saturation

In addition to adder/subtracter saturation, writes to data space can also be saturated, but without affecting the contents of the source accumulator. The data space write saturation logic block accepts a 16-bit, 1.15 fractional value from the round logic block as its input, together with overflow status from the original source (accumulator) and the 16-bit round adder. These inputs are combined and used to select the appropriate 1.15 fractional value as output to write to data space memory.

If the SATDW bit in the CORCON register is set, data (after rounding or truncation) is tested for overflow and adjusted accordingly:

- For input data greater than 0x007FFF, data written to memory is forced to the maximum positive 1.15 value, 0x7FFF.
- For input data less than 0xFF8000, data written to memory is forced to the maximum negative 1.15 value, 0x8000.

The MSb of the source (bit 39) is used to determine the sign of the operand being tested.

If the SATDW bit in the CORCON register is not set, the input data is always passed through unmodified under all conditions.

3.6.4 BARREL SHIFTER

The barrel shifter can perform up to 16-bit arithmetic or logic right shifts, or up to 16-bit left shifts, in a single cycle. The source can be either of the two DSP accumulators or the X bus (to support multi-bit shifts of register or memory data).

The shifter requires a signed binary value to determine both the magnitude (number of bits) and direction of the shift operation. A positive value shifts the operand right. A negative value shifts the operand left. A value of '0' does not modify the operand.

The barrel shifter is 40 bits wide, thereby obtaining a 40-bit result for DSP shift operations and a 16-bit result for MCU shift operations. Data from the X bus is presented to the barrel shifter between Bit Positions 16 and 31 for right shifts, and between Bit Positions 0 and 16 for left shifts.

TABLE 4-26: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33FJ32(GP/MC)104 DEVICES

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPOR0	06C0	—	—	—	RP1R<4:0>					—	—	—	RP0R<4:0>					0000
RPOR1	06C2	—	—	—	RP3R<4:0>					—	—	—	RP2R<4:0>					0000
RPOR2	06C4	—	—	—	RP5R<4:0>					—	—	—	RP4R<4:0>					0000
RPOR3	06C6	—	—	—	RP7R<4:0>					—	—	—	RP6R<4:0>					0000
RPOR4	06C8	—	—	—	RP9R<4:0>					—	—	—	RP8R<4:0>					0000
RPOR5	06CA	—	—	—	RP11R<4:0>					—	—	—	RP10R<4:0>					0000
RPOR6	06CC	—	—	—	RP13R<4:0>					—	—	—	RP12R<4:0>					0000
RPOR7	06CE	—	—	—	RP15R<4:0>					—	—	—	RP14R<4:0>					0000
RPOR8	06D0	—	—	—	RP17R<4:0>					—	—	—	RP16R<4:0>					0000
RPOR9	06D2	—	—	—	RP19R<4:0>					—	—	—	RP18R<4:0>					0000
RPOR10	06D4	—	—	—	RP21R<4:0>					—	—	—	RP20R<4:0>					0000
RPOR11	06D6	—	—	—	RP23R<4:0>					—	—	—	RP22R<4:0>					0000
RPOR12	06D8	—	—	—	RP25R<4:0>					—	—	—	RP24R<4:0>					0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-27: PORTA REGISTER MAP FOR dsPIC33FJ16(GP/MC)101/102 DEVICES

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISA	02C0	—	—	—	—	—	—	—	—	—	—	—	TRISA<4:0>					001F
PORTA	02C2	—	—	—	—	—	—	—	—	—	—	—	RA<4:0					xxxx
LATA	02C4	—	—	—	—	—	—	—	—	—	—	—	LATA<4:0					xxxx
ODCA	02C6	—	—	—	—	—	—	—	—	—	—	—	ODCA<4:2>			—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-28: PORTA REGISTER MAP FOR dsPIC33FJ32(GP/MC)101/102 DEVICES

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISA	02C0	—	—	—	—	—	—	—	—	—	—	—	TRISA<4:0>					001F
PORTA	02C2	—	—	—	—	—	—	—	—	—	—	—	RA<4:0					xxxx
LATA	02C4	—	—	—	—	—	—	—	—	—	—	—	LATA<4:0					xxxx
ODCA	02C6	—	—	—	—	—	—	—	—	—	—	—	—	ODCA<3:2>		—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-33: PORTB REGISTER MAP FOR dsPIC33FJ32GP101 DEVICES

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISB	02C8	TRISB<15:14>		—	—	—	—	TRISB<9:7>			—	—	TRISB4	—	—	TRISB<1:0>		C393
PORTB	02CA	RB<15:14>		—	—	—	—	RB<9:7>			—	—	RB4	—	—	RB<1:0>		xxxx
LATB	02CC	LATB<15:14>		—	—	—	—	LATB<9:7>			—	—	LATB4	—	—	LATB<1:0>		xxxx
ODCB	02CE	ODCB<15:14>		—	—	—	—	ODCB<9:7>			—	—	—	—	—	—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-34: PORTB REGISTER MAP FOR dsPIC33FJ32MC101 DEVICES

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISB	02C8	TRISB<15:12>				—	—	TRISB<9:7>			—	—	TRISB4	—	—	TRISB<1:0>		F393
PORTB	02CA	RB<15:12>				—	—	RB<9:7>			—	—	RB4	—	—	RB<1:0>		xxxx
LATB	02CC	LATB<15:12>				—	—	LATB<9:7>			—	—	LATB4	—	—	LATB<1:0>		xxxx
ODCB	02CE	ODCB<15:12>				—	—	ODCB<9:7>			—	—	—	—	—	—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-35: PORTB REGISTER MAP FOR dsPIC33FJ32(GP/MC)102 AND dsPIC33FJ32(GP/MC)104 DEVICES

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISB	02C8	TRISB<15:0>																FFFF
PORTB	02CA	RB<15:0>																xxxx
LATB	02CC	LATB<15:0>																xxxx
ODCB	02CE	ODCB<15:5>											—	—	—	—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-36: PORTC REGISTER MAP FOR dsPIC33FJ32(GP/MC)104 DEVICES

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISC	02D0	—	—	—	—	—	—	TRISC<9:0>										FFFF
PORTC	02D2	—	—	—	—	—	—	RC<9:0>										xxxx
LATC	02D4	—	—	—	—	—	—	LATC<9:0>										xxxx
ODCC	02D6	—	—	—	—	—	—	ODCC<9:6>				—	—	—	—	—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

REGISTER 5-1:   NVMCON: FLASH MEMORY CONTROL REGISTER

R/SO-0[1]	R/W-0[1]	R/W-0[1]	U-0	U-0	U-0	U-0	U-0
WR	WREN	WRERR	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0[1]	U-0	U-0	R/W-0[1]	R/W-0[1]	R/W-0[1]	R/W-0[1]
—	ERASE	—	—	NVMOP3[2]	NVMOP2[2]	NVMOP1[2]	NVMOP0[2]
bit 7							bit 0

Legend:		SO = Settable Only bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 15 **WR:** Write Control bit[1]

1 = Initiates a Flash memory program or erase operation; the operation is self-timed and the bit is cleared by hardware once operation is complete
0 = Program or erase operation is complete and inactive

bit 14 **WREN:** Write Enable bit[1]

1 = Enables Flash program/erase operations
0 = Inhibits Flash program/erase operations

bit 13 **WRERR:** Write Sequence Error Flag bit[1]

1 = An improper program or erase sequence attempt or termination has occurred (bit is set automatically on any set attempt of the WR bit)
0 = The program or erase operation completed normally

bit 12-7 **Unimplemented:** Read as '0'

bit 6 **ERASE:** Erase/Program Enable bit[1]

1 = Performs the erase operation specified by NVMOP<3:0> on the next WR command
0 = Performs the program operation specified by NVMOP<3:0> on the next WR command

bit 5-4 **Unimplemented:** Read as '0'

bit 3-0 **NVMOP<3:0>:** NVM Operation Selection bits[1,2]

<u>If ERASE = 1:</u>
1111 = No operation
1101 = Erase General Segment
1100 = No operation
0011 = No operation
0010 = Memory page erase operation
0001 = No operation
0000 = No operation
<u>If ERASE = 0:</u>
1111 = No operation
1101 = No operation
1100 = No operation
0011 = Memory word program operation
0010 = No operation
0001 = No operation
0000 = No operation

Note 1: These bits can only be reset on a POR.
2: All other combinations of NVMOP<3:0> are unimplemented.

REGISTER 5-2:   NVMKEY: NONVOLATILE MEMORY KEY REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—

REGISTER 7-3: **INTCON1: INTERRUPT CONTROL REGISTER 1**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NSTDIS	OVAERR	OVBERR	COVAERR	COVBERR	OVATE	OVBTE	COVTE
bit 15							bit 8

R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
SFTACERR	DIV0ERR	—	MATHERR	ADDRERR	STKERR	OSCFAIL	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **NSTDIS:** Interrupt Nesting Disable bit
1 = Interrupt nesting is disabled
0 = Interrupt nesting is enabled

bit 14 **OVAERR:** Accumulator A Overflow Trap Flag bit
1 = Trap was caused by overflow of Accumulator A
0 = Trap was not caused by overflow of Accumulator A

bit 13 **OVBERR:** Accumulator B Overflow Trap Flag bit
1 = Trap was caused by overflow of Accumulator B
0 = Trap was not caused by overflow of Accumulator B

bit 12 **COVAERR:** Accumulator A Catastrophic Overflow Trap Flag bit
1 = Trap was caused by catastrophic overflow of Accumulator A
0 = Trap was not caused by catastrophic overflow of Accumulator A

bit 11 **COVBERR:** Accumulator B Catastrophic Overflow Trap Flag bit
1 = Trap was caused by catastrophic overflow of Accumulator B
0 = Trap was not caused by catastrophic overflow of Accumulator B

bit 10 **OVATE:** Accumulator A Overflow Trap Enable bit
1 = Trap overflow of Accumulator A
0 = Trap is disabled

bit 9 **OVBTE:** Accumulator B Overflow Trap Enable bit
1 = Trap overflow of Accumulator B
0 = Trap is disabled

bit 8 **COVTE:** Catastrophic Overflow Trap Enable bit
1 = Trap on catastrophic overflow of Accumulator A or B is enabled
0 = Trap is disabled

bit 7 **SFTACERR:** Shift Accumulator Error Status bit
1 = Math error trap was caused by an invalid accumulator shift
0 = Math error trap was not caused by an invalid accumulator shift

bit 6 **DIV0ERR:** Arithmetic Error Status bit
1 = Math error trap was caused by a divide-by-zero
0 = Math error trap was not caused by a divide-by-zero

bit 5 **Unimplemented:** Read as '0'

bit 4 **MATHERR:** Arithmetic Error Status bit
1 = Math error trap has occurred
0 = Math error trap has not occurred

REGISTER 10-3:   RPINR3: PERIPHERAL PIN SELECT INPUT REGISTER 3

U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	—	T3CKR4	T3CKR3	T3CKR2	T3CKR1	T3CKR0

bit 15   bit 8

U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	—	T2CKR4	T2CKR3	T2CKR2	T2CKR1	T2CKR0

bit 7   bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13   **Unimplemented:** Read as '0'

bit 12-8   **T3CKR<4:0>:** Assign Timer3 External Clock (T3CK) to the Corresponding RPn Pin bits
             11111 = Input tied to Vss
             11110 = Reserved
             .
             .
             .
             11010 = Reserved
             11001 = Input tied to RP25
             .
             .
             .
             00001 = Input tied to RP1
             00000 = Input tied to RP0

bit 7-5   **Unimplemented:** Read as '0'

bit 4-0   **T2CKR<4:0>:** Assign Timer2 External Clock (T2CK) to the Corresponding RPn Pin bits
             11111 = Input tied to Vss
             11110 = Reserved
             .
             .
             .
             11010 = Reserved
             11001 = Input tied to RP25
             .
             .
             .
             00001 = Input tied to RP1
             00000 = Input tied to RP0

REGISTER 10-9: **RPINR20: PERIPHERAL PIN SELECT INPUT REGISTER 20**

U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	—	SCK1R4[1]	SCK1R3[1]	SCK1R2[1]	SCK1R1[1]	SCK1R0[1]
bit 15							bit 8

U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	—	SDI1R4[1]	SDI1R3[1]	SDI1R2[1]	SDI1R1[1]	SDI1R0[1]
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **SCK1R<4:0>:** Assign SPI1 Clock Input (SCK1IN) to the Corresponding RPn Pin bits[1]

11111 = Input tied to Vss
11110 = Reserved
.
.
.
11010 = Reserved
11001 = Input tied to RP25
.
.
.
00001 = Input tied to RP1
00000 = Input tied to RP0

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **SDI1R<4:0>:** Assign SPI1 Data Input (SDI1) to the Corresponding RPn Pin bits[1]

11111 = Input tied to Vss
11110 = Reserved
.
.
.
11010 = Reserved
11001 = Input tied to RP25
.
.
.
00001 = Input tied to RP1
00000 = Input tied to RP0

Note 1: These bits are available in dsPIC33FJ32(GP/MC)10X devices only.

REGISTER 12-3: T4CON: TIMER4 CONTROL REGISTER[1]

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
TON	—	TSIDL	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0
—	TGATE	TCKPS1	TCKPS0	T32	—	TCS	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **TON:** Timer4 On bit

When T32 = 1:
1 = Starts 32-bit Timer4/5
0 = Stops 32-bit Timer4/5

When T32 = 0:
1 = Starts 16-bit Timer4
0 = Stops 16-bit Timer4

bit 14 **Unimplemented:** Read as '0'

bit 13 **TSIDL:** Timer4 Stop in Idle Mode bit

1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12-7 **Unimplemented:** Read as '0'

bit 6 **TGATE:** Timer4 Gated Time Accumulation Enable bit

When TCS = 1:
This bit is ignored.

When TCS = 0:
1 = Gated time accumulation is enabled
0 = Gated time accumulation is disabled

bit 5-4 **TCKPS<1:0>:** Timer4 Input Clock Prescale Select bits

11 = 1:256
10 = 1:64
01 = 1:8
00 = 1:1

bit 3 **T32:** 32-Bit Timer Mode Select bit

1 = Timer4 and Timer5 form a single 32-bit timer
0 = Timer4 and Timer5 act as two 16-bit timers

bit 2 **Unimplemented:** Read as '0'

bit 1 **TCS:** Timer4 Clock Source Select bit

1 = External clock from pin, T4CK (on the rising edge)
0 = Internal clock (F$_{CY}$)

bit 0 **Unimplemented:** Read as '0'

Note 1: This register is available in dsPIC33FJ32(GP/MC)10X devices only.

REGISTER 16-3: SPIxCON2: SPIx CONTROL REGISTER 2

R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0
FRMEN	SPIFSD	FRMPOL	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	U-0
—	—	—	—	—	—	FRMDLY	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15   **FRMEN:** Framed SPIx Support bit

1 = Framed SPIx support is enabled ($\overline{SS}$x pin is used as Frame Sync pulse input/output)
0 = Framed SPIx support is disabled

bit 14   **SPIFSD:** Frame Sync Pulse Direction Control bit

1 = Frame Sync pulse input (slave)
0 = Frame Sync pulse output (master)

bit 13   **FRMPOL:** Frame Sync Pulse Polarity bit

1 = Frame Sync pulse is active-high
0 = Frame Sync pulse is active-low

bit 12-2   **Unimplemented:** Read as '0'

bit 1   **FRMDLY:** Frame Sync Pulse Edge Select bit

1 = Frame Sync pulse coincides with first bit clock
0 = Frame Sync pulse precedes first bit clock

bit 0   **Unimplemented:** This bit must not be set to '1' by the user application

NOTES:

21.1 RTCC Module Registers

The RTCC module registers are organized into three categories:

• RTCC Control Registers
• RTCC Value Registers
• Alarm Value Registers

21.1.1 REGISTER MAPPING

To limit the register interface, the RTCC Timer and Alarm Time registers are accessed through corresponding register pointers. The RTCC Value register window (RTCVALH and RTCVALL) uses the RTCPTR bits (RCFGCAL<9:8>) to select the desired Timer register pair (see Table 21-1).

By writing the RTCVALH byte, the RTCC Pointer value (RTCPTR<1:0> bits) decrements by one until it reaches '00'. Once it reaches '00', the MINUTES and SECONDS value will be accessible through RTCVALH and RTCVALL until the pointer value is manually changed.

TABLE 21-1: RTCVAL REGISTER MAPPING

RTCPTR <1:0>	RTCC Value Register Window	
	RTCVAL<15:8>	RTCVAL<7:0>
00	MINUTES	SECONDS
01	WEEKDAY	HOURS
10	MONTH	DAY
11	—	YEAR

The Alarm Value register window (ALRMVALH and ALRMVALL) uses the ALRMPTR bits (ALCFGRPT<9:8>) to select the desired Alarm register pair (see Table 21-2).

By writing the ALRMVALH byte, the Alarm Pointer value (ALRMPTR<1:0> bits) decrements by one until it reaches '00'. Once it reaches '00', the ALRMMIN and ALRMSEC value will be accessible through ALRMVALH and ALRMVALL until the pointer value is manually changed.

TABLE 21-2: ALRMVAL REGISTER MAPPING

ALRMPTR <1:0>	Alarm Value Register Window	
	ALRMVAL<15:8>	ALRMVAL<7:0>
00	ALRMMIN	ALRMSEC
01	ALRMWD	ALRMHR
10	ALRMMNTH	ALRMDAY
11	—	—

Considering that the 16-bit core does not distinguish between 8-bit and 16-bit read operations, the user must be aware that when reading either the ALRMVALH or ALRMVALL, bytes will decrement the ALRMPTR<1:0> value. The same applies to the RTCVALH or RTCVALL bytes with the RTCPTR<1:0> being decremented.

Note: This only applies to read operations and not write operations.

21.1.2 WRITE LOCK

In order to perform a write to any of the RTCC Timer registers, the RTCWREN bit (RCFGCAL<13>) must be set (refer to Example 21-1).

Note: To avoid accidental writes to the timer, it is recommended that the RTCWREN bit (RCFGCAL<13>) is kept clear at any other time. For the RTCWREN bit to be set, there is only 1 instruction cycle time window allowed between the 55h/AA sequence and the setting of RTCWREN; therefore, it is recommended that code follow the procedure in Example 21-1.

EXAMPLE 21-1: SETTING THE RTCWREN BIT

```
    MOV     #NVMKEY, W1      ;move the address of NVMKEY into W1
    MOV     #0x55, W2
    MOV     #0xAA, W3
    MOV     W2, [W1]         ;start 55/AA sequence
    MOV     W3, [W1]
    BSET    RCFGCAL, #13     ;set the RTCWREN bit
```
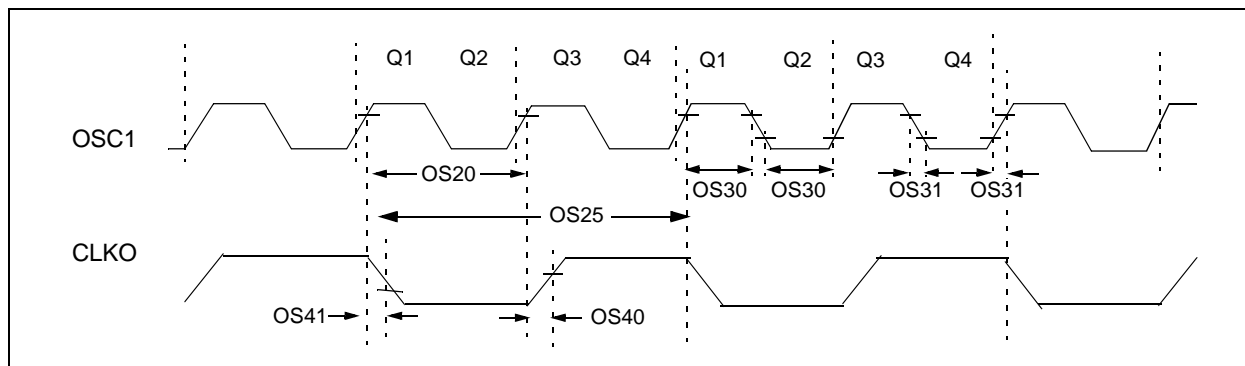
FIGURE 26-2: **EXTERNAL CLOCK TIMING**

**TABLE 26-16:** **EXTERNAL CLOCK TIMING REQUIREMENTS**

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symb	Characteristic	Min	Typ[1]	Max	Units	Conditions
OS10	F_{IN}	External CLKI Frequency (External clocks allowed only in EC and ECPLL modes)	DC	—	32	MHz	EC
		Oscillator Crystal Frequency	3.0 10 31	— — —	10 32 33	MHz MHz kHz	MS HS SOSC
OS20	T_{OSC}	T_{OSC} = 1/F_{OSC}	31.25	—	DC	ns	
OS25	T_{CY}	Instruction Cycle Time[2,4]	62.5	—	DC	ns	
OS30	TosL, TosH	External Clock in (OSC1)[5] High or Low Time	0.45 x T_{OSC}	—	—	ns	EC
OS31	TosR, TosF	External Clock in (OSC1)[5] Rise or Fall Time	—	—	20	ns	EC
OS40	TckR	CLKO Rise Time[3,5]	—	6	10	ns	
OS41	TckF	CLKO Fall Time[3,5]	—	6	10	ns	
OS42	G_M	External Oscillator Transconductance[4]	14	16	18	mA/V	VDD = 3.3V, TA = +25°C

Note 1: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.

2: Instruction cycle period (TCY) equals two times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type, under standard operating conditions, with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKI pin. When an external clock input is used, the "max." cycle time limit is "DC" (no clock) for all devices.

3: Measurements are taken in EC mode. The CLKO signal is measured on the OSC2 pin.

4: These parameters are characterized by similarity, but are tested in manufacturing at F_{IN} = 32 MHz only.

5: These parameters are characterized by similarity, but are not tested in manufacturing.

TABLE 26-29:   SPIx MAXIMUM DATA/CLOCK RATE SUMMARY FOR dsPIC33FJ16(GP/MC)10X

AC CHARACTERISTICS			Standard Operating Conditions: 2.4V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended		
Maximum Data Rate	**Master Transmit Only (Half-Duplex)**	**Master Transmit/Receive (Full-Duplex)**	**Slave Transmit/Receive (Full-Duplex)**	**CKE**	**CKP**	**SMP**
15 MHz	Table 26-30	—	—	0,1	0,1	0,1
10 MHz	—	Table 26-31	—	1	0,1	1
10 MHz	—	Table 26-32	—	0	0,1	1
15 MHz	—	—	Table 26-33	1	0	0
11 MHz	—	—	Table 26-34	1	1	0
15 MHz	—	—	Table 26-35	0	1	0
11 MHz	—	—	Table 26-36	0	0	0

FIGURE 26-11:   SPIx MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY, CKE = 0) TIMING CHARACTERISTICS FOR dsPIC33FJ16(GP/MC)10X

Note: Refer to Figure 26-1 for load conditions.
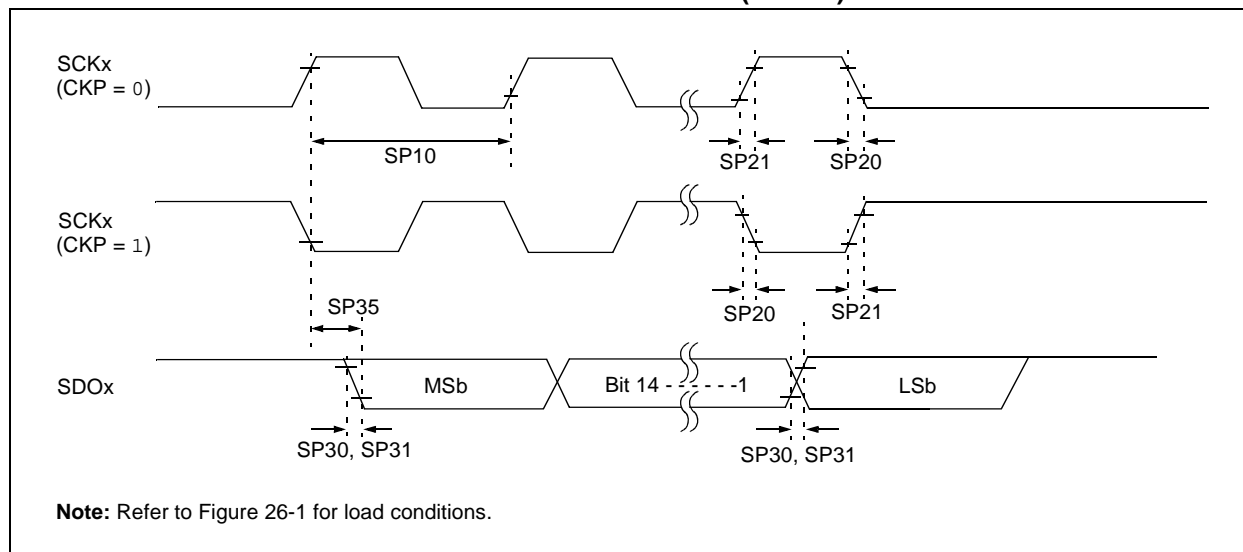
TABLE 26-46: I2Cx BUS DATA TIMING REQUIREMENTS (SLAVE MODE)

AC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Param.	Symbol	Characteristic		Min	Max	Units	Conditions
IS10	TLO:SCL	Clock Low Time	100 kHz mode	4.7	—	μs	Device must operate at a minimum of 1.5 MHz
			400 kHz mode	1.3	—	μs	Device must operate at a minimum of 10 MHz
			1 MHz mode[1]	0.5	—	μs	
IS11	THI:SCL	Clock High Time	100 kHz mode	4.0	—	μs	Device must operate at a minimum of 1.5 MHz
			400 kHz mode	0.6	—	μs	Device must operate at a minimum of 10 MHz
			1 MHz mode[1]	0.5	—	μs	
IS20	TF:SCL	SDAx and SCLx Fall Time	100 kHz mode	—	300	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
			1 MHz mode[1]	—	100	ns	
IS21	TR:SCL	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
			1 MHz mode[1]	—	300	ns	
IS25	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	ns	
			400 kHz mode	100	—	ns	
			1 MHz mode[1]	100	—	ns	
IS26	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	μs	
			400 kHz mode	0	0.9	μs	
			1 MHz mode[1]	0	0.3	μs	
IS30	TSU:STA	Start Condition Setup Time	100 kHz mode	4.7	—	μs	Only relevant for Repeated Start condition
			400 kHz mode	0.6	—	μs	
			1 MHz mode[1]	0.25	—	μs	
IS31	THD:STA	Start Condition Hold Time	100 kHz mode	4.0	—	μs	After this period, the first clock pulse is generated
			400 kHz mode	0.6	—	μs	
			1 MHz mode[1]	0.25	—	μs	
IS33	TSU:STO	Stop Condition Setup Time	100 kHz mode	4.7	—	μs	
			400 kHz mode	0.6	—	μs	
			1 MHz mode[1]	0.6	—	μs	
IS34	THD:STO	Stop Condition Hold Time	100 kHz mode	4000	—	ns	
			400 kHz mode	600	—	ns	
			1 MHz mode[1]	250		ns	
IS40	TAA:SCL	Output Valid from Clock	100 kHz mode	0	3500	ns	
			400 kHz mode	0	1000	ns	
			1 MHz mode[1]	0	350	ns	
IS45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	μs	Time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	μs	
			1 MHz mode[1]	0.5	—	μs	
IS50	CB	Bus Capacitive Loading		—	400	pF	

Note 1:   Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

18-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging
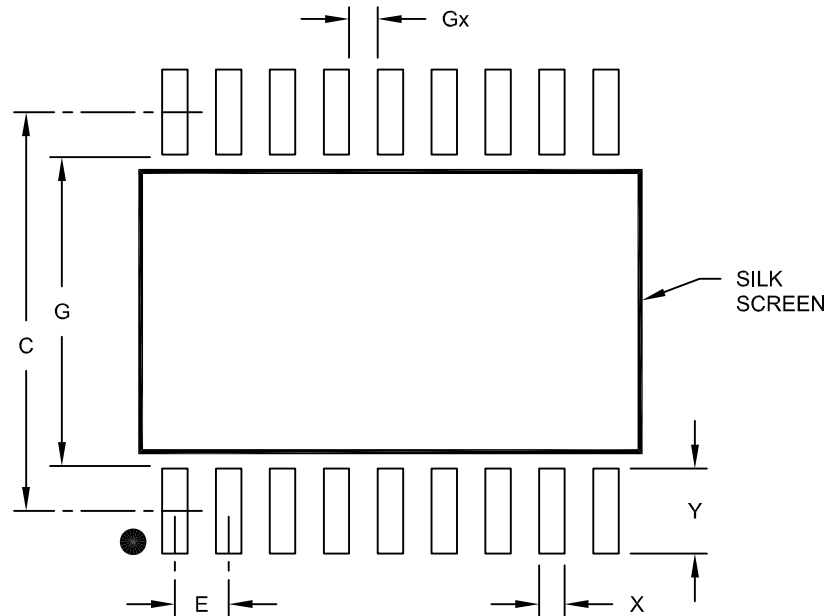
RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		9.40	
Contact Pad Width	X			0.60
Contact Pad Length	Y			2.00
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	7.40		

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2051A

**44-Terminal Very Thin Leadless Array Package (TL) – 6x6x0.9 mm Body
With Exposed Pad [VTLA]**

Note: For the most current package drawings, please see the Microchip Packaging Specification located at
http://www.microchip.com/packaging

TOP VIEW

SIDE VIEW

BOTTOM VIEW

Microchip Technology Drawing C04-157C Sheet 1 of 2

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NOTES: