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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Details	
Product Status	Obsolete
Core Processor	dsPIC
Core Size	16-Bit
Speed	16 MIPs
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	21
Program Memory Size	32KB (11K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj32gp102t-e-ml

Email: info@E-XFL.COM

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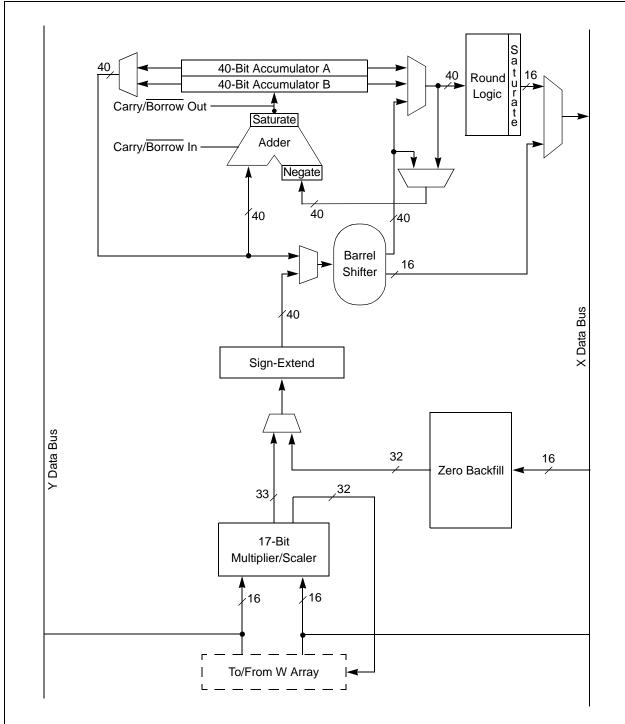


FIGURE 3-3: DSP ENGINE BLOCK DIAGRAM

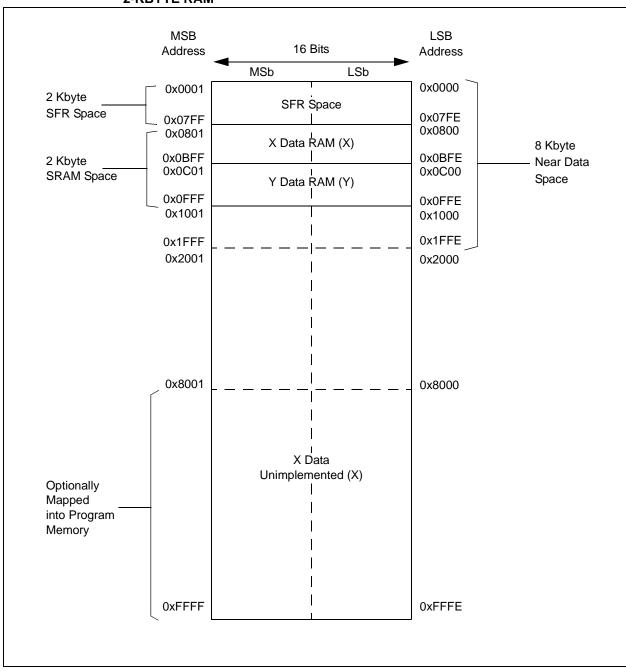


FIGURE 4-5: DATA MEMORY MAP FOR dsPIC33FJ32(GP/MC)101/102/104 DEVICES WITH 2-KBYTE RAM

4.2.5 X AND Y DATA SPACES

The core has two data spaces, X and Y. These data spaces can be considered either separate (for some DSP instructions), or as one unified linear address range (for MCU instructions). The data spaces are accessed using two Address Generation Units (AGUs) and separate data paths. This feature allows certain instructions to concurrently fetch two words from RAM, thereby enabling efficient execution of DSP algorithms such as Finite Impulse Response (FIR) filtering and Fast Fourier transform (FFT).

The X data space is used by all instructions and supports all addressing modes. X data space has separate read and write data buses. The X read data bus is the read data path for all instructions that view data space as combined X and Y address space. It is also the X data prefetch path for the dual operand DSP instructions (MAC class).

The Y data space is used in concert with the X data space by the MAC class of instructions (CLR, ED, EDAC, MAC, MOVSAC, MPY, MPY. N and MSC) to provide two concurrent data read paths.

Both the X and Y data spaces support Modulo Addressing mode for all instructions, subject to addressing mode restrictions. Bit-Reversed Addressing mode is only supported for writes to X data space.

All data memory writes, including in DSP instructions, view data space as combined X and Y address space. The boundary between the X and Y data spaces is device-dependent and is not user-programmable.

All Effective Addresses are 16 bits wide and point to bytes within the data space. Therefore, the data space address range is 64 Kbytes, or 32K words, although the implemented memory locations vary by device. NOTES:

6.3 POR

A POR circuit ensures the device is reset from poweron. The POR circuit is active until VDD crosses the VPOR threshold and the delay, TPOR, has elapsed. The delay, TPOR, ensures that the internal device bias circuits become stable.

The device supply voltage characteristics must meet the specified starting voltage and rise rate requirements to generate the POR. Refer to **Section 26.0** "**Electrical Characteristics**" for details.

The Power-on Reset (POR) status bit in the Reset Control (RCON<0>) register is set to indicate the Power-on Reset.

6.4 BOR and PWRT

The on-chip regulator has a BOR circuit that resets the device when the VDD is too low (VDD < VBOR) for proper device operation. The BOR circuit keeps the device in Reset until VDD crosses the VBOR threshold and the delay, TBOR, has elapsed. The delay, TBOR, ensures the voltage regulator output becomes stable.

The Brown-out Reset (BOR) status bit in the Reset Control (RCON<1>) register is set to indicate the Brown-out Reset.

The device will not run at full speed after a BOR as the VDD should rise to acceptable levels for full-speed operation. The Power-up Timer (PWRT) provides power-up time delay (TPWRT) to ensure that the system power supplies have stabilized at the appropriate levels for full-speed operation before the SYSRST is released.

Refer to **Section 23.0 "Special Features"** for further details.

Figure 6-3 shows the typical brown-out scenarios. The Reset delay (TBOR + TPWRT) is initiated each time VDD rises above the VBOR trip point.

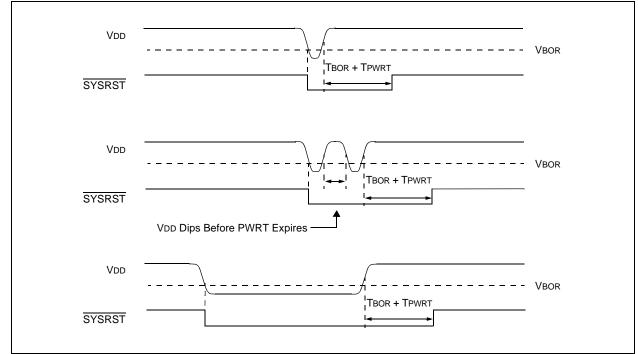


FIGURE 6-3: BROWN-OUT RESET SITUATIONS

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0					
—	U1RXIP2	U1RXIP1	U1RXIP0	—	SPI1IP2	SPI1IP1	SPI1IP0					
bit 15							bit					
	D 444	DAMA	DAMA		D 44/ 4	DAMA	DAMO					
U-0	R/W-1 SPI1EIP2	R/W-0 SPI1EIP1	R/W-0 SPI1EIP0	U-0	R/W-1 T3IP2	R/W-0 T3IP1	R/W-0 T3IP0					
bit 7	OTTEN 2	OFFICIENT	OFFICIENT		10112	1011 1	bit					
							_					
Legend: R = Readable	hit.		b :+		manted bit read							
		W = Writable		-	emented bit, read							
-n = Value at	POR	'1' = Bit is set		'0' = Bit is cl	eared	x = Bit is unkı	lown					
bit 15	Unimplemen	ted: Read as '	0'									
bit 14-12	-			Priority bits								
	U1RXIP<2:0>: UART1 Receiver Interrupt Priority bits 111 = Interrupt is Priority 7 (highest priority interrupt)											
	•											
	• 001 = Interrupt is Priority 1											
		pt is Friding 1 pt source is dis	abled									
bit 11		-										
bit 10-8	Unimplemented: Read as '0' SPI1IP<2:0>: SPI1 Event Interrupt Priority bits											
	111 = Interrupt is Priority 7 (highest priority interrupt)											
	•	pt le 1 llell, j 1 l	(geet pe	.,								
	•											
	001 = Interrupt is Priority 1 000 = Interrupt source is disabled											
bit 7		ited: Read as '										
bit 6-4	-			ty hite								
	SPI1EIP<2:0>: SPI1 Error Interrupt Priority bits											
	 111 = Interrupt is Priority 7 (highest priority interrupt) 											
	•											
	001 = Interru	pt is Priority 1 pt source is dis	abled									
bit 3		ited: Read as '										
bit 2-0	-	imer3 Interrupt										
Dit 2-0		pt is Priority 7	-	ty interrupt)								
	•	prist nonty /	(ingriest priorit	ly interrupt)								
	•											
	•											
	• 001 = Interrupt is Priority 1											

REGISTER 7-20: IPC5: INTERRUPT PRIORITY CONTROL REGISTER 5

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
		—	_	—		—	_
bit 15							bit 8
U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R/W-0
—	—	—	—	—	INT1IP2	INT1IP1	INT1IP0
bit 7							bit 0
Logondi							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit,	read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-3	Unimplemented: Read as '0'
bit 2-0	INT1IP<2:0>: External Interrupt 1 Priority bits
	111 = Interrupt is Priority 7 (highest priority interrupt)
	•
	•
	• 001 = Interrupt is Priority 1
	000 = Interrupt source is disabled

REGISTER 7-21: IPC6: INTERRUPT PRIORITY CONTROL REGISTER 6

U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0
_	T4IP2 ⁽¹⁾	T4IP1 ⁽¹⁾	T4IP0 ⁽¹⁾	—	_	_	_
bit 15							bit 8
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0
Legend:							
R = Readable I	bit	W = Writable	bit	U = Unimplemented bit, read as '0'			
-n = Value at POR '1' = Bit is set			'0' = Bit is cleared x = Bit is unknown			nown	
bit 15	Unimplemen	ted: Read as '	0'				

bit 14-12	T4IP<2:0>: Timer4 Interrupt Priority bits ⁽¹⁾
	111 = Interrupt is Priority 7 (highest priority interrupt)
	•
	•
	•
	001 = Interrupt is Priority 1
	000 = Interrupt source is disabled
bit 11-0	Unimplemented: Read as '0'

Note 1: These bits are available in dsPIC33FJ32(GP/MC)10X devices only.

PMD Control Registers 9.5

R/W-0 U-0 R/W-0 U-0 R/W-0 U-0 R/W-0 I2C1MD	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0		
R/W-0 U-0 R/W-0 U-0 R/W-0 U-0 R/W-0 I2C1MD	T5MD ⁽¹⁾	T4MD ⁽¹⁾	T3MD	T2MD	T1MD	_	PWM1MD	_		
I2C1MD - U1MD - SPI1MD - AD1MDf2 bit 7 bit - bit bit bit Legend: R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' nn = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown bit 15 TSMD: Timer5 Module Disable bit ⁽¹⁾ 1 = Timer5 module is disabled 0 = Timer6 module is disabled 0 = Timer7 module is disabled bit 14 T4MD: Timer4 Module Disable bit ⁽¹⁾ 1 = Timer6 module is enabled 0 = Timer7 module is disabled 0 = Timer7 module is disabled bit 13 T3MD: Timer3 Module Disable bit 1 = Timer7 module is disabled 0 = Timer7 module is enabled bit 14 T4MD: Timer2 Module Disable bit 1 = Timer2 module is enabled 0 = Timer7 module is disabled bit 11 Timer2 module is disabled 0 = Timer4 module is disabled 0 = Timer1 module is disabled 0 = Timer1 module is disabled bit 11 Timer2 module is disabled 0 = Timer4 module is disabled 0 = Timer4 module is disabled 0 = Timer4 module is disabled bit 11 Timer1 module is disabled 0 = Timer4 module is disabled 0 = Timer4 module is disabled 0 = Timer4 module is disabled	bit 15	•		1				bit		
I2C1MD - U1MD - SPI1MD - AD1MDf2 bit 7 bit - bit bit bit Legend: R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' nn = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown bit 15 TSMD: Timer5 Module Disable bit ⁽¹⁾ 1 = Timer5 module is disabled 0 = Timer6 module is disabled 0 = Timer7 module is disabled bit 14 T4MD: Timer4 Module Disable bit ⁽¹⁾ 1 = Timer6 module is enabled 0 = Timer7 module is disabled 0 = Timer7 module is disabled bit 13 T3MD: Timer3 Module Disable bit 1 = Timer7 module is disabled 0 = Timer7 module is enabled bit 14 T4MD: Timer2 Module Disable bit 1 = Timer2 module is enabled 0 = Timer7 module is disabled bit 11 Timer2 module is disabled 0 = Timer4 module is disabled 0 = Timer1 module is disabled 0 = Timer1 module is disabled bit 11 Timer2 module is disabled 0 = Timer4 module is disabled 0 = Timer4 module is disabled 0 = Timer4 module is disabled bit 11 Timer1 module is disabled 0 = Timer4 module is disabled 0 = Timer4 module is disabled 0 = Timer4 module is disabled										
Legend: R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown bit 15 T5MD: Timer5 Module Disable bit ⁽¹⁾ 1 = Timer5 module is enabled 0 = Timer5 module is enabled 0 = Timer4 module is enabled 0 = Timer4 module is disabled 0 = Timer3 module is enabled 0 = Timer3 module is enabled 0 = Timer4 module Disable bit 1 = Timer2 Module Disable bit 1 = Timer2 Module Disable bit 1 = Timer2 module is disabled 0 = Timer4 module is enabled 0 = Timer7 module is enabled 0 = Timer7 module is disabled 0 = Timer2 module is disabled 0 = Timer2 module is disabled 0 = Timer1 module is disabled 0 = UART1 modul	R/W-0	U-0	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0		
Legend: R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' in = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown bit 15 T5MD: Timer5 Module Disable bit ⁽¹⁾ 1 = Timer5 module is disabled 0 = Timer5 module is disabled 0 = Timer4 module is disabled 0 = Timer4 module is disabled 0 = Timer3 module is disabled 0 = Timer3 module is disabled 0 = Timer3 module is enabled 0 = Timer3 module is disabled 0 = Timer3 module is disabled 0 = Timer3 module is disabled 0 = Timer2 module is disabled 0 = Timer2 module is disabled 0 = Timer2 module is enabled 0 = Timer2 module is enabled 0 = Timer1 module is disabled 0 = Timer1 module is disabled 0 = Timer2 module is disabled 0 = Timer2 module is enabled 0 = Timer4 module is disabled 0 = UXM11 module is disabled 0 = UXM11 module is disabled 0 = UART1 module is disabled 0 = UART4 module i	I2C1MD		U1MD		SPI1MD	_	—	AD1MD ⁽²⁾		
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1 = Timer2 module is disabled 0 = Timer2 module is enabled bit 11 T1MD: Timer1 Module Disable bit 1 = Timer1 module is disabled 0 = Timer1 module is enabled bit 10 Unimplemented: Read as '0' bit 9 PWM1MD: PWM1 Module Disable bit 1 = PWM1 module is disabled 0 = PWM1 module is disabled 0 = PWM1 module is disabled 0 = PWM1 module is enabled bit 8 Unimplemented: Read as '0' bit 7 I2C1 Module Disable bit 1 = I2C1 module is disabled 0 = I2C1 module is disabled 0 = I2C1 module is disabled 0 = I2C1 module is disabled bit 6 Unimplemented: Read as '0' bit 5 U1MD: UART1 Module Disable bit 1 = UART1 module is disabled 0 = UART1 module is enabled 0 = UART1 module is enabled 0 = UART1 module is enabled	bit 12	T2MD: Time	r2 Module Disa	ble bit						
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1 = Timer1 module is disabled 0 = Timer1 module is enabled 0 = Timer1 module is enabled 0 = Timer1 module is enabled 0 = PWM1MD: PWM1 Module Disable bit 1 = PWM1 module is disabled 0 = PWM1 module is enabled 0 = I2C1 Module Disable bit 1 = I2C1 module is disabled 0 = I2C1 module is enabled 0 = I2C1 module is disabled 0 = I2C1 module is enabled 0 = UART1 Module Disable bit 1 = UART1 module is disabled 0 = UART1 module is enabled		0 = Timer2 n	nodule is enable	ed						
0 = Timer1 module is enabled bit 10 Unimplemented: Read as '0' bit 9 PWM1MD: PWM1 Module Disable bit 1 = PWM1 module is disabled 0 = PWM1 module is disabled 0 = PWM1 module is enabled 0 = PWM1 module is enabled bit 8 Unimplemented: Read as '0' bit 7 I2C1MD: I2C1 Module Disable bit 1 = I2C1 module is disabled 0 = I2C1 module is enabled 0 = I2C1 module is enabled 0 = I2C1 module is enabled bit 6 Unimplemented: Read as '0' bit 5 U1MD: UART1 Module Disable bit 1 = UART1 module is disabled 0 = UART1 module is enabled bit 4 Unimplemented: Read as '0'	bit 11	T1MD: Time	r1 Module Disa	ble bit						
bit 10 Unimplemented: Read as '0' bit 9 PWM1MD: PWM1 Module Disable bit 1 = PWM1 module is disabled 0 = PWM1 module is enabled bit 8 Unimplemented: Read as '0' bit 7 I2C1MD: I2C1 Module Disable bit 1 = I2C1 module is disabled 0 = I2C1 module is disabled 0 = I2C1 module is enabled 0 = I2C1 module is enabled bit 6 Unimplemented: Read as '0' bit 5 U1MD: UART1 Module Disable bit 1 = UART1 module is disabled 0 = UART1 module is enabled bit 4 Unimplemented: Read as '0'										
bit 9PWM1MD: PWM1 Module Disable bit1 = PWM1 module is disabled 0 = PWM1 module is enabledbit 8Unimplemented: Read as '0'bit 7I2C1MD: I2C1 Module Disable bit 1 = I2C1 module is disabled 0 = I2C1 module is enabledbit 6Unimplemented: Read as '0'bit 5U1MD: UART1 Module Disable bit 1 = UART1 module is disabled 0 = UART1 module is enabledbit 4Unimplemented: Read as '0'										
1 = PWM1 module is disabled $0 = PWM1$ module is enabledbit 8Unimplemented: Read as '0'bit 7I2C1MD: I2C1 Module Disable bit $1 = I2C1$ module is disabled $0 = I2C1$ module is enabledbit 6Unimplemented: Read as '0'bit 5U1MD: UART1 Module Disable bit $1 = UART1$ module is disabled $0 = UART1$ module is enabledbit 4Unimplemented: Read as '0'		-								
0 = PWM1 module is enabled bit 8 Unimplemented: Read as '0' bit 7 I2C1MD: I2C1 Module Disable bit 1 = I2C1 module is disabled 0 = I2C1 module is enabled bit 6 Unimplemented: Read as '0' bit 5 U1MD: UART1 Module Disable bit 1 = UART1 module is disabled 0 = UART1 module is enabled bit 4 Unimplemented: Read as '0'	bit 9									
bit 8 Unimplemented: Read as '0' bit 7 I2C1MD: I2C1 Module Disable bit 1 = I2C1 module is disabled 0 = I2C1 module is enabled bit 6 Unimplemented: Read as '0' bit 5 U1MD: UART1 Module Disable bit 1 = UART1 module is disabled 0 0 = UART1 module is enabled 0 bit 4 Unimplemented: Read as '0'										
bit 7 I2C1 Module Disable bit 1 = I2C1 module is disabled 0 = I2C1 module is enabled bit 6 Unimplemented: Read as '0' bit 5 U1MD: UART1 Module Disable bit 1 = UART1 module is disabled 0 = UART1 module is enabled bit 4	hit 8									
1 = 12C1 module is disabled $0 = 12C1$ module is enabled $0 = 12C1$ module is enabled $0 = 12C1$ module is enabled $0 = 12C1$ module is enabled $1 = UART1$ module Disable bit $1 = UART1$ module is enabled $0 = UART1$ module is enabled $0 = UART1$ module is enabled $0 = UART1$ module is enabled		-								
0 = I2C1 module is enabled bit 6 Unimplemented: Read as '0' bit 5 U1MD: UART1 Module Disable bit 1 = UART1 module is disabled 0 = UART1 module is enabled bit 4										
bit 5 U1MD: UART1 Module Disable bit 1 = UART1 module is disabled 0 = UART1 module is enabled bit 4 Unimplemented: Read as '0'										
1 = UART1 module is disabled 0 = UART1 module is enabled bit 4 Unimplemented: Read as '0'	bit 6	Unimpleme	nted: Read as '	0'						
0 = UART1 module is enabledDit 4Unimplemented: Read as '0'	bit 5	U1MD: UAR	T1 Module Disa	able bit						
bit 4 Unimplemented: Read as '0'		1 = UART1 r	module is disabl	led						
		0 = UART1 r	nodule is enabl	ed						
Note 1: These bits are available in dsPIC33FJ32(GP/MC)10X devices only.	bit 4	Unimpleme	nted: Read as '	0'						
	Note 1: ⊤	hese bits are av	vailable in dsPl	C33FJ32(GP/	MC)10X devices	only.				

REGISTER 9-1: PMD1: PERIPHERAL MODULE DISABLE CONTROL REGISTER 1

2: PCFGx bits have no effect if the ADC module is disabled by setting this bit. When the bit is set, all port pins that have been multiplexed with ANx will be in Digital mode.

10.4 Peripheral Pin Select (PPS)

Peripheral Pin Select configuration enables peripheral set selection and placement on a wide range of I/O pins. By increasing the pinout options available on a particular device, programmers can better tailor the microcontroller to their entire application, rather than trimming the application to fit the device.

The Peripheral Pin Select configuration feature operates over a fixed subset of digital I/O pins. Programmers can independently map the input and/or output of most digital peripherals to any one of these I/O pins. Peripheral Pin Select is performed in software and generally does not require the device to be reprogrammed. Hardware safeguards are included that prevent accidental or spurious changes to the peripheral mapping, once it has been established.

10.4.1 AVAILABLE PINS

The Peripheral Pin Select feature is used with a range of up to 16 pins. The number of available pins depends on the particular device and its pin count. Pins that support the Peripheral Pin Select feature include the designation "RPn" in their full pin designation, where "RP" designates a remappable peripheral and "n" is the remappable pin number.

10.4.2 CONTROLLING PERIPHERAL PIN SELECT

Peripheral Pin Select features are controlled through two sets of Special Function Registers: one to map peripheral inputs and one to map outputs. Because they are separately controlled, a particular peripheral's input and output (if the peripheral has both) can be placed on any selectable function pin without constraint.

The association of a peripheral to a peripheral selectable pin is handled in two different ways, depending on whether an input or output is being mapped.

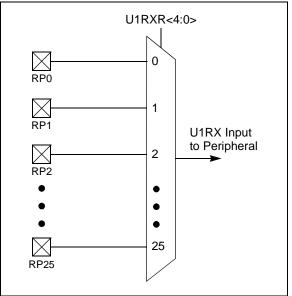
10.4.2.1 Input Mapping

The inputs of the Peripheral Pin Select options are mapped on the basis of the peripheral. A control register associated with a peripheral dictates the pin it will be mapped to. The RPINRx registers are used to configure peripheral input mapping (see Register 10-1 through Register 10-10). Each register contains sets of 5-bit fields, with each set associated with one of the remappable peripherals. Programming a given peripheral's bit field with an appropriate 5-bit value maps the RPn pin with that value to that peripheral. For any given device, the valid range of values for any bit field corresponds to the maximum number of Peripheral Pin Selections supported by the device.

Figure 10-2 Illustrates remappable pin selection for U1RX input.

Note: For input mapping only, the Peripheral Pin Select (PPS) functionality does not have priority over the TRISx settings. Therefore, when configuring the RPx pin for input, the corresponding bit in the TRISx register must also be configured for input (i.e., set to '1').

FIGURE 10-2: REMAPPABLE MUX INPUT FOR U1RX



U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0			
—	—	—		SEVOPS<3:0>						
bit 15							bit 8			
U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0			
_	—	—	_	—	IUE	OSYNC	UDIS			
bit 7	·						bit 0			
Legend:										
R = Readab	le bit	W = Writable I	oit	U = Unimplen	nented bit, rea	d as '0'				
-n = Value a	t POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkn	own			
bit 15-12	Unimplemen	ted: Read as ')'							
bit 11-8	SEVOPS<3:0>: PWMx Special Event Trigger Output Postscale Select bits									
	1111 = 1:16 postscale									
	•									
	•									
	• 0001 = 1:2 p	netecale								
	0000 = 1.2 p									
bit 7-3	•	ted: Read as 'd)'							
bit 2	IUE: Immedia	ate Update Enal	ole bit							
		to the active Px		are immediate						
	0 = Updates	to the active Px	DC registers	are synchroniz	ed to the PWN	lx time base				
bit 1	OSYNC: Out	put Override Sy	nchronizatio	n bit						
						he PWMx time b	ase			
	•			register occur o	on the next TCN	boundary				
bit 0		Update Disable		5 <i>4</i>						
				Buffer registers						
	0 = Updates from Duty Cycle and Period Buffer registers are enabled									

REGISTER 15-6: PWMxCON2: PWMx CONTROL REGISTER 2

REGISTER 18-2: UxSTA: UARTx STATUS AND CONTROL REGISTER (CONTINUED)

bit 5	ADDEN: Address Character Detect bit (Bit 8 of received data = 1) 1 = Address Detect mode is enabled; if 9-bit mode is not selected, this does not take effect
	0 = Address Detect mode is disabled
bit 4	RIDLE: Receiver Idle bit (read-only)
	1 = Receiver is Idle0 = Receiver is active
bit 3	PERR: Parity Error Status bit (read-only)
	 1 = Parity error has been detected for the current character (character at the top of the receive FIFO) 0 = Parity error has not been detected
bit 2	FERR: Framing Error Status bit (read-only)
	 1 = Framing error has been detected for the current character (character at the top of the receive FIFO) 0 = Framing error has not been detected
bit 1	OERR: Receive Buffer Overrun Error Status bit (read-only/clear only)
	1 = Receive buffer has overflowed
	0 = Receive buffer has not overflowed; clearing a previously set OERR bit (1 \rightarrow 0 transition) will reset the receiver buffer and the UxRSR to the empty state
bit 0	URXDA: UARTx Receive Buffer Data Available bit (read-only)
	1 = Receive buffer has data, at least one more character can be read
	0 = Receive buffer is empty

Note 1: Refer to "**UART**" (DS70188) in the "*dsPIC33/PIC24 Family Reference Manual*" for information on enabling the UART module for transmit operation.

	19-5: AD1C				CT REGISTE	IN IN				
R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
CH0NB	—	—	CH0SB4	CH0SB3	CH0SB2	CH0SB1	CH0SB0			
bit 15							bit 8			
R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
CH0NA		_	CH0SA4	CH0SA3	CH0SA2	CH0SA1	CH0SA0			
bit 7				1			bit (
Legend:										
R = Readable	e bit	W = Writable	bit	U = Unimplen	nented bit, read	d as '0'				
-n = Value at I	POR	'1' = Bit is se	t	'0' = Bit is clea		x = Bit is unkr	nown			
bit 15		-	e Input Select f	or Sample B bi	t					
		0 negative inpu 0 negative inpu								
bit 14-13		ited: Read as								
bit 12-8	-			lect for Sample	B hits					
511 12 0	CH0SB<4:0>: Channel 0 Positive Input Select for Sample B bits 11111-10000 = Reserved; do not use									
	01111 = Channel 0 positive input is $AN15^{(2)}$									
	01110 = No channels connected, all inputs are floating (used for CTMU)									
	01101 = Channel 0 positive input is connected to CTMU temperature sensor 01100 = Channel 0 positive input is AN12 ⁽²⁾									
			input is AN12 ⁴ input is AN11 ⁽²							
	01011 = Cha	annel 0 positive	input is AN10 ^{(;}	3)						
			input is AN9 ⁽³⁾							
			input is AN8 ⁽²⁾							
			input is AN7 ⁽²⁾							
		nnel 0 positive	input is AN6 ^{•-}							
	00101 = Channel 0 positive input is AN5 ⁽¹⁾ 00100 = Channel 0 positive input is AN4 ⁽¹⁾									
	00100 = 010		input is AN5 ⁽¹⁾)						
			input is AN5 ⁽¹⁾ input is AN4 ⁽¹⁾)						
	00011 = Cha 00010 = Cha	annel 0 positive annel 0 positive annel 0 positive	input is AN5 ⁽¹⁾ input is AN4 ⁽¹⁾ input is AN3 input is AN2)						
	00011 = Cha 00010 = Cha 00001 = Cha	annel 0 positive annel 0 positive annel 0 positive annel 0 positive	input is AN5 ⁽¹⁾ input is AN4 ⁽¹⁾ input is AN3 input is AN2 input is AN2)						
h:+ 7	00011 = Cha 00010 = Cha 00001 = Cha 00000 = Cha	annel 0 positive annel 0 positive annel 0 positive annel 0 positive annel 0 positive	input is AN5 ⁽¹⁾ input is AN4 ⁽¹⁾ input is AN3 input is AN2 input is AN1 input is AN0							
bit 7	00011 = Cha 00010 = Cha 00001 = Cha 00000 = Cha CH0NA: Cha	annel 0 positive annel 0 positive annel 0 positive annel 0 positive annel 0 positive annel 0 Negative	input is AN5 ⁽¹⁾ input is AN4 ⁽¹⁾ input is AN3 input is AN2 input is AN1 input is AN0 e Input Select f		t					
bit 7	00011 = Cha 00010 = Cha 00001 = Cha 00000 = Cha CHONA: Cha 1 = Channel	annel 0 positive annel 0 positive annel 0 positive annel 0 positive annel 0 positive annel 0 Negative 0 negative inpu	input is AN5 ⁽¹⁾ input is AN4 ⁽¹⁾ input is AN3 input is AN2 input is AN1 input is AN0 e Input Select fut is AN1		t					
	00011 = Cha 00010 = Cha 00001 = Cha 00000 = Cha CH0NA: Cha 1 = Channel 0 = Channel	annel 0 positive annel 0 positive annel 0 positive annel 0 positive annel 0 positive annel 0 Negative 0 negative inpu 0 negative inpu	input is AN5 ⁽¹⁾ input is AN4 ⁽¹⁾ input is AN3 input is AN2 input is AN1 input is AN0 e Input Select fut is AN1 ut is AVSS		t					
bit 6-5	00011 = Cha 00010 = Cha 00001 = Cha 00000 = Cha CH0NA: Cha 1 = Channel 0 = Channel Unimplemer	annel 0 positive annel 0 positive annel 0 positive annel 0 positive annel 0 positive annel 0 Negative 0 negative inpu 0 negative inpu ated: Read as	input is AN5 ⁽¹⁾ input is AN4 ⁽¹⁾ input is AN3 input is AN2 input is AN1 input is AN0 e Input Select f at is AN1 at is AVSS	or Sample A bi						
bit 7 bit 6-5 bit 4-0	00011 = Cha 00010 = Cha 00001 = Cha 00000 = Cha CH0NA: Cha 1 = Channel 0 = Channel Unimplemer CH0SA<4:0	annel 0 positive annel 0 positive annel 0 positive annel 0 positive annel 0 positive annel 0 Negative 0 negative inpu 0 negative inpu ated: Read as •: Channel 0 P	input is AN5 ⁽¹⁾ input is AN4 ⁽¹⁾ input is AN3 input is AN2 input is AN1 input is AN0 e Input Select fut is AN1 ut is AVSS	or Sample A bi						
bit 6-5 bit 4-0	00011 = Cha 00010 = Cha 00001 = Cha 00000 = Cha CH0NA: Cha 1 = Channel 0 = Channel Unimplemer CH0SA<4:0 >	annel 0 positive annel 0 positive annel 0 positive annel 0 positive annel 0 positive annel 0 Negative 0 negative inpu 0 negative inpu ated: Read as •: Channel 0 P c12-8> for the a	input is AN5 ⁽¹⁾ input is AN4 ⁽¹⁾ input is AN3 input is AN2 input is AN1 input is AN0 e Input Select f at is AN1 at is AVss o' ositive Input Se available setting	or Sample A bi lect for Sample ls.	e A bits	01, where it is r	eserved.			
bit 6-5 bit 4-0 Note 1: Thi	00011 = Cha 00010 = Cha 00001 = Cha 00000 = Cha CH0NA: Cha 1 = Channel 0 = Channel Unimplemer CH0SA<4:0 Refer to bits<	annel 0 positive annel 0 positive annel 0 positive annel 0 positive annel 0 positive annel 0 Negative 0 negative inpu 0 negative inpu ated: Read as •: Channel 0 P at2-8> for the a ilable in all dev	input is AN5 ⁽¹⁾ input is AN4 ⁽¹⁾ input is AN3 input is AN2 input is AN1 input is AN0 e Input Select fut is AN1 it is AVss o' ositive Input Se available setting	or Sample A bi lect for Sample js. the dsPIC33F.	A bits JXX(GP/MC)10					

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REGISTER 2	22-2: CTMU	JCON2: CTM	U CONTROL	REGISTER	2					
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
EDG1MOD	EDG1POL	EDG1SEL3	EDG1SEL2	EDG1SEL1	EDG1SEL0	EDG2STAT	EDG1STAT			
bit 15							bit 8			
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0			
EDG2MOD	EDG2POL	EDG2SEL3	EDG2SEL2	EDG2SEL1	EDG2SEL0		—			
bit 7							bit 0			
Legend:										
R = Readable	hit	W = Writable	hit	II – Unimplem	nented bit, read	las 'N'				
-n = Value at		1' = Bit is set	on	$0^{\circ} = \text{Bit is clear}$		x = Bit is unkr				
		1 – Dit 13 3et					IOWIT			
bit 15	EDG1MOD: E	Edge 1 Edge Sa	ampling Selecti	ion bit						
		edge-sensitive								
	0 = Edge 1 is	level-sensitive								
bit 14		dge 1 Polarity								
		programmed f								
bit 13-10	•	programmed f	•	•						
DIL 13-10		:0>: Edge 1 So		5						
	1xxx = Reserved 01xx = Reserved									
	0011 = CTED1 pin									
	0010 = CTED2 pin									
	0001 = OC1 r 0000 = Timer									
bit 9		Edge 2 Status b	.i+							
DIL 9		-		vritten to contro	l the edge sou	rce				
	1 = Edge 2 ha				i the edge sou	106.				
		as not occurred	ł							
bit 8	EDG1STAT: E	Edge 1 Status b	it							
		ates the status of Edge 1 and can be written to control the edge source.								
	 1 = Edge 1 has occurred 0 = Edge 1 has not occurred 									
bit 7	-			ion hit						
	EDG2MOD: Edge 2 Edge Sampling Selection bit 1 = Edge 2 is edge-sensitive									
		level-sensitive								
bit 6	EDG2POL: Edge 2 Polarity Select bit									
		programmed f programmed f								
bit 5-2	EDG2SEL<3:	0>: Edge 2 So	urce Select bits	6						
	1xxx = Reser									
	01xx = Reser									
	0011 = CTED 0010 = CTED									
		parator 2 modul	е							
		arator 2 modul	e							

REGISTER 22-2: CTMUCON2: CTMU CONTROL REGISTER 2

DC CHARACI	ERISTICS		(unless oth	perating Condition erwise stated) emperature -40°C -40°C		
Parameter No.	Typical ⁽¹⁾	Max	Units		Conditions	
Idle Current (I	DLE): Core Of	f, Clock On	Base Current	⁽²⁾ – dsPIC33FJ16(GP/MC)10X Device	es
DC40d	0.4	1.0	mA	-40°C		
DC40a	0.4	1.0	mA	+25°C	2.21/	LPRC
DC40b	0.4	1.0	mA	+85°C	- 3.3V	(32.768 kHz) ⁽³⁾
DC40c	0.5	1.0	mA	+125°C		
DC41d	0.5	1.1	mA	-40°C		
DC41a	0.5	1.1	mA	+25°C	2.01/	1 MIPS ⁽³⁾
DC41b	0.5	1.1	mA	+85°C	- 3.3V	T MIPS(*)
DC41c	0.8	1.1	mA	+125°C	1	
DC42d	0.9	1.6	mA	-40°C		
DC42a	0.9	1.6	mA	+25°C	2.21/	4 MIPS ⁽³⁾
DC42b	1.0	1.6	mA	+85°C	- 3.3V	4 101175(*)
DC42c	1.2	1.6	mA	+125°C	1	
DC43a	1.6	2.6	mA	+25°C		
DC43d	1.6	2.6	mA	-40°C	2.21/	10 MIPS ⁽³⁾
DC43b	1.7	2.6	mA	+85°C	- 3.3V	TU MIPS
DC43c	2	2.6	mA	+125°C	1	
DC44d	2.4	3.8	mA	-40°C		
DC44a	2.4	3.8	mA	+25°C	2.2)/	16 MIPS ⁽³⁾
DC44b	2.6	3.8	mA	+85°C	- 3.3V	TO MIPS
DC44c	2.9	3.8	mA	+125°C	1	

TABLE 26-7: DC CHARACTERISTICS: IDLE CURRENT (IIDLE)

Note 1: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

2: Base Idle current is measured as follows:

• CPU core is off, oscillator is configured in EC mode, OSC1 is driven with external square wave from rail-to-rail

- CLKO is configured as an I/O input pin in the Configuration Word
- External Secondary Oscillator (SOSC) is disabled (i.e., SOSCO and SOSCI pins are configured as digital I/O inputs)
- All I/O pins are configured as inputs and pulled to Vss
- $\overline{\text{MCLR}}$ = VDD, WDT and FSCM are disabled
- No peripheral modules are operating; however, every peripheral is being clocked (PMDx bits are all zeroed)
- **3:** These parameters are characterized, but not tested in manufacturing.

	RACTER			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)						
	RAUIER	131163	Operati	ng tempe	erature		\leq TA \leq +85°C for Industrial			
	1					-40°C :	\leq TA \leq +125°C for Extended			
Param No.	Symbol	Characteristic ⁽³⁾	Min	Typ ⁽¹⁾	Max	Units	Conditions			
		Program Flash Memory								
D130a	Eр	Cell Endurance	10,000	—	—	E/W	-40°C to +125°C			
D131	Vpr	VDD for Read	VMIN	—	3.6	V	VMIN = Minimum operating voltage			
D132b	Vpew	VDD for Self-Timed Write	VMIN	—	3.6	V	VMIN = Minimum operating voltage			
D134	Tretd	Characteristic Retention	20	_	—	Year	Provided no other specifications are violated			
D135	IDDP	Supply Current during Programming	—	10	—	mA				
D137a	TPE	Page Erase Time	20.1	—	26.5	ms	TPE = 168517 FRC cycles, TA = +85°C, See Note 2			
D137b	TPE	Page Erase Time	19.5	—	27.3	ms	TPE = 168517 FRC cycles, TA = +125°C, See Note 2			
D138a	Tww	Word Write Cycle Time	47.4	—	49.3	μs	Tww = 355 FRC cycles, TA = +85°C, See Note 2			
D138b	Tww	Word Write Cycle Time	47.4		49.3	μs	Tww = 355 FRC cycles, TA = +125°C, See Note 2			

TABLE 26-12: DC CHARACTERISTICS: PROGRAM MEMORY

Note 1: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.

2: Other conditions: FRC = 7.37 MHz, TUN<5:0> = b'011111 (for Min), TUN<5:0> = b'100000 (for Max). This parameter depends on the FRC accuracy (see Table 26-18) and the value of the FRC Oscillator Tuning register (see Register 8-3). For complete details on calculating the Minimum and Maximum time, see Section 5.3 "Programming Operations".

3: These parameters are ensured by design, but are not characterized or tested in manufacturing.

TABLE 26-13: INTERNAL VOLTAGE REGULATOR SPECIFICATIONS

DC CHA	RACTERIS	STICS	(unless		se state erature	d) -40°C ≤ 1	3.0V to 3.6V $\overline{A} \le +85^{\circ}C$ for Industrial $\overline{A} \le +125^{\circ}C$ for Extended
Param No.	Symbol	Characteristics	Min	Тур	Max	Units	Comments
	Cefc	External Filter Capacitor Value ⁽¹⁾	4.7	10	_	μF	Capacitor must be low series resistance (< 5 ohms)

Note 1: Typical VCAP voltage = 2.5V when VDD \ge VDDMIN.

FIGURE 26-9: MOTOR CONTROL PWMx MODULE FAULT TIMING CHARACTERISTICS

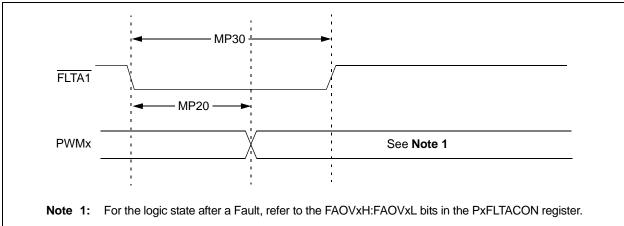


FIGURE 26-10: MOTOR CONTROL PWMx MODULE TIMING CHARACTERISTICS

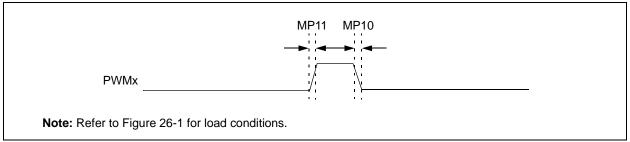


TABLE 26-28: MOTOR CONTROL PWMx MODULE TIMING REQUIREMENTS

АС СНА	RACTERIS	TICS	$\begin{array}{ll} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^\circ C \leq TA \leq +85^\circ C \mbox{ for Industrial} \\ & -40^\circ C \leq TA \leq +125^\circ C \mbox{ for Extended} \end{array}$					
Param No.	Symbol	Characteristic ⁽¹⁾	Min	Тур	Max	Units	Conditions	
MP10	TFPWM	PWM Output Fall Time	—	—	—	ns	See Parameter DO32	
MP11	TRPWM	PWM Output Rise Time	—	—		ns	See Parameter DO31	
MP20	Tfd	Fault Input ↓ to PWM I/O Change	—	—	50	ns		
MP30	Tfh	Minimum Pulse Width	50	_		ns		

Note 1: These parameters are characterized by similarity, but are not tested in manufacturing.

DC CHARACT	TERISTICS					/ (unless otherwise stated) for High Temperature
Parameter No.	Typical ⁽¹⁾	Max	Doze Ratio	Units		Conditions
Doze Current	(IDOZE) – dsF	PIC33FJ16(0	SP/MC)10X Dev	rices		
DC74a	4.3	7.2	1:2	mA	3.3V	5 MIPS
DC74f	1.6	6.2	1:64	mA	3.3V	5 MIPS
DC74g	1.5	6.2	1:128	mA	3.3V	5 MIPS
Doze Current	(IDOZE) – dsF	PIC33FJ32(0	P/MC)10X Dev	rices		
DC74a	4.7	7.2	1:2	mA	3.3V	5 MIPS
DC74f	1.9	6.2	1:64	mA	3.3V	5 MIPS
DC74g	1.4	6.2	1:128	mA	3.3V	5 MIPS

TABLE 27-7: DC CHARACTERISTICS: DOZE CURRENT (IDOZE)

Note 1: Data in the Typical column is 3.3V unless otherwise stated.

TABLE 27-8: DC CHARACTERISTICS: PROGRAM MEMORY

DC CHA	RACTER	ISTICS	(unless	otherw	ise stat e erature	ed) -40°C ≤	s: 3.0V to 3.6V TA ≤ +85°C for Industrial TA ≤ +150°C for High Temperature
Param No.	Symbol	Characteristic ⁽¹⁾	Min	Тур	Max	Units	Conditions
		Program Flash Memory					
HD130	Ер	Cell Endurance	10,000	_	_	E/W	-40°C to +150°C ⁽²⁾
HD134	Tretd	Characteristic Retention	20	—	_	Year	1000 E/W cycles or less and no other specifications are violated

Note 1: These parameters are assured by design, but are not characterized or tested in manufacturing.

2: Programming of the Flash memory is allowed up to +150°C.

TABLE 27-9: AC CHARACTERISTICS: INTERNAL FAST RC (FRC) ACCURACY

AC CHA	RACTERISTICS	Standard	Operating	Condition	s: 3.0V to 3	3.6V (unless otherwise	stated)
Param No.	Characteristic	Min	Тур	Max	Units	Conditio	ns
	Internal FRC Accura	acy @ 7.37	′ MHz ⁽¹⁾				
F20d	FRC	-8	±0.25	+8	%	$-40^{\circ}C \leq TA \leq +150^{\circ}C$	Vdd 3.0-3.6V

Note 1: Frequency is calibrated at +25°C and 3.3V. TUNx bits may be used to compensate for temperature drift.

TABLE 27-10: INTERNAL LOW-POWER RC (LPRC) ACCURACY

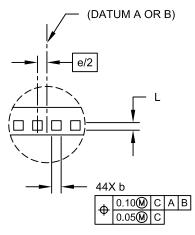
AC CHAF	RACTERISTICS	Standard	Operating	Conditio	ns: 3.0V to	o 3.6V (unless otherwise	stated)
Param No.	Characteristic	Min	Тур	Мах	Units	Condition	าร
	LPRC @ 32.768 kH	<mark>z</mark> (1,2)					
F21c	LPRC	-40	±10	+40	%	$\text{-40°C} \leq \text{TA} \leq \text{+150°C}$	VDD 3.0-3.6V

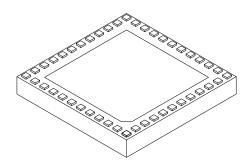
Note 1: Change of LPRC frequency as VDD changes.

2: LPRC accuracy impacts the Watchdog Timer Time-out Period (TwDT1). See Section 23.4 "Watchdog Timer (WDT)" for more information.

44-Terminal Very Thin Leadless Array Package (TL) – 6x6x0.9 mm Body With Exposed Pad [VTLA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





DETAIL A

	Units	N	ILLIMETER	S
Dimension	Limits	MIN	NOM	MAX
Number of Pins	N		44	
Number of Pins per Side	ND		12	
Number of Pins per Side	NE		10	
Pitch	е		0.50 BSC	
Overall Height	А	0.80	0.90	1.00
Standoff	A1	0.025	-	0.075
Overall Width	E		6.00 BSC	
Exposed Pad Width	E2	4.40	4.55	4.70
Overall Length	D		6.00 BSC	
Exposed Pad Length	D2	4.40	4.55	4.70
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.20	0.25	0.30
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Package is saw singulated.

3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

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