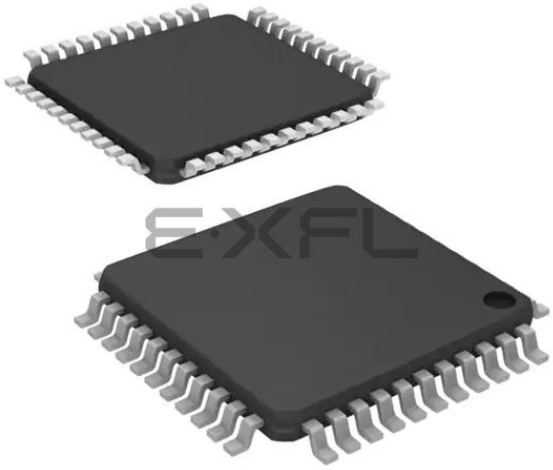

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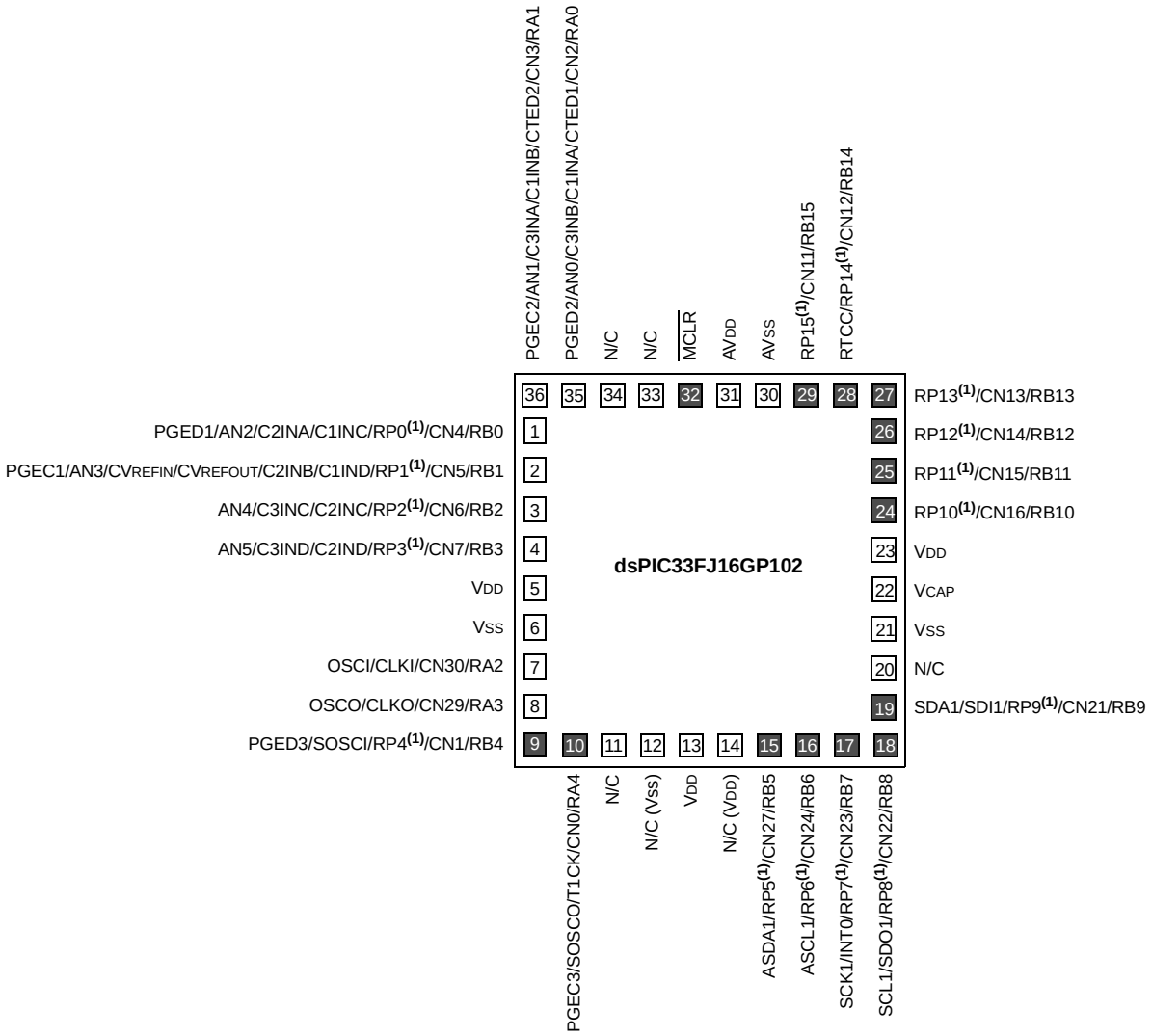
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	16 MIPs
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	35
Program Memory Size	32KB (11K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 14x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj32gp104-i-pt

Pin Diagrams (Continued)

36-Pin VTLA(2)

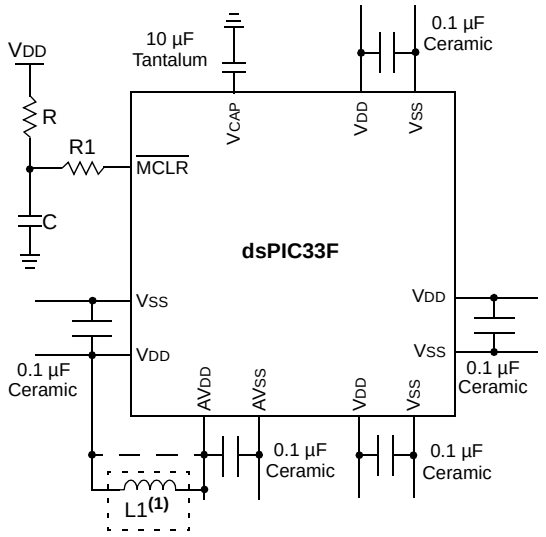
■ = Pins are up to 5V tolerant



Note 1: The RPn pins can be used by any remappable peripheral. See Table 1 for the list of available peripherals.

2: The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

FIGURE 2-1: RECOMMENDED MINIMUM CONNECTION



Note 1: As an option, instead of a hard-wired connection, an inductor (L1) can be substituted between VDD and AVDD to improve ADC noise rejection. The inductor impedance should be less than 1Ω and the inductor capacity greater than 10 mA.

Where:

$$f = \frac{F_{CNV}}{2}$$ (i.e., ADC conversion rate/2)

$$f = \frac{1}{(2\pi\sqrt{LC})}$$

$$L = \left(\frac{1}{(2\pi f\sqrt{C})}\right)^2$$

2.2.1 TANK CAPACITORS

On boards with power traces running longer than six inches in length, it is suggested to use a tank capacitor for integrated circuits including DSCs to supply a local power source. The value of the tank capacitor should be determined based on the trace resistance that connects the power supply source to the device and the maximum current drawn by the device in the application. In other words, select the tank capacitor so that it meets the acceptable voltage sag at the device. Typical values range from 4.7 µF to 47 µF.

2.3 CPU Logic Filter Capacitor Connection (VCAP)

A low-ESR (< 5 Ohms) capacitor is required on the VCAP pin, which is used to stabilize the voltage regulator output voltage. The VCAP pin must not be connected to VDD, and must have a capacitor between 4.7 µF and 10 µF, 16V connected to ground. The type can be ceramic or tantalum. Refer to **Section 26.0 "Electrical Characteristics"** for additional information.

The placement of this capacitor should be close to the VCAP. It is recommended that the trace length not exceed one-quarter inch (6 mm). Refer to **Section 23.2 "On-Chip Voltage Regulator"** for details.

2.4 Master Clear (MCLR) Pin

The MCLR pin provides two specific device functions:

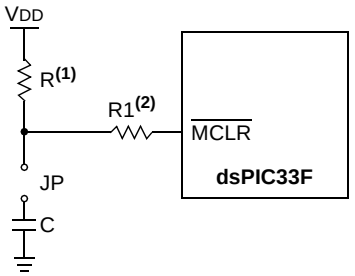
- Device Reset
- Device programming and debugging

During device programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the MCLR pin. Consequently, specific voltage levels (VIH and VIL) and fast signal transitions must not be adversely affected. Therefore, specific values of R and C will need to be adjusted based on the application and PCB requirements.

For example, as shown in Figure 2-2, it is recommended that the capacitor C, be isolated from the MCLR pin during programming and debugging operations.

Place the components shown in Figure 2-2 within one-quarter inch (6 mm) from the MCLR pin.

FIGURE 2-2: EXAMPLE OF MCLR PIN CONNECTIONS



Note 1: R ≤ 10 kΩ is recommended. A suggested starting value is 10 kΩ. Ensure that the MCLR pin VIH and VIL specifications are met.

2: R1 ≤ 470Ω will limit any current flowing into MCLR from the external capacitor, C, in the event of MCLR pin breakdown, due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS). Ensure that the MCLR pin VIH and VIL specifications are met.

3.0 CPU

Note 1: This data sheet summarizes the features of the dsPIC33FJ16(GP/MC)101/102 and dsPIC33FJ32(GP/MC)101/102/104 family devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"CPU"** (DS70204) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33FJ16(GP/MC)101/102 and dsPIC33FJ32(GP/MC)101/102/104 CPU module has a 16-bit (data) modified Harvard architecture with an enhanced instruction set, including significant support for DSP. The CPU has a 24-bit instruction word with a variable length opcode field. The Program Counter (PC) is 23 bits wide and addresses up to 4M x 24 bits of user program memory space. The actual amount of program memory implemented varies by device. A single-cycle instruction prefetch mechanism is used to help maintain throughput and provides predictable execution. All instructions execute in a single cycle, with the exception of instructions that change the program flow, the double-word move (`MOV.D`) instruction and the table instructions. Overhead-free program loop constructs are supported using the `DO` and `REPEAT` instructions, both of which are interruptible at any point.

The dsPIC33FJ16(GP/MC)101/102 and dsPIC33FJ32(GP/MC)101/102/104 devices have sixteen, 16-bit Working registers in the programmer's model. Each of the Working registers can serve as a data, address, or address offset register. The 16th Working register (W15) operates as a Software Stack Pointer (SSP) for interrupts and calls.

There are two classes of instruction in the dsPIC33FJ16(GP/MC)101/102 and dsPIC33FJ32(GP/MC)101/102/104 devices: MCU and DSP. These two instruction classes are seamlessly integrated into a single CPU. The instruction set includes many addressing modes and is designed for optimum C compiler efficiency. For most instructions, dsPIC33FJ16(GP/MC)101/102 and dsPIC33FJ32(GP/MC)101/102/104 devices are capable of executing a data (or program data) memory read, a Working register (data) read, a data memory write and a program (instruction) memory read per instruction cycle. As a result, three parameter instructions can be supported, allowing A + B = C operations to be executed in a single cycle.

A block diagram of the CPU is shown in Figure 3-1, and the programmer's model for the dsPIC33FJ16(GP/MC)101/102 and dsPIC33FJ32(GP/MC)101/102/104 is shown in Figure 3-2.

3.1 Data Addressing Overview

The data space can be addressed as 32K words or 64 Kbytes and is split into two blocks, referred to as X and Y data memory. Each memory block has its own independent Address Generation Unit (AGU). The MCU class of instructions operates solely through the X memory AGU, which accesses the entire memory map as one linear data space. Certain DSP instructions operate through the X and Y AGUs to support dual operand reads, which splits the data address space into two parts. The X and Y data space boundary is device-specific.

Overhead-free circular buffers (Modulo Addressing mode) are supported in both X and Y address spaces. The Modulo Addressing removes the software boundary checking overhead for DSP algorithms. Furthermore, the X AGU circular addressing can be used with any of the MCU class of instructions. The X AGU also supports Bit-Reversed Addressing to greatly simplify input or output data reordering for radix-2 FFT algorithms.

The upper 32 Kbytes of the data space memory map can optionally be mapped into program space at any 16K program word boundary defined by the 8-bit Program Space Visibility Page (PSVPAG) register. The program-to-data-space mapping feature lets any instruction access program space as if it were data space.

3.2 DSP Engine Overview

The DSP engine features a high-speed, 17-bit by 17-bit multiplier, a 40-bit ALU, two 40-bit saturating accumulators and a 40-bit bidirectional barrel shifter. The barrel shifter is capable of shifting a 40-bit value up to 16 bits right or left, in a single cycle. The DSP instructions operate seamlessly with all other instructions and have been designed for optimal real-time performance. The `MAC` instruction and other associated instructions can concurrently fetch two data operands from memory, while multiplying two W registers and accumulating and optionally saturating the result in the same cycle. This instruction functionality requires that the RAM data space be split for these instructions and linear for all others. Data space partitioning is achieved in a transparent and flexible manner through dedicating certain Working registers to each address space.

FIGURE 4-8: BIT-REVERSED ADDRESS EXAMPLE

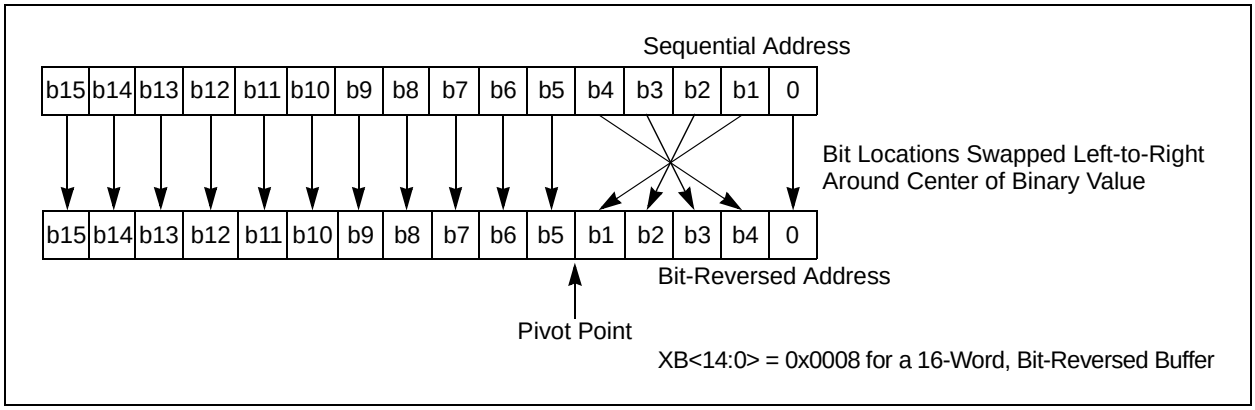


TABLE 4-41: BIT-REVERSED ADDRESS SEQUENCE (16-ENTRY)

Normal Address					Bit-Reversed Address				
A3	**A2**	**A1**	**A0**	**Decimal**	**A3**	**A2**	**A1**	**A0**	**Decimal**
0	0	0	0	0	0	0	0	0	0
0	0	0	1	1	1	0	0	0	8
0	0	1	0	2	0	1	0	0	4
0	0	1	1	3	1	1	0	0	12
0	1	0	0	4	0	0	1	0	2
0	1	0	1	5	1	0	1	0	10
0	1	1	0	6	0	1	1	0	6
0	1	1	1	7	1	1	1	0	14
1	0	0	0	8	0	0	0	1	1
1	0	0	1	9	1	0	0	1	9
1	0	1	0	10	0	1	0	1	5
1	0	1	1	11	1	1	0	1	13
1	1	0	0	12	0	0	1	1	3
1	1	0	1	13	1	0	1	1	11
1	1	1	0	14	0	1	1	1	7
1	1	1	1	15	1	1	1	1	15

REGISTER 7-5: IFS0: INTERRUPT FLAG STATUS REGISTER 0 (CONTINUED)

bit 2 **OC1IF:** Output Compare Channel 1 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 1 **IC1IF:** Input Capture Channel 1 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 0 **INT0IF:** External Interrupt 0 Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

REGISTER 7-17: IPC2: INTERRUPT PRIORITY CONTROL REGISTER 2

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	U1RXIP2	U1RXIP1	U1RXIP0	—	SPI1IP2	SPI1IP1	SPI1IP0
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	SPI1EIP2	SPI1EIP1	SPI1EIP0	—	T3IP2	T3IP1	T3IP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-12 **U1RXIP<2:0>:** UART1 Receiver Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as ‘0’

bit 10-8 **SPI1IP<2:0>:** SPI1 Event Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **SPI1EIP<2:0>:** SPI1 Error Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as ‘0’

bit 2-0 **T3IP<2:0>:** Timer3 Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

REGISTER 7-26: IPC16: INTERRUPT PRIORITY CONTROL REGISTER 16

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
—	U1EIP2	U1EIP1	U1EIP0	—	FLTB1IP2(1)	FLTB1IP1(1)	FLTB1IP0(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-7 **Unimplemented:** Read as ‘0’

bit 6-4 **U1EIP<2:0>:** UART1 Error Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as ‘0’

bit 2-0 **FLTB1IP<2:0>:** PWM1 Fault B Interrupt Priority bits(1)
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

Note 1: These bits are available in dsPIC(16/32)MC102/104 devices only.

TABLE 10-1: SELECTABLE INPUT SOURCES (MAPS INPUT TO FUNCTION)(1)

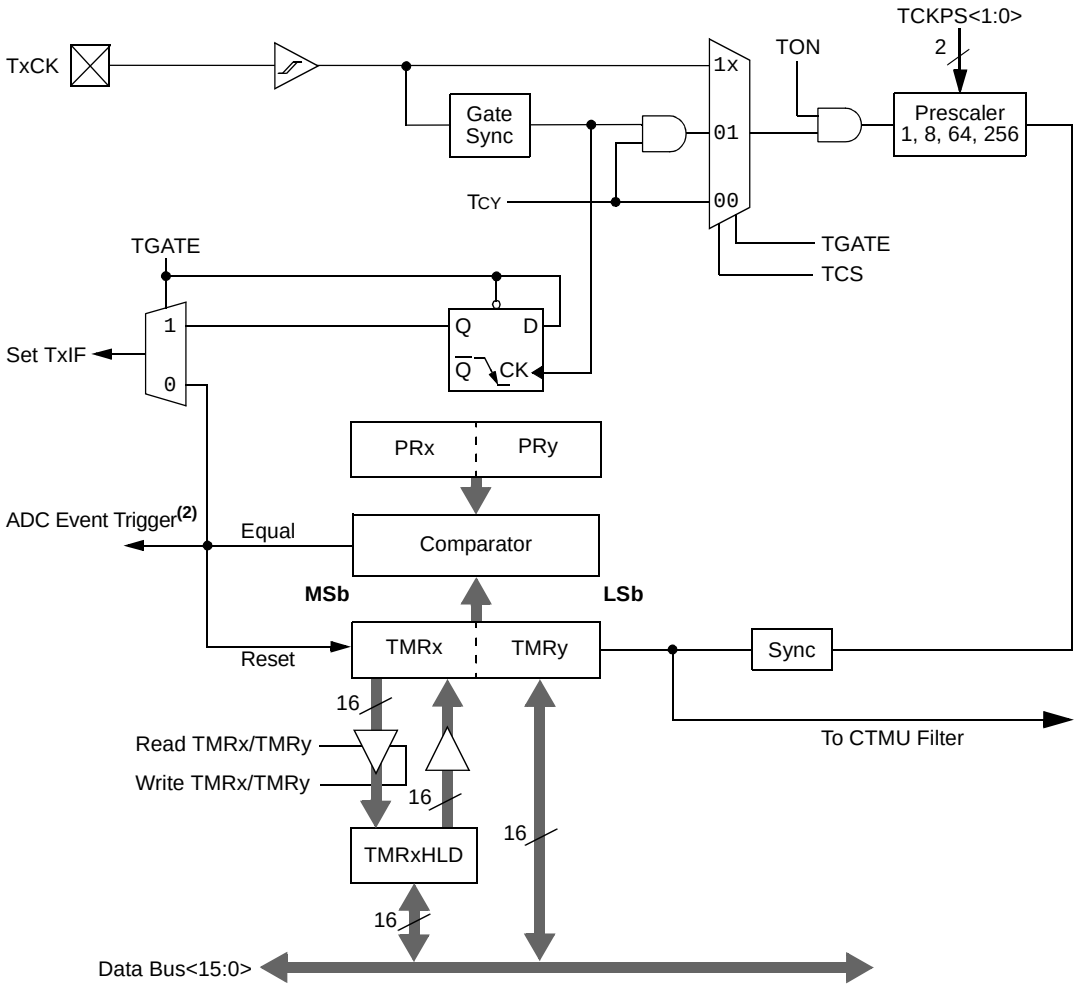
Input Name	Function Name	Register	Configuration Bits
External Interrupt 1	INT1	RPINR0	INT1R<4:0>
External Interrupt 2	INT2	RPINR1	INT2R<4:0>
Timer2 External Clock	T2CK	RPINR3	T2CKR<4:0>
Timer3 External Clock	T3CK	RPINR3	T3CKR<4:0>
Timer4 External Clock	T4CK	RPINR4	T4CKR<4:0>(2)
Timer5 External Clock	T5CK	RPINR4	T5CKR<4:0>(2)
Input Capture 1	IC1	RPINR7	IC1R<4:0>
Input Capture 2	IC2	RPINR7	IC2R<4:0>
Input Capture 3	IC3	RPINR8	IC3R<4:0>
Output Compare Fault A	OCFA	RPINR11	OCFAR<4:0>
UART1 Receive	U1RX	RPINR18	U1RXR<4:0>
UART1 Clear-to-Send	$\overline{\text{U1CTS}}$	RPINR18	U1CTSR<4:0>
SDI1 SPI Data Input 1	SDI1	RPINR20	SDI1R<4:0>(2)
SCK1 SPI Clock Input 1	SCK1	RPINR20	SCK1R<4:0>(2)
SPI1 Slave Select Input	$\overline{\text{SS1}}$	RPINR21	SS1R<4:0>(2)

Note 1: Unless otherwise noted, all inputs use the Schmitt input buffers.

2: These bits are available in dsPIC33FJ32(GP/MC)10X devices only.

NOTES:

FIGURE 12-1: TIMER2/3 AND TIMER4/5 (32-BIT) BLOCK DIAGRAM(1,3,4)



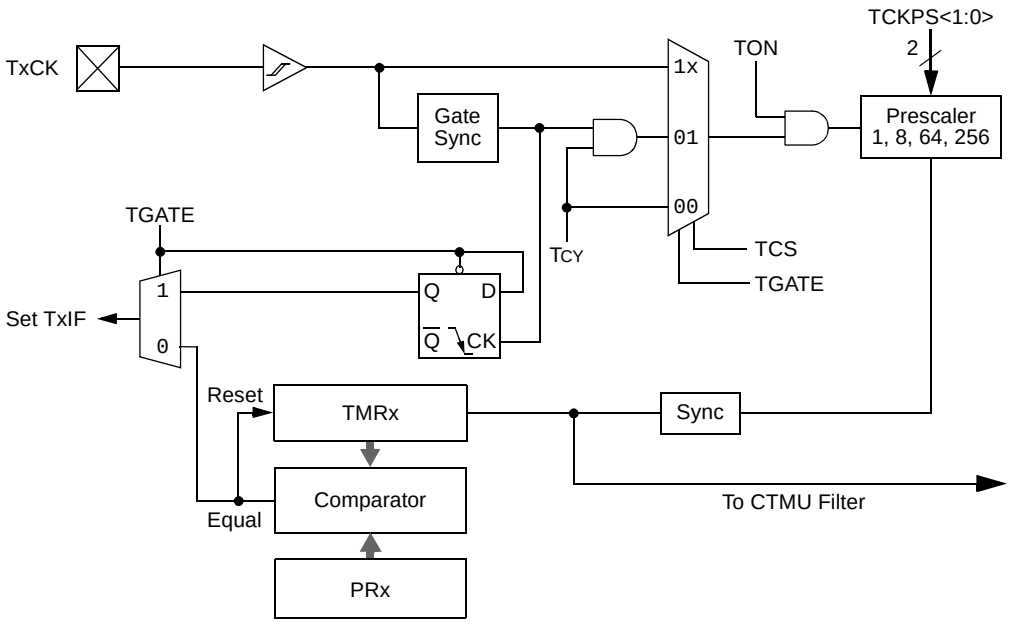
Note 1: The 32-bit timer control bit, T32, must be set for 32-bit timer/counter operation. All control bits are respective to the TxCON register.

2: The ADC event trigger is available only on Timer2/3.

3: Timer4/5 is available in dsPIC33FJ32(GP/MC)10X devices only.

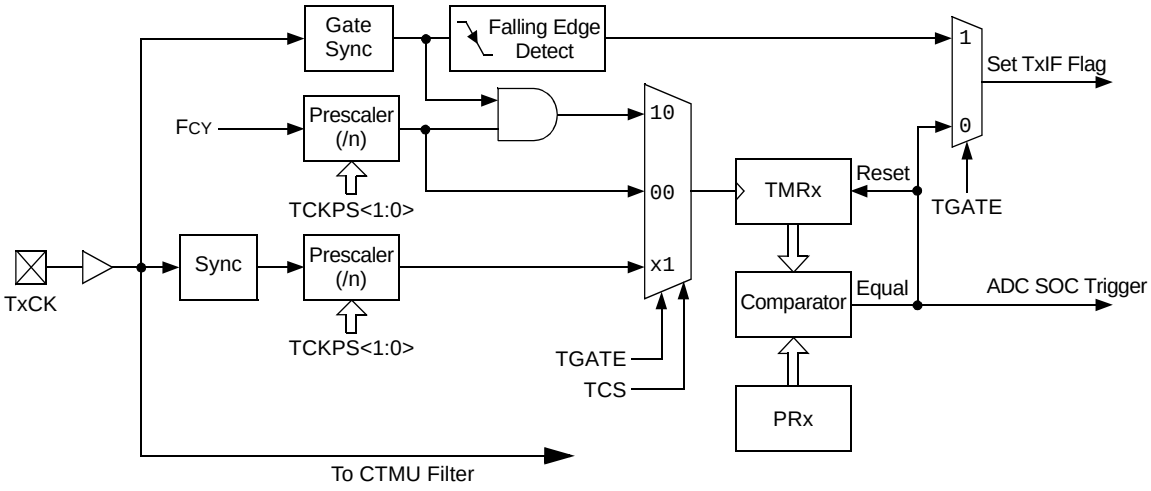
4: Where ‘x’ or ‘y’ is present, x = 2 or 4; y = 3 or 5.

FIGURE 12-2: TIMER2 AND TIMER4 (16-BIT) BLOCK DIAGRAM(1)



Note 1: Timer4 is available in dsPIC33FJ32(GP/MC)10X devices only.

FIGURE 12-3: TIMER3 AND TIMER5 (16-BIT) BLOCK DIAGRAM(1)



Note 1: Timer5 is available in dsPIC33FJ32(GP/MC)10X devices only.

REGISTER 12-3: T4CON: TIMER4 CONTROL REGISTER(1)

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
TON	—	TSIDL	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0
—	TGATE	TCKPS1	TCKPS0	T32	—	TCS	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **TON:** Timer4 On bit
When T32 = 1:
1 = Starts 32-bit Timer4/5
0 = Stops 32-bit Timer4/5
When T32 = 0:
1 = Starts 16-bit Timer4
0 = Stops 16-bit Timer4

bit 14 **Unimplemented:** Read as '0'

bit 13 **TSIDL:** Timer4 Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12-7 **Unimplemented:** Read as '0'

bit 6 **TGATE:** Timer4 Gated Time Accumulation Enable bit
When TCS = 1:
This bit is ignored.
When TCS = 0:
1 = Gated time accumulation is enabled
0 = Gated time accumulation is disabled

bit 5-4 **TCKPS<1:0>:** Timer4 Input Clock Prescale Select bits
11 = 1:256
10 = 1:64
01 = 1:8
00 = 1:1

bit 3 **T32:** 32-Bit Timer Mode Select bit
1 = Timer4 and Timer5 form a single 32-bit timer
0 = Timer4 and Timer5 act as two 16-bit timers

bit 2 **Unimplemented:** Read as '0'

bit 1 **TCS:** Timer4 Clock Source Select bit
1 = External clock from pin, T4CK (on the rising edge)
0 = Internal clock (FCY)

bit 0 **Unimplemented:** Read as '0'

Note 1: This register is available in dsPIC33FJ32(GP/MC)10X devices only.

EXAMPLE 15-1: ASSEMBLY CODE FOR WRITE-PROTECTED REGISTER UNLOCK AND FAULT CLEARING SEQUENCE

```
; FLTA1 pin must be pulled high externally in order to clear and disable the Fault
; Writing to P1FLTBCON register requires unlock sequence

mov #0xabcd,w10       ; Load first unlock key to w10 register
mov #0x4321,w11       ; Load second unlock key to w11 register
mov #0x0000,w0        ; Load desired value of P1FLTACON register in w0
mov w10, PWM1KEY      ; Write first unlock key to PWM1KEY register
mov w11, PWM1KEY      ; Write second unlock key to PWM1KEY register
mov w0,P1FLTACON      ; Write desired value to P1FLTACON register

; FLTB1 pin must be pulled high externally in order to clear and disable the Fault
; Writing to P1FLTBCON register requires unlock sequence

mov #0xabcd,w10       ; Load first unlock key to w10 register
mov #0x4321,w11       ; Load second unlock key to w11 register
mov #0x0000,w0        ; Load desired value of P1FLTBCON register in w0
mov w10, PWM1KEY      ; Write first unlock key to PWM1KEY register
mov w11, PWM1KEY      ; Write second unlock key to PWM1KEY register
mov w0,P1FLTBCON      ; Write desired value to P1FLTBCON register

; Enable all PWMs using PWM1CON1 register
; Writing to PWM1CON1 register requires unlock sequence

mov #0xabcd,w10       ; Load first unlock key to w10 register
mov #0x4321,w11       ; Load second unlock key to w11 register
mov #0x0077,w0        ; Load desired value of PWM1CON1 register in w0
mov w10, PWM1KEY      ; Write first unlock key to PWM1KEY register
mov w11, PWM1KEY      ; Write second unlock key to PWM1KEY register
mov w0,PWM1CON1       ; Write desired value to PWM1CON1 register
```

EXAMPLE 15-2: C CODE FOR WRITE-PROTECTED REGISTER UNLOCK AND FAULT CLEARING SEQUENCE

```
// FLTA1 pin must be pulled high externally in order to clear and disable the Fault
// Writing to P1FLTACON register requires unlock sequence
// Use builtin function to write 0x0000 to P1FLTACON register
__builtin_write_PWMSFR(&P1FLTACON, 0x0000, &PWM1KEY);

// FLTB1 pin must be pulled high externally in order to clear and disable the Fault
// Writing to P1FLTBCON register requires unlock sequence
// Use builtin function to write 0x0000 to P1FLTBCON register
__builtin_write_PWMSFR(&P1FLTBCON, 0x0000, &PWM1KEY);

// Enable all PWMs using PWM1CON1 register
// Writing to PWM1CON1 register requires unlock sequence
// Use builtin function to write 0x0077 to PWM1CON1 register
__builtin_write_PWMSFR(&PWM1CON1, 0x0077, &PWM1KEY);
```

15.4 PWM Control Registers

REGISTER 15-1: PxTCON: PWMx TIME BASE CONTROL REGISTER

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
PTEN	—	PTSIDL	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTOPS3	PTOPS2	PTOPS1	PTOPS0	PTCKPS1	PTCKPS0	PTMOD1	PTMOD0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **PTEN:** PWMx Time Base Timer Enable bit
1 = PWMx time base is on
0 = PWMx time base is off

bit 14 **Unimplemented:** Read as ‘0’

bit 13 **PTSIDL:** PWMx Time Base Stop in Idle Mode bit
1 = PWMx time base halts in CPU Idle mode
0 = PWMx time base runs in CPU Idle mode

bit 12-8 **Unimplemented:** Read as ‘0’

bit 7-4 **PTOPS<3:0>:** PWMx Time Base Output Postscale Select bits
1111 = 1:16 postscale
•
•
•
0001 = 1:2 postscale
0000 = 1:1 postscale

bit 3-2 **PTCKPS<1:0>:** PWMx Time Base Input Clock Prescale Select bits
11 = PWMx time base input clock period is 64 TCY (1:64 prescale)
10 = PWMx time base input clock period is 16 TCY (1:16 prescale)
01 = PWMx time base input clock period is 4 TCY (1:4 prescale)
00 = PWMx time base input clock period is TCY (1:1 prescale)

bit 1-0 **PTMOD<1:0>:** PWMx Time Base Mode Select bits
11 = PWMx time base operates in a Continuous Up/Down Count mode with interrupts for double PWM updates
10 = PWMx time base operates in a Continuous Up/Down Count mode
01 = PWMx time base operates in Single Pulse mode
00 = PWMx time base operates in a Free-Running mode

REGISTER 15-7: PxDTCON1: PWMx DEAD-TIME CONTROL REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DTBPS1	DTBPS0	DTB5	DTB4	DTB3	DTB2	DTB1	DTB0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DTAPS1	DTAPS0	DTA5	DTA4	DTA3	DTA2	DTA1	DTA0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

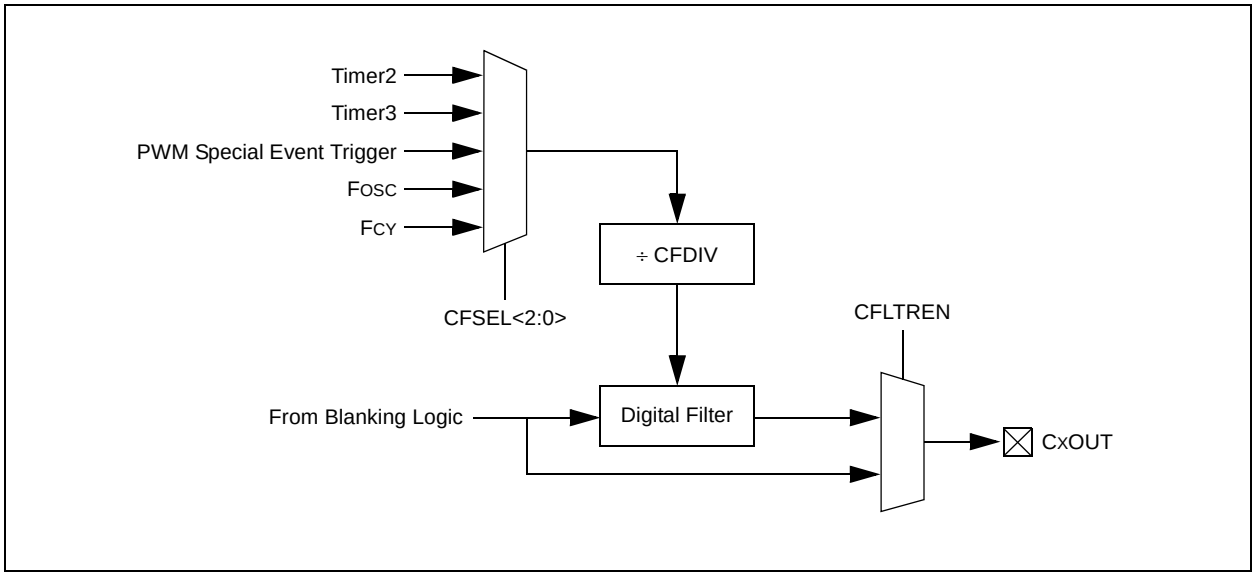
bit 15-14 **DTBPS<1:0>:** Dead-Time Unit B Prescale Select bits
11 = Clock period for Dead-Time Unit B is 8 TCY
10 = Clock period for Dead-Time Unit B is 4 TCY
01 = Clock period for Dead-Time Unit B is 2 TCY
00 = Clock period for Dead-Time Unit B is TCY

bit 13-8 **DTB<5:0>:** Unsigned 6-Bit Dead-Time Value for Dead-Time Unit B bits

bit 7-6 **DTAPS<1:0>:** Dead-Time Unit A Prescale Select bits
11 = Clock period for Dead-Time Unit A is 8 TCY
10 = Clock period for Dead-Time Unit A is 4 TCY
01 = Clock period for Dead-Time Unit A is 2 TCY
00 = Clock period for Dead-Time Unit A is TCY

bit 5-0 **DTA<5:0>:** Unsigned 6-Bit Dead-Time Value for Dead-Time Unit A bits

FIGURE 20-4: DIGITAL FILTER INTERCONNECT BLOCK DIAGRAM



REGISTER 20-3: CMxMSKSRC: COMPARATOR x MASK SOURCE SELECT REGISTER (CONTINUED)

bit 3-0 **SELSRCA<3:0>:** Mask A Input Select bits

1111 = Reserved
1110 = Reserved
1101 = Reserved
1100 = Reserved
1011 = Reserved
1010 = Reserved
1001 = Reserved
1000 = Reserved
0111 = Reserved
0110 = Reserved
0101 = PWM1H3
0100 = PWM1L3
0011 = PWM1H2
0010 = PWM1L2
0001 = PWM1H1
0000 = PWM1L1

TABLE 26-10: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
	VIL	**Input Low Voltage**					
DI10		I/O Pins	VSS	—	0.2 VDD	V	
DI15		$\overline{\text{MCLR}}$	VSS	—	0.2 VDD	V	
DI18		I/O Pins with SDAx, SCLx	VSS	—	0.3 VDD	V	SMBus disabled
DI19		I/O Pins with SDAx, SCLx	VSS	—	0.8	V	SMBus enabled
	VIH	**Input High Voltage**					
DI20		I/O Pins Not 5V Tolerant(4) I/O Pins 5V Tolerant(4)	0.7 VDD 0.7 VDD	— —	VDD 5.5	V V	
DI28		SDAx, SCLx	0.7 VDD	—	5.5	V	SMBus disabled
DI29		SDAx, SCLx	2.1	—	5.5	V	SMBus enabled
	ICNPU	**CNx Pull-up Current**					
DI30			50	250	450	µA	VDD = 3.3V, VPIN = VSS
	IIL	**Input Leakage Current(2,3)**					
DI50		I/O Pins 5V Tolerant(4)	—	—	±2	µA	VSS ≤ VPIN ≤ VDD, Pin at high-impedance
DI51		I/O Pins Not 5V Tolerant(4)	—	—	±1	µA	VSS ≤ VPIN ≤ VDD, Pin at high-impedance, -40°C ≤ TA ≤ +85°C
DI51a		I/O Pins Not 5V Tolerant(4)	—	—	±2	µA	Shared with external reference pins, -40°C ≤ TA ≤ +85°C
DI51b		I/O Pins Not 5V Tolerant(4)	—	—	±3.5	µA	VSS ≤ VPIN ≤ VDD, Pin at high-impedance, -40°C ≤ TA ≤ +125°C
DI51c		I/O Pins Not 5V Tolerant(4)	—	—	±8	µA	Analog pins shared with external reference pins, -40°C ≤ TA ≤ +125°C
DI55		$\overline{\text{MCLR}}$	—	—	±2	µA	VSS ≤ VPIN ≤ VDD
DI56		OSC1	—	—	±2	µA	VSS ≤ VPIN ≤ VDD, XT and HS modes

Note 1: Data in “Typ” column is at 3.3V, +25°C unless otherwise stated.

2: The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current can be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

4: See the **“Pin Diagrams”** section for the 5V tolerant I/O pins.

5: VIL source < (VSS – 0.3). Characterized but not tested.

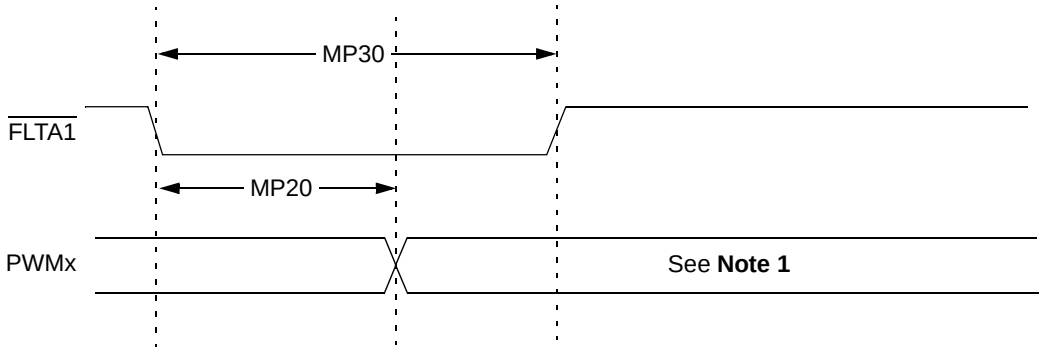
6: Non-5V tolerant pins, VIH source > (VDD + 0.3), 5V tolerant pins, VIH source > 5.5V. Characterized but not tested.

7: Digital 5V tolerant pins cannot tolerate any “positive” input injection current from input sources > 5.5V.

8: Injection currents > | 0 | can affect the ADC results by approximately 4-6 counts.

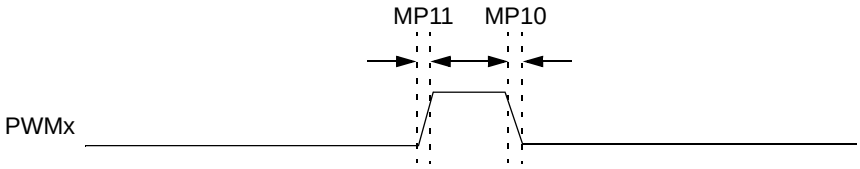
9: Any number and/or combination of I/O pins, not excluded under IICL or IICH conditions, are permitted provided the mathematical “absolute instantaneous” sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.

FIGURE 26-9: MOTOR CONTROL PWMx MODULE FAULT TIMING CHARACTERISTICS



Note 1: For the logic state after a Fault, refer to the FAOVxH:FAOVxL bits in the PxFLTACON register.

FIGURE 26-10: MOTOR CONTROL PWMx MODULE TIMING CHARACTERISTICS



Note: Refer to Figure 26-1 for load conditions.

TABLE 26-28: MOTOR CONTROL PWMx MODULE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic(1)**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
MP10	TFPWM	PWM Output Fall Time	—	—	—	ns	See Parameter DO32
MP11	TRPWM	PWM Output Rise Time	—	—	—	ns	See Parameter DO31
MP20	TFD	Fault Input ↓ to PWM I/O Change	—	—	50	ns	
MP30	TFH	Minimum Pulse Width	50	—	—	ns	

Note 1: These parameters are characterized by similarity, but are not tested in manufacturing.

TABLE 26-50: COMPARATOR TIMING SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ**	**Max.**	**Units**	**Conditions**
300	TRESP	Response Time(1,2)	—	150	400	ns	
301	TMC2OV	Comparator Mode Change to Output Valid(1)	—	—	10	µs	
302	TON2OV	Comparator Enabled to Output Valid(1)	—	—	10	µs	

Note 1: Parameters are characterized but not tested.

2: Response time is measured with one comparator input at (VDD – 1.5)/2, while the other input transitions from VSS to VDD.

TABLE 26-51: COMPARATOR MODULE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ**	**Max.**	**Units**	**Conditions**
D300	VIOFF	Input Offset Voltage(1)	-20	±10	20	mV	
D301	VICM	Input Common-Mode Voltage(1)	0	—	AVDD – 1.5V	V	
D302	CMRR	Common-Mode Rejection Ratio(1)	-54	—	—	dB	
D305	IVREF	Internal Voltage Reference(1)	1.116	1.24	1.364	V	

Note 1: Parameters are characterized but not tested.

TABLE 26-52: COMPARATOR VOLTAGE REFERENCE SETTLING TIME SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ**	**Max.**	**Units**	**Conditions**
VR310	TSET	Settling Time(1)	—	—	10	µs	

Note 1: Settling time measured while CVRR = 1 and the CVR<3:0> bits transition from '0000' to '1111'.