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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	dsPIC
Core Size	16-Bit
Speed	16 MIPs
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, Motor Control PWM, POR, PWM, WDT
Number of I/O	15
Program Memory Size	32KB (11K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	20-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj32mc101-e-p

NOTES:

4.2.6 SOFTWARE STACK

In addition to its use as a working register, the W15 register in the dsPIC33FJ16(GP/MC)101/102 and dsPIC33FJ32(GP/MC)101/102/104 devices is also used as a Software Stack Pointer. The Stack Pointer always points to the first available free word and grows from lower to higher addresses. It pre-decrements for stack pops and post-increments for stack pushes, as shown in Figure 4-6. For a PC push during any CALL instruction, the MSb of the PC is zero-extended before the push, ensuring that the MSb is always clear.

Note:	A PC push during exception processing concatenates the SRL register to the MSb of the PC prior to the push.

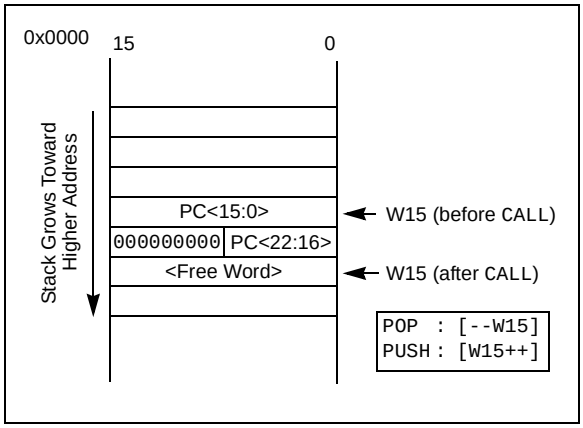
The Stack Pointer Limit register (SPLIM) associated with the Stack Pointer sets an upper address boundary for the stack. SPLIM is uninitialized at Reset. As is the case for the Stack Pointer, SPLIM<0> is forced to '0' because all stack operations must be word-aligned.

Whenever an EA is generated using W15 as a source or destination pointer, the resulting address is compared with the value in SPLIM. If the contents of the Stack Pointer (W15) and the SPLIM register are equal and a push operation is performed, a stack error trap will not occur. However, the stack error trap will occur on a subsequent push operation. For example, to cause a stack error trap when the stack grows beyond address 0x0C00 in RAM, initialize the SPLIM with the value 0x0BFE.

Similarly, a Stack Pointer underflow (stack error) trap is generated when the Stack Pointer address is found to be less than 0x0800. This prevents the stack from interfering with the SFR space.

A write to the SPLIM register should not be immediately followed by an indirect read operation using W15.

FIGURE 4-6: CALL STACK FRAME



4.2.7 DATA RAM PROTECTION FEATURE

The dsPIC33F product family supports data RAM protection features that enable segments of RAM to be protected when used in conjunction with Boot and Secure Code Segment Security. BSRAM (Secure RAM Segment for BS) is accessible only from the Boot Segment Flash code when enabled. SSRAM (Secure RAM Segment for RAM) is accessible only from the Secure Segment Flash code when enabled. See Table 4-1 for an overview of the BSRAM and SSRAM SFRs.

4.3 Instruction Addressing Modes

The addressing modes shown in Table 4-40 form the basis of the addressing modes that are optimized to support the specific features of individual instructions. The addressing modes provided in the MAC class of instructions differ from those provided in other instruction types.

4.3.1 FILE REGISTER INSTRUCTIONS

Most file register instructions use a 13-bit address field (f) to directly address data present in the first 8192 bytes of data memory (Near Data Space). Most file register instructions employ a Working register, W0, which is denoted as WREG in these instructions. The destination is typically either the same file register or WREG (with the exception of the MUL instruction), which writes the result to a register or register pair. The MOV instruction allows additional flexibility and can access the entire data space.

4.3.2 MCU INSTRUCTIONS

The three-operand MCU instructions are of the form:

```
Operand 3 = Operand 1 <function> Operand 2
```

where Operand 1 is always a Working register (that is, the addressing mode can only be Register Direct), which is referred to as Wb. Operand 2 can be a W register, fetched from data memory, or a 5-bit literal. The result location can be either a W register or a data memory location. The following addressing modes are supported by MCU instructions:

- Register Direct
- Register Indirect
- Register Indirect Post-Modified
- Register Indirect Pre-Modified
- 5-Bit or 10-Bit Literal

Note:	Not all instructions support all of the addressing modes given above. Individual instructions can support different subsets of these addressing modes.

6.3 POR

A POR circuit ensures the device is reset from power-on. The POR circuit is active until VDD crosses the VPOR threshold and the delay, TPOR, has elapsed. The delay, TPOR, ensures that the internal device bias circuits become stable.

The device supply voltage characteristics must meet the specified starting voltage and rise rate requirements to generate the POR. Refer to **Section 26.0 "Electrical Characteristics"** for details.

The Power-on Reset (POR) status bit in the Reset Control (RCON<0>) register is set to indicate the Power-on Reset.

6.4 BOR and PWRT

The on-chip regulator has a BOR circuit that resets the device when the VDD is too low (VDD < VBOR) for proper device operation. The BOR circuit keeps the device in Reset until VDD crosses the VBOR threshold and the delay, TBOR, has elapsed. The delay, TBOR, ensures the voltage regulator output becomes stable.

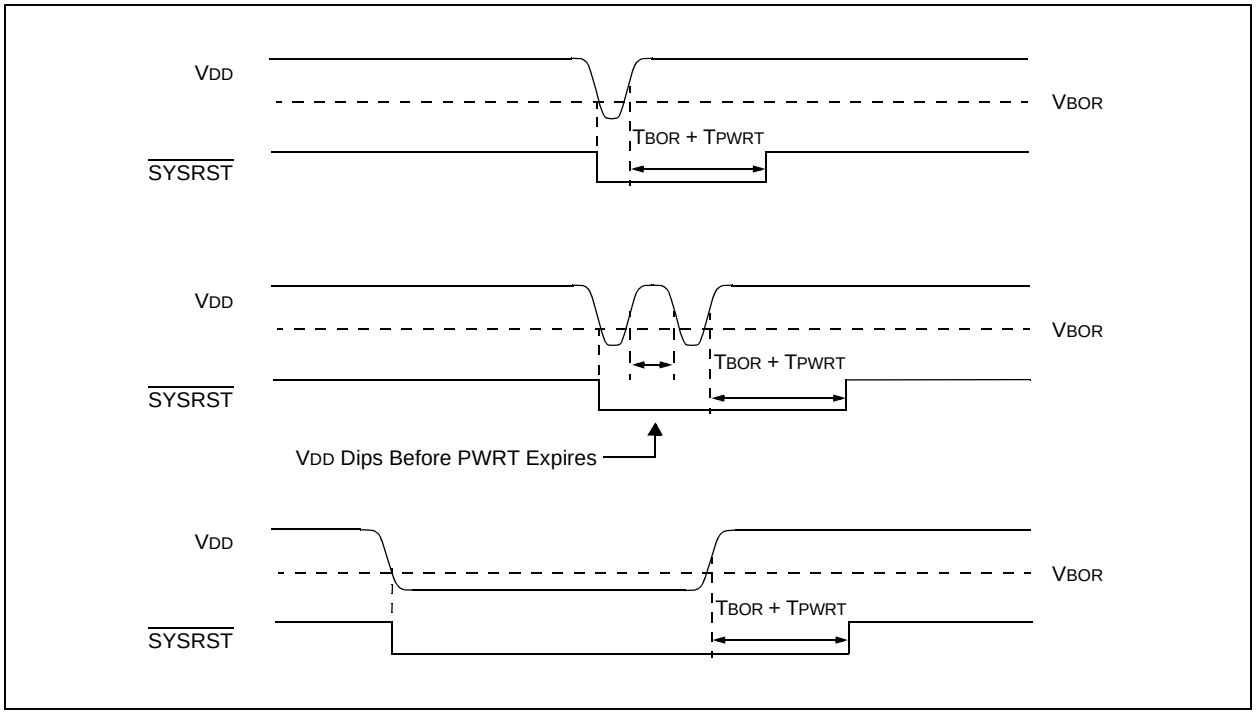
The Brown-out Reset (BOR) status bit in the Reset Control (RCON<1>) register is set to indicate the Brown-out Reset.

The device will not run at full speed after a BOR as the VDD should rise to acceptable levels for full-speed operation. The Power-up Timer (PWRT) provides power-up time delay (TPWRT) to ensure that the system power supplies have stabilized at the appropriate levels for full-speed operation before the $\overline{\text{SYSRST}}$ is released.

Refer to **Section 23.0 "Special Features"** for further details.

Figure 6-3 shows the typical brown-out scenarios. The Reset delay (TBOR + TPWRT) is initiated each time VDD rises above the VBOR trip point.

FIGURE 6-3: BROWN-OUT RESET SITUATIONS



REGISTER 7-3: INTCON1: INTERRUPT CONTROL REGISTER 1 (CONTINUED)

bit 3 **ADDRERR:** Address Error Trap Status bit
1 = Address error trap has occurred
0 = Address error trap has not occurred

bit 2 **STKERR:** Stack Error Trap Status bit
1 = Stack error trap has occurred
0 = Stack error trap has not occurred

bit 1 **OSCFAIL:** Oscillator Failure Trap Status bit
1 = Oscillator failure trap has occurred
0 = Oscillator failure trap has not occurred

bit 0 **Unimplemented:** Read as '0'

REGISTER 7-14: IEC4: INTERRUPT ENABLE CONTROL REGISTER 4

U-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
—	—	CTMUIE	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	U1EIE	FLTB1IE(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **CTMUIE:** CTMU Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 12-2 **Unimplemented:** Read as '0'

bit 1 **U1EIE:** UART1 Error Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 0 **FLTB1IE:** PWM1 Fault B Interrupt Enable bit(1)
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

Note 1: This bit is available in dsPIC(16/32)MC102/104 devices only.

9.2.2 IDLE MODE

The following occurs in Idle mode:

- The CPU stops executing instructions.
- The WDT is automatically cleared.
- The system clock source remains active. By default, all peripheral modules continue to operate normally from the system clock source, but can also be selectively disabled (see **Section 9.4 "Peripheral Module Disable"**).
- If the WDT or FSCM is enabled, the LPRC also remains active.

The device will wake from Idle mode on any of these events:

- Any interrupt that is individually enabled
- Any device Reset
- A WDT time-out

On wake-up from Idle mode, the clock is reapplied to the CPU and instruction execution will begin (2-4 clock cycles later), starting with the instruction following the PWRSAV instruction, or the first instruction in the ISR.

9.2.3 INTERRUPTS COINCIDENT WITH POWER SAVE INSTRUCTIONS

Any interrupt that coincides with the execution of a PWRSAV instruction is held off until entry into Sleep or Idle mode has completed. The device then wakes up from Sleep or Idle mode.

9.3 Doze Mode

The preferred strategies for reducing power consumption are changing clock speed and invoking one of the power-saving modes. In some circumstances, this may not be practical. For example, it may be necessary for an application to maintain uninterrupted synchronous communication, even while it is doing nothing else. Reducing system clock speed can introduce communication errors, while using a power-saving mode can stop communications completely.

Doze mode is a simple and effective alternative method to reduce power consumption while the device is still executing code. In this mode, the system clock continues to operate from the same source and at the same speed. Peripheral modules continue to be clocked at the same speed, while the CPU clock speed is reduced. Synchronization between the two clock domains is maintained, allowing the peripherals to access the SFRs while the CPU executes code at a slower rate.

Doze mode is enabled by setting the DOZEN bit (CLKDIV<11>). The ratio between peripheral and core clock speed is determined by the DOZE<2:0> bits (CLKDIV<14:12>). There are eight possible configurations, from 1:1 to 1:128, with 1:1 being the default setting.

Programs can use Doze mode to selectively reduce power consumption in event-driven applications. This allows clock-sensitive functions, such as synchronous communications, to continue without interruption while the CPU Idles, waiting for something to invoke an interrupt routine. An automatic return to full-speed CPU operation on interrupts can be enabled by setting the ROI bit (CLKDIV<15>). By default, interrupt events have no effect on Doze mode operation.

For example, suppose the device is operating at 20 MIPS and the UART module has been configured for 500 kbps based on this device operating speed. If the device is placed in Doze mode with a clock frequency ratio of 1:4, the UART module continues to communicate at the required bit rate of 500 kbps, but the CPU now starts executing instructions at a frequency of 5 MIPS.

9.4 Peripheral Module Disable

The Peripheral Module Disable (PMDx) registers provide a method to disable a peripheral module by stopping all clock sources supplied to that module. When a peripheral is disabled using the appropriate PMDx control bit, the peripheral is in a minimum power consumption state. The control and status registers associated with the peripheral are also disabled, so writes to those registers will have no effect and read values will be invalid.

A peripheral module is enabled only if both the associated bit in the PMDx register is cleared and the peripheral is supported by the specific dsPIC® DSC variant. If the peripheral is present in the device, it is enabled in the PMDx register by default.

Note:	If a PMDx bit is set, the corresponding module is disabled after a delay of one instruction cycle. Similarly, if a PMDx bit is cleared, the corresponding module is enabled after a delay of one instruction cycle (assuming the module control registers are already configured to enable module operation).

9.5 PMD Control Registers

REGISTER 9-1: PMD1: PERIPHERAL MODULE DISABLE CONTROL REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0
T5MD(1)	T4MD(1)	T3MD	T2MD	T1MD	—	PWM1MD	—
bit 15							bit 8

R/W-0	U-0	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0
I2C1MD	—	U1MD	—	SPI1MD	—	—	AD1MD(2)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **T5MD:** Timer5 Module Disable bit(1)
1 = Timer5 module is disabled
0 = Timer5 module is enabled

bit 14 **T4MD:** Timer4 Module Disable bit(1)
1 = Timer4 module is disabled
0 = Timer4 module is enabled

bit 13 **T3MD:** Timer3 Module Disable bit
1 = Timer3 module is disabled
0 = Timer3 module is enabled

bit 12 **T2MD:** Timer2 Module Disable bit
1 = Timer2 module is disabled
0 = Timer2 module is enabled

bit 11 **T1MD:** Timer1 Module Disable bit
1 = Timer1 module is disabled
0 = Timer1 module is enabled

bit 10 **Unimplemented:** Read as '0'

bit 9 **PWM1MD:** PWM1 Module Disable bit
1 = PWM1 module is disabled
0 = PWM1 module is enabled

bit 8 **Unimplemented:** Read as '0'

bit 7 **I2C1MD:** I2C1 Module Disable bit
1 = I2C1 module is disabled
0 = I2C1 module is enabled

bit 6 **Unimplemented:** Read as '0'

bit 5 **U1MD:** UART1 Module Disable bit
1 = UART1 module is disabled
0 = UART1 module is enabled

bit 4 **Unimplemented:** Read as '0'

Note 1: These bits are available in dsPIC33FJ32(GP/MC)10X devices only.

2: PCFGx bits have no effect if the ADC module is disabled by setting this bit. When the bit is set, all port pins that have been multiplexed with ANx will be in Digital mode.

10.7 Peripheral Pin Select Registers

The dsPIC33FJ16(GP/MC)101/102 and dsPIC33FJ32(GP/MC)101/102/104 family of devices implements up to 23 registers for remappable peripheral configuration.

Note: Input and output register values can only be changed if IOLOCK (OSCCON<6>) = 0. See **Section 10.4.3.1 "Control Register Lock"** for a specific command sequence.

REGISTER 10-1: RPINR0: PERIPHERAL PIN SELECT INPUT REGISTER 0

U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	—	INT1R4	INT1R3	INT1R2	INT1R1	INT1R0
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **INT1R<4:0>:** Assign External Interrupt 1 (INTR1) to the Corresponding RPn Pin bits

11111 = Input tied to Vss
11110 = Reserved
.
.
.
11010 = Reserved
11001 = Input tied to RP25
.
.
.
00001 = Input tied to RP1
00000 = Input tied to RP0

bit 7-0 **Unimplemented:** Read as '0'

EXAMPLE 15-1: ASSEMBLY CODE FOR WRITE-PROTECTED REGISTER UNLOCK AND FAULT CLEARING SEQUENCE

```
; FLTA1 pin must be pulled high externally in order to clear and disable the Fault
; Writing to P1FLTBCON register requires unlock sequence

mov #0xabcd,w10       ; Load first unlock key to w10 register
mov #0x4321,w11       ; Load second unlock key to w11 register
mov #0x0000,w0        ; Load desired value of P1FLTACON register in w0
mov w10, PWM1KEY      ; Write first unlock key to PWM1KEY register
mov w11, PWM1KEY      ; Write second unlock key to PWM1KEY register
mov w0,P1FLTACON      ; Write desired value to P1FLTACON register

; FLTB1 pin must be pulled high externally in order to clear and disable the Fault
; Writing to P1FLTBCON register requires unlock sequence

mov #0xabcd,w10       ; Load first unlock key to w10 register
mov #0x4321,w11       ; Load second unlock key to w11 register
mov #0x0000,w0        ; Load desired value of P1FLTBCON register in w0
mov w10, PWM1KEY      ; Write first unlock key to PWM1KEY register
mov w11, PWM1KEY      ; Write second unlock key to PWM1KEY register
mov w0,P1FLTBCON      ; Write desired value to P1FLTBCON register

; Enable all PWMs using PWM1CON1 register
; Writing to PWM1CON1 register requires unlock sequence

mov #0xabcd,w10       ; Load first unlock key to w10 register
mov #0x4321,w11       ; Load second unlock key to w11 register
mov #0x0077,w0        ; Load desired value of PWM1CON1 register in w0
mov w10, PWM1KEY      ; Write first unlock key to PWM1KEY register
mov w11, PWM1KEY      ; Write second unlock key to PWM1KEY register
mov w0,PWM1CON1       ; Write desired value to PWM1CON1 register
```

EXAMPLE 15-2: C CODE FOR WRITE-PROTECTED REGISTER UNLOCK AND FAULT CLEARING SEQUENCE

```
// FLTA1 pin must be pulled high externally in order to clear and disable the Fault
// Writing to P1FLTACON register requires unlock sequence
// Use builtin function to write 0x0000 to P1FLTACON register
__builtin_write_PWMSFR(&P1FLTACON, 0x0000, &PWM1KEY);

// FLTB1 pin must be pulled high externally in order to clear and disable the Fault
// Writing to P1FLTBCON register requires unlock sequence
// Use builtin function to write 0x0000 to P1FLTBCON register
__builtin_write_PWMSFR(&P1FLTBCON, 0x0000, &PWM1KEY);

// Enable all PWMs using PWM1CON1 register
// Writing to PWM1CON1 register requires unlock sequence
// Use builtin function to write 0x0077 to PWM1CON1 register
__builtin_write_PWMSFR(&PWM1CON1, 0x0077, &PWM1KEY);
```

REGISTER 15-5: PWMxCON1: PWMx CONTROL REGISTER 1(1)

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	PMOD3	PMOD2	PMOD1
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
—	PEN3H(2)	PEN2H(2)	PEN1H(2)	—	PEN3L(2)	PEN2L(2)	PEN1L(2)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-11 **Unimplemented:** Read as '0'

bit 10-8 **PMOD<3:1>:** PWMx I/O Pair Mode bits
1 = PWMx I/O pin pair is in the Independent PWM Output mode
0 = PWMx I/O pin pair is in the Complementary Output mode

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **PEN3H:PEN1H:** PWMxH I/O Enable bits(2)
1 = PWMxH pin is enabled for PWMx output
0 = PWMxH pin is disabled, I/O pin becomes a general purpose I/O

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **PEN3L:PEN1L:** PWMxL I/O Enable bits(2)
1 = PWMxL pin is enabled for PWMx output
0 = PWMxL pin is disabled, I/O pin becomes a general purpose I/O

Note 1: The PWMxCON1 register is a write-protected register. Refer to **Section 15.3 "Write-Protected Registers"** for more information on the unlock sequence.

2: The Reset status for these bits depends on the setting of the PWMPIN Configuration bit (FPOR<7>):
- If PWMPIN = 1 (default), the PWM pins are controlled by the PORT register at Reset, meaning they are initially programmed as inputs (i.e., tri-stated).
- If PWMPIN = 0, the PWM pins are controlled by the PWM module at Reset and are therefore, initially programmed as output pins.

NOTES:

REGISTER 21-8: ALRMVAL (WHEN ALRMPTR<1:0> = 10): ALARM MONTH AND DAY VALUE REGISTER(1)

U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—	MTHTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0
bit 15							bit 8

U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	DAYTEN1	DAYTEN0	DAYONE3	DAYONE2	DAYONE1	DAYONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12 **MTHTEN0:** Binary Coded Decimal Value of Month's Tens Digit bit
Contains a value of 0 or 1.

bit 11-8 **MTHONE<3:0>:** Binary Coded Decimal Value of Month's Ones Digit bits
Contains a value from 0 to 9.

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **DAYTEN<1:0>:** Binary Coded Decimal Value of Day's Tens Digit bits
Contains a value from 0 to 3.

bit 3-0 **DAYONE<3:0>:** Binary Coded Decimal Value of Day's Ones Digit bits
Contains a value from 0 to 9.

Note 1: A write to this register is only allowed when RTCWREN = 1.

22.0 CHARGE TIME MEASUREMENT UNIT (CTMU)

Note 1: This data sheet summarizes the features of the dsPIC33FJ16(GP/MC)101/102 and dsPIC33FJ32(GP/MC)101/102/104 device families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Charge Time Measurement Unit (CTMU)"** (DS70635) in the "*dsPIC33/PIC24 Family Reference Manual*", which is available on the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The Charge Time Measurement Unit (CTMU) is a flexible analog module that provides accurate differential time measurement between pulse sources, as well as asynchronous pulse generation. Its key features include:

- Four edge input trigger sources
- Polarity control for each edge source
- Control of edge sequence
- Control of response to edges
- Precise time measurement resolution of 200 ps
- Accurate current source suitable for capacitive measurement
- On-chip temperature measurement using a built-in diode

Together with other on-chip analog modules, the CTMU can be used to precisely measure time, measure capacitance, measure relative changes in capacitance or generate output pulses that are independent of the system clock.

The CTMU module is ideal for interfacing with capacitive-based sensors. The CTMU is controlled through three registers: CTMUCON1, CTMUCON2 and CTMUICON. CTMUCON1 enables the module, the edge delay generation, sequencing of edges, and controls the current source and the output trigger. CTMUCON2 controls the edge source selection, edge source polarity selection and edge sampling mode. The CTMUICON register controls the selection and trim of the current source.

Figure 22-1 shows the CTMU block diagram.

TABLE 24-1: SYMBOLS USED IN OPCODE DESCRIPTIONS (CONTINUED)

Field	Description
Wm*Wm	Multiplicand and Multiplier Working register pair for Square instructions ∈ {W4 * W4,W5 * W5,W6 * W6,W7 * W7}
Wm*Wn	Multiplicand and Multiplier Working register pair for DSP instructions ∈ {W4 * W5,W4 * W6,W4 * W7,W5 * W6,W5 * W7,W6 * W7}
Wn	One of 16 Working registers ∈ {W0..W15}
Wnd	One of 16 destination Working registers ∈ {W0..W15}
Wns	One of 16 source Working registers ∈ {W0..W15}
WREG	W0 (Working register used in file register instructions)
Ws	Source W register ∈ { Ws, [Ws], [Ws++], [Ws--], [++Ws], [--Ws] }
Wso	Source W register ∈ { Wns, [Wns], [Wns++], [Wns--], [++Wns], [--Wns], [Wns+Wb] }
Wx	X data space prefetch address register for DSP instructions ∈ {[W8] + = 6, [W8] + = 4, [W8] + = 2, [W8], [W8] - = 6, [W8] - = 4, [W8] - = 2, [W9] + = 6, [W9] + = 4, [W9] + = 2, [W9], [W9] - = 6, [W9] - = 4, [W9] - = 2, [W9 + W12], none}
Wxd	X data space prefetch destination register for DSP instructions ∈ {W4..W7}
Wy	Y data space prefetch address register for DSP instructions ∈ {[W10] + = 6, [W10] + = 4, [W10] + = 2, [W10], [W10] - = 6, [W10] - = 4, [W10] - = 2, [W11] + = 6, [W11] + = 4, [W11] + = 2, [W11], [W11] - = 6, [W11] - = 4, [W11] - = 2, [W11 + W12], none}
Wyd	Y data space prefetch destination register for DSP instructions ∈ {W4..W7}

FIGURE 26-2: EXTERNAL CLOCK TIMING

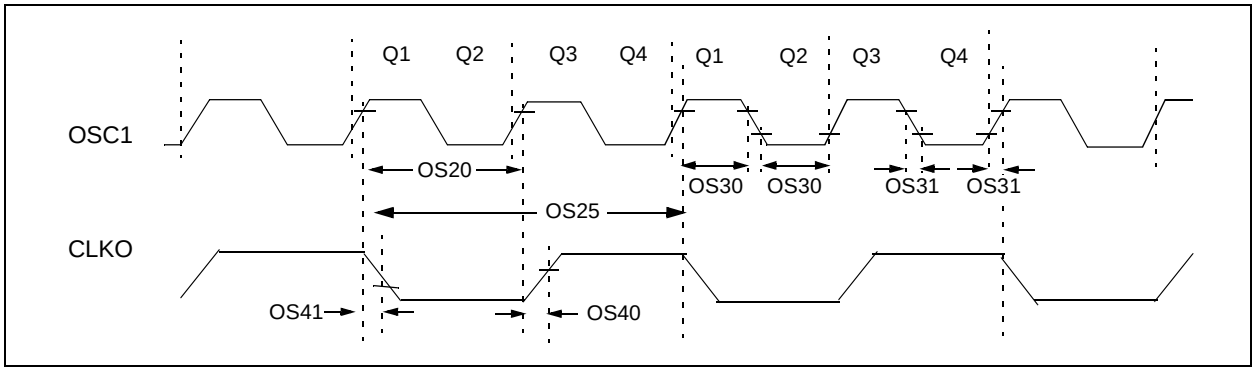


TABLE 26-16: EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symb**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
OS10	FIN	External CLKI Frequency (External clocks allowed only in EC and ECPLL modes)	DC	—	32	MHz	EC
		Oscillator Crystal Frequency	3.0 10 31	— — —	10 32 33	MHz MHz kHz	MS HS SOSC
OS20	TOSC	TOSC = 1/FOSC	31.25	—	DC	ns	
OS25	TCY	Instruction Cycle Time(2,4)	62.5	—	DC	ns	
OS30	TosL, TosH	External Clock in (OSC1)(5) High or Low Time	0.45 x TOSC	—	—	ns	EC
OS31	TosR, TosF	External Clock in (OSC1)(5) Rise or Fall Time	—	—	20	ns	EC
OS40	TckR	CLKO Rise Time(3,5)	—	6	10	ns	
OS41	TckF	CLKO Fall Time(3,5)	—	6	10	ns	
OS42	GM	External Oscillator Transconductance(4)	14	16	18	mA/V	VDD = 3.3V, TA = +25°C

Note 1: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.

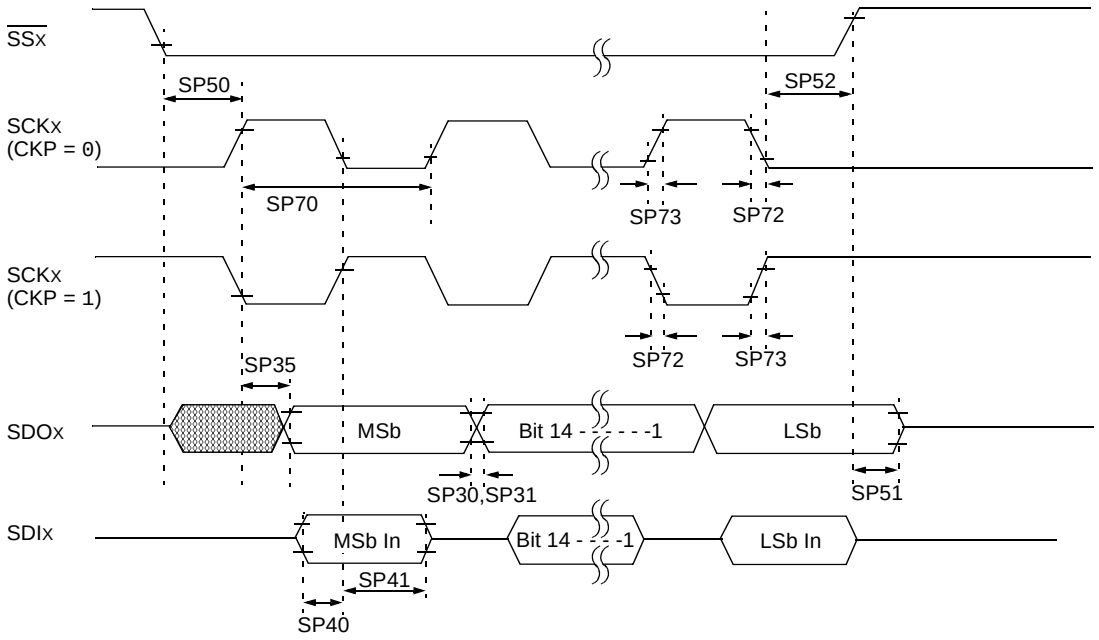
2: Instruction cycle period (TCY) equals two times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type, under standard operating conditions, with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKI pin. When an external clock input is used, the "max." cycle time limit is "DC" (no clock) for all devices.

3: Measurements are taken in EC mode. The CLKO signal is measured on the OSC2 pin.

4: These parameters are characterized by similarity, but are tested in manufacturing at FIN = 32 MHz only.

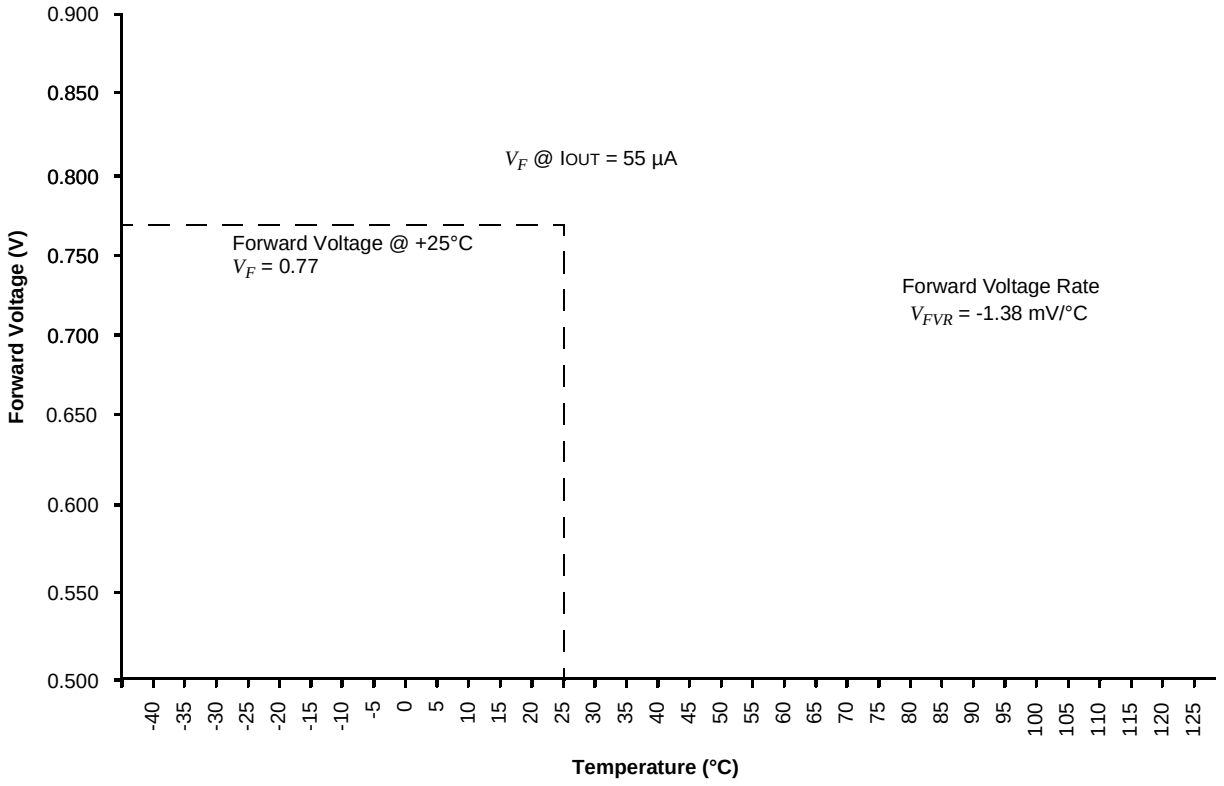
5: These parameters are characterized by similarity, but are not tested in manufacturing.

FIGURE 26-18: SPIx SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0) TIMING CHARACTERISTICS FOR dsPIC33FJ16(GP/MC)10X



Note: Refer to Figure 26-1 for load conditions.

FIGURE 26-33: FORWARD VOLTAGE VERSUS TEMPERATURE



Note: This graph is a statistical summary based on a limited number of samples and this data is characterized but not tested in manufacturing.

APPENDIX A: REVISION HISTORY

Revision A (January 2011)

This is the initial released version of the document.

Revision B (February 2011)

All major changes are referenced by their respective section in Table A-1.

In addition, minor text and formatting changes were incorporated throughout the document.

TABLE A-1: MAJOR SECTION UPDATES

Section Name	Update Description
High-Performance, Ultra Low Cost 16-bit Digital Signal Controllers	Pin diagram updates (see **"Pin Diagrams"**): • 20-pin PDIP/SOIC/SSOP (dsPIC33FJ16MC101): Removed the $\overline{\text{FLTB1}}$ pin from pin 10 • 28-pin SPDIP/SOIC/SSOP (dsPIC33FJ16MC102): Relocated the $\overline{\text{FLTB1}}$ pin from pin 12 to pin 14; relocated the $\overline{\text{FLTA1}}$ pin from pin 16 to pin 15 • 28-pin QFN (dsPIC33FJ16MC102): Relocated the $\overline{\text{FLTA1}}$ pin from pin 13 to pin 12; relocated the $\overline{\text{FLTB1}}$ pin from pin 9 to pin 11 • 36-pin TLA (dsPIC33FJ16MC102): Relocated the $\overline{\text{FLTA1}}$ pin from pin 17 to pin 16; relocated the $\overline{\text{FLTB1}}$ pin from pin 10 to pin 15
Section 1.0 "Device Overview"	Added Notes 1, 2, and 3 regarding the $\overline{\text{FLTA1}}$ and $\overline{\text{FLTB1}}$ pins to the Pinout I/O Descriptions (see Table 1-1). Added **Section ""**.
Section 4.0 "Memory Organization"	Updated All Resets value for PxFLTACON and PxFLTABCON to the 6-Output PWM1 Register Map (see Table 4-9). Added Note 1 to the PMD Register Map (see Table 4-29).
Section 6.0 "Resets"	Removed Reset timing sequence information from **Section 6.2 "System Reset"**, as this information is provided in Figure 6-2.
Section 15.0 "Motor Control PWM Module"	Added Note 2 and Note 3 regarding the $\overline{\text{FLTA1}}$ and $\overline{\text{FLTB1}}$ pins to the 6-channel PWM Module Block Diagram (see Figure 15-1). Added **Section 15.2 "PWM Faults"** and **Section 15.3 "Write-protected Registers"**. Added Note 2 and Note 3 regarding the $\overline{\text{FLTA1}}$ and $\overline{\text{FLTB1}}$ pins to the note boxes located below the PxFLTACON and PxFLTBCON registers (see Register 15-9 and Register 15-10).
Section 17.0 "Inter-Integrated Circuit™ (I^2C™)"	Updated the descriptions for the conditional If STREN = 1 and If STREN = 0 statements for the SCLREL bit in the I2Cx Control Register (see Register 17-1).
Section 23.0 "Special Features"	Added the RTSP Effect column to the dsPIC33F Configuration Bits Description (see Table 23-3).
Section 26.0 "Electrical Characteristics"	Added Parameters 300 and D305 (see Table 26-42 and Table 26-43).
Section 27.0 "Packaging Information"	Modified the pending TLA packaging page.

TABLE A-2: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description
Section 23.0 "Special Features"	Updated bits 5 and 4 of FPOR, modified Note 2, and removed Note 3 from the Configuration Shadow Register Map (see Table 23-1). Updated bit 14 of CONFIG1 and removed Note 5 from the Configuration Flash Words (see Table 23-2). Updated the PLLKEN Configuration bit description (see Table 23-3). Added Note 3 to Connections for the On-Chip Voltage Regulator (see Figure 23-1).
Section 26.0 "Electrical Characteristics"	Updated the Standard Operating Conditions to: 3.0V to 3.6V in all tables. Removed the Voltage on V_{CAP} with respect to V_{SS} entry in Absolute Maximum Ratings(1). Updated the V_{DD} Range (in Volts) in Operating MIPS vs. Voltage (see Table 26-1). Removed Parameter DC18 and updated the minimum value for Parameter DC 10 in the DC Temperature and Voltage Specifications (see Table 26-4). Updated the Characteristic definition and the Typical value for Parameter BO10 in Electrical Characteristics: BOR (see Table 26-5). Updated Note 2 in the DC Characteristics: Operating Current (I_{DD}) (see Table 26-6). Updated Note 2 in the DC Characteristics: Idle Current (I_{IDLE}) (see Table 26-7). Updated Note 2 and Parameters DC60C and DC61a-DC61d in the DC Characteristics: Power-Down Current (I_{PD}) (see Table 26-8). Updated Note 2 in the DC Characteristics: Doze Current (I_{DOZE}) (see Table 26-9). Added Note 1 to the Internal Voltage Regulator Specifications (see Table 26-13). Updated the Minimum and Maximum values for Parameter F20a and the Typical value for Parameter F20b in AC Characteristics: Internal Fast RC (FRC) Accuracy (see Table 26-18). Updated the Minimum, Typical, and Maximum values for Parameter F21a and F21b in Internal Low-Power RC (LPRC) Accuracy (see Table 26-19). Updated the Minimum, Typical, and Maximum values for Parameter D305 in the Comparator Module Specifications (see Table 26-43). Added Parameters CTMUFV1 and CTMUFV2 and updated Note 1 and the Conditions for all parameters in the CTMU Current Source Specifications (see Table 26-46). Added Forward Voltage Versus Temperature (see Figure 26-25).