Microchip Technology - DSPIC33FJ32MC101-E/SS Datasheet

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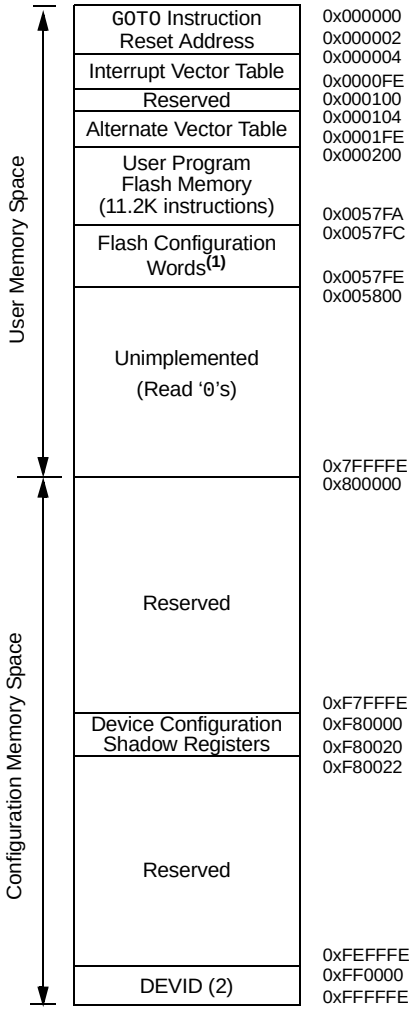
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	dsPIC
Core Size	16-Bit
Speed	16 MIPs
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, Motor Control PWM, POR, PWM, WDT
Number of I/O	15
Program Memory Size	32KB (11K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj32mc101-e-ss

FIGURE 4-2: PROGRAM MEMORY MAP FOR dsPIC33FJ32(GP/MC)101/102/104 DEVICES



Note 1: On Reset, these bits are automatically copied into the device Configuration Shadow registers.

TABLE 4-12: I2C1 REGISTER MAP

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
I2C1RCV	0200	—	—	—	—	—	—	—	—	I2C1 Receive Register								0000
I2C1TRN	0202	—	—	—	—	—	—	—	—	I2C1 Transmit Register								00FF
I2C1BRG	0204	—	—	—	—	—	—	—	Baud Rate Generator Register									0000
I2C1CON	0206	I2CEN	—	I2CSIDL	SCLREL	IPMIEN	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000
I2C1STAT	0208	ACKSTAT	TRSTAT	—	—	—	BCL	GCSTAT	ADD10	IWCOL	I2COV	D_A	P	S	R_W	RBF	TBF	0000
I2C1ADD	020A	—	—	—	—	—	—	I2C1 Address Register										0000
I2C1MSK	020C	—	—	—	—	—	—	I2C1 Address Mask Register										0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-13: UART1 REGISTER MAP

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
U1MODE	0220	UARTEN	—	USIDL	IREN	RTSMD	—	UEN1	UEN0	WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSEL1	PDSEL0	STSEL	0000
U1STA	0222	UTXISEL1	UTXINV	UTXISEL0	—	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL1	URXISEL0	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
U1TXREG	0224	—	—	—	—	—	—	—	UART1 Transmit Register									xxxx
U1RXREG	0226	—	—	—	—	—	—	—	UART1 Receive Register									0000
U1BRG	0228	Baud Rate Generator Prescaler																0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-14: SPI1 REGISTER MAP

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
SPI1STAT	0240	SPIEN	—	SPISIDL	—	—	—	—	—	—	SPIROV	—	—	—	—	SPITBF	SPIRBF	0000
SPI1CON1	0242	—	—	—	DISSCK	DISSDO	MODE16	SMP	CKE	SSEN	CKP	MSTEN	SPRE2	SPRE1	SPRE0	PPRE1	PPRE0	0000
SPI1CON2	0244	FRMEN	SPIFSD	FRMPOL	—	—	—	—	—	—	—	—	—	—	—	FRMDLY	—	0000
SPI1BUF	0248	SPI1 Transmit and Receive Buffer Register																0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

5.2 RTSP Operation

The dsPIC33FJ16(GP/MC)101/102 and dsPIC33FJ32(GP/MC)101/102/104 Flash program memory array is organized into rows of 64 instructions or 192 bytes. RTSP allows the user application to erase a page of memory, which consists of eight rows (512 instructions); and to program one word. Table 26-12 shows typical erase and programming times. The 8-row erase pages are edge-aligned from the beginning of program memory, on boundaries of 1536 bytes.

5.3 Programming Operations

A complete programming sequence is necessary for programming or erasing the internal Flash in RTSP mode. The processor stalls (waits) until the operation is finished.

The programming time depends on the FRC accuracy (see Table 26-18) and the value of the FRC Oscillator Tuning register (see Register 8-3). Use the following formula to calculate the minimum and maximum values for the Word write time and page erase time (see Parameters D138a and D138b, and Parameters D137a and D137b in Table 26-12, respectively).

EQUATION 5-1: PROGRAMMING TIME

$$\frac{T}{7.37\ MHz \times (FRC\ Accuracy)\% \times (FRC\ Tuning)\%}$$

For example, if the device is operating at +125°C, the FRC accuracy will be ±2%. If the TUN<5:0> bits (see Register 8-3) are set to `'b000000`, the minimum row write time is equal to Equation 5-2.

EQUATION 5-2: MINIMUM ROW WRITE TIME

$$T_{RW} = \frac{355\ Cycles}{7.37\ MHz \times (1 + 0.02) \times (1 - 0.00375)} = 47.4\mu s$$

The maximum row write time is equal to Equation 5-3.

EQUATION 5-3: MAXIMUM ROW WRITE TIME

$$T_{RW} = \frac{355\ Cycles}{7.37\ MHz \times (1 - 0.02) \times (1 - 0.00375)} = 49.3\mu s$$

Setting the WR bit (NVMCON<15>) starts the operation and the WR bit is automatically cleared when the operation is finished.

5.3.1 PROGRAMMING ALGORITHM FOR FLASH PROGRAM MEMORY

Programmers can program one word (24 bits) of program Flash memory at a time. To do this, it is necessary to erase the 8-row erase page that contains the desired address of the location the user wants to change.

For protection against accidental operations, the write initiate sequence for NVMKEY must be used to allow any erase or program operation to proceed. After the programming command has been executed, the user application must wait for the programming time until programming is complete. The two instructions following the start of the programming sequence should be `NOP`s.

Note:	Performing a page erase operation on the last page of program memory will clear the Flash Configuration Words, thereby enabling code protection as a result. Therefore, users should avoid performing page erase operations on the last page of program memory.

Refer to **"Flash Programming"** (DS70191) in the *"dsPIC33/PIC24 Family Reference Manual"* for details and codes examples on programming using RTSP.

5.4 Control Registers

Two SFRs are used to read and write the program Flash memory: NVMCON and NVMKEY.

The NVMCON register (Register 5-1) controls which blocks are to be erased, which memory type is to be programmed and the start of the programming cycle.

NVMKEY is a write-only register that is used for write protection. To start a programming or erase sequence, the user application must consecutively write 0x55 and 0xAA to the NVMKEY register. Refer to **Section 5.3 "Programming Operations"** for further details.

REGISTER 7-16: IPC1: INTERRUPT PRIORITY CONTROL REGISTER 1

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	T2IP2	T2IP1	T2IP0	—	OC2IP2	OC2IP1	OC2IP0
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	IC2IP2	IC2IP1	IC2IP0	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-12 **T2IP<2:0>:** Timer2 Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as ‘0’

bit 10-8 **OC2IP<2:0>:** Output Compare Channel 2 Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **IC2IP<2:0>:** Input Capture Channel 2 Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3-0 **Unimplemented:** Read as ‘0’

REGISTER 7-19: IPC4: INTERRUPT PRIORITY CONTROL REGISTER 4

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	CNIP2	CNIP1	CNIP0	—	CMIP2	CMIP1	CMIP0
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	MI2C1IP2	MI2C1IP1	MI2C1IP0	—	SI2C1IP2	SI2C1IP1	SI2C1IP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-12 **CNIP<2:0>:** Change Notification Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as ‘0’

bit 10-8 **CMIP<2:0>:** Comparator Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **MI2C1IP<2:0>:** I2C1 Master Events Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as ‘0’

bit 2-0 **SI2C1IP<2:0>:** I2C1 Slave Events Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

REGISTER 8-3: OSCTUN: FRC OSCILLATOR TUNING REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	TUN<5:0>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-6 **Unimplemented:** Read as ‘0’

bit 5-0 **TUN<5:0>:** FRC Oscillator Tuning bits

011111 = Maximum frequency deviation of 1.453% (7.477 MHz)
011110 = Center frequency + 1.406% (7.474 MHz)
•
•
•
000001 = Center frequency + 0.047% (7.373 MHz)
000000 = Center frequency (7.37 MHz nominal)
111111 = Center frequency – 0.047% (7.367 MHz)
•
•
•
100001 = Center frequency – 1.453% (7.263 MHz)
100000 = Minimum frequency deviation of -1.5% (7.259 MHz)

10.4.3 CONTROLLING CONFIGURATION CHANGES

Because peripheral remapping can be changed during run time, some restrictions on peripheral remapping are needed to prevent accidental configuration changes. dsPIC33FJ16(GP/MC)101/102 and dsPIC33FJ32(GP/MC)101/102/104 devices include three features to prevent alterations to the peripheral map:

- Control register lock sequence
- Continuous state monitoring
- Configuration bit pin select lock

10.4.3.1 Control Register Lock

Under normal operation, writes to the RPINRx and RPORx registers are not allowed. Attempted writes appear to execute normally, but the contents of the registers remain unchanged. To change these registers, they must be unlocked in hardware. The register lock is controlled by the IOLOCK bit (OSCCON<6>). Setting IOLOCK prevents writes to the control registers; clearing IOLOCK allows writes.

To set or clear IOLOCK, a specific command sequence must be executed:

1. Write 0x46 to OSCCON<7:0>.
2. Write 0x57 to OSCCON<7:0>.
3. Clear (or set) IOLOCK as a single operation.

Note: MPLAB® C30 provides built-in C language functions for unlocking the OSCCON register:

```
__builtin_write_OSCCONL(value)
__builtin_write_OSCCONH(value)
```

See MPLAB IDE Help for more information.

Unlike the similar sequence with the oscillator's LOCK bit, IOLOCK remains in one state until changed. This allows all of the Peripheral Pin Selects to be configured with a single unlock sequence followed by an update to all control registers, then locked with a second lock sequence.

10.4.3.2 Continuous State Monitoring

In addition to being protected from direct writes, the contents of the RPINRx and RPORx registers are constantly monitored in hardware by shadow registers. If an unexpected change in any of the registers occurs (such as cell disturbances caused by ESD or other external events), a Configuration Mismatch Reset will be triggered.

10.4.3.3 Configuration Bit Pin Select Lock

As an additional level of safety, the device can be configured to prevent more than one write session to the RPINRx and RPORx registers. The IOL1WAY (FOSC<5>) Configuration bit blocks the IOLOCK bit from being cleared after it has been set once. If IOLOCK remains set, the register unlock procedure will not execute and the Peripheral Pin Select Control registers cannot be written to. The only way to clear the bit and re-enable peripheral remapping is to perform a device Reset.

In the default (unprogrammed) state, IOL1WAY is set, restricting users to one write session. Programming IOL1WAY allows user applications unlimited access (with the proper use of the unlock sequence) to the Peripheral Pin Select registers.

REGISTER 10-11: RPOR0: PERIPHERAL PIN SELECT OUTPUT REGISTER 0

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	RP1R<4:0>				
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	RP0R<4:0>				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-13 **Unimplemented:** Read as ‘0’

bit 12-8 **RP1R<4:0>:** Peripheral Output Function is Assigned to RP1 Output Pin bits
(see Table 10-2 for peripheral function numbers)

bit 7-5 **Unimplemented:** Read as ‘0’

bit 4-0 **RP0R<4:0>:** Peripheral Output Function is Assigned to RP0 Output Pin bits
(see Table 10-2 for peripheral function numbers)

REGISTER 10-12: RPOR1: PERIPHERAL PIN SELECT OUTPUT REGISTER 1

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	RP3R<4:0>(1)				
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	RP2R<4:0>(1)				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-13 **Unimplemented:** Read as ‘0’

bit 12-8 **RP3R<4:0>:** Peripheral Output Function is Assigned to RP3 Output Pin bits(1)
(see Table 10-2 for peripheral function numbers)

bit 7-5 **Unimplemented:** Read as ‘0’

bit 4-0 **RP2R<4:0>:** Peripheral Output Function is Assigned to RP2 Output Pin bits(1)
(see Table 10-2 for peripheral function numbers)

Note 1: These bits are not available in dsPIC33FJXX(GP/MC)101 devices.

11.0 TIMER1

Note 1: This data sheet summarizes the features of the dsPIC33FJ16(GP/MC)101/102 and dsPIC33FJ32(GP/MC)101/102/104 family devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Timers"** (DS70205) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The Timer1 module is a 16-bit timer, which can serve as the time counter for the Real-Time Clock (RTC) or operate as a free-running interval timer/counter. Timer1 can operate in three modes:

- 16-Bit Timer
- 16-Bit Synchronous Counter
- 16-Bit Asynchronous Counter

Timer1 also supports these features:

- Timer gate operation
- Selectable prescaler settings
- Timer operation during CPU Idle and Sleep modes
- Interrupt on 16-bit Period register match or falling edge of external gate signal

Figure 11-1 presents a block diagram of the 16-bit timer module.

To configure Timer1 for operation:

1. Load the timer value into the TMR1 register.
2. Load the timer period value into the PR1 register.
3. Select the timer prescaler ratio using the TCKPS<1:0> bits in the T1CON register.
4. Set the Clock and Gating modes using the TCS and TGATE bits in the T1CON register.
5. Set or clear the TSYNC bit in T1CON to select synchronous or asynchronous operation.
6. If interrupts are required, set the Timer1 Interrupt Enable bit, T1IE. Use the Timer1 Interrupt Priority bits, T1IP<2:0>, to set the interrupt priority.
7. Set the TON bit (= 1) in the T1CON register.

FIGURE 11-1: 16-BIT TIMER1 MODULE BLOCK DIAGRAM

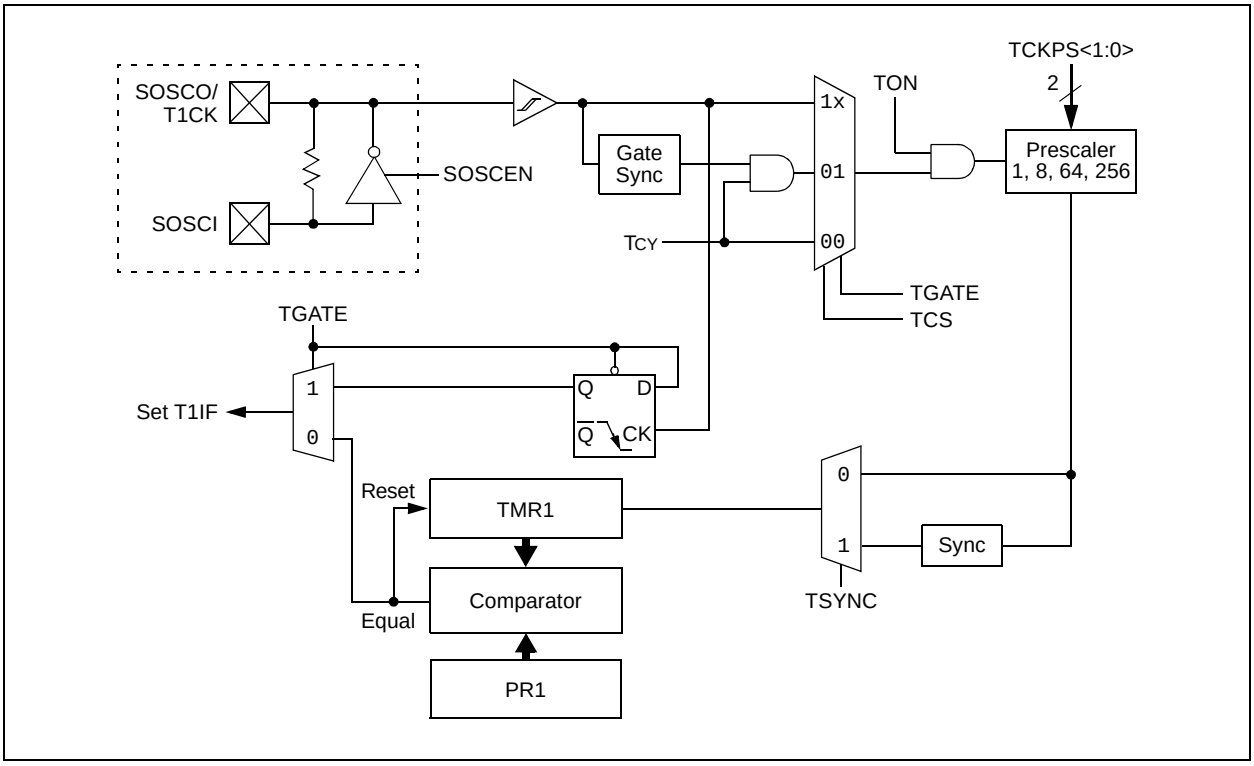
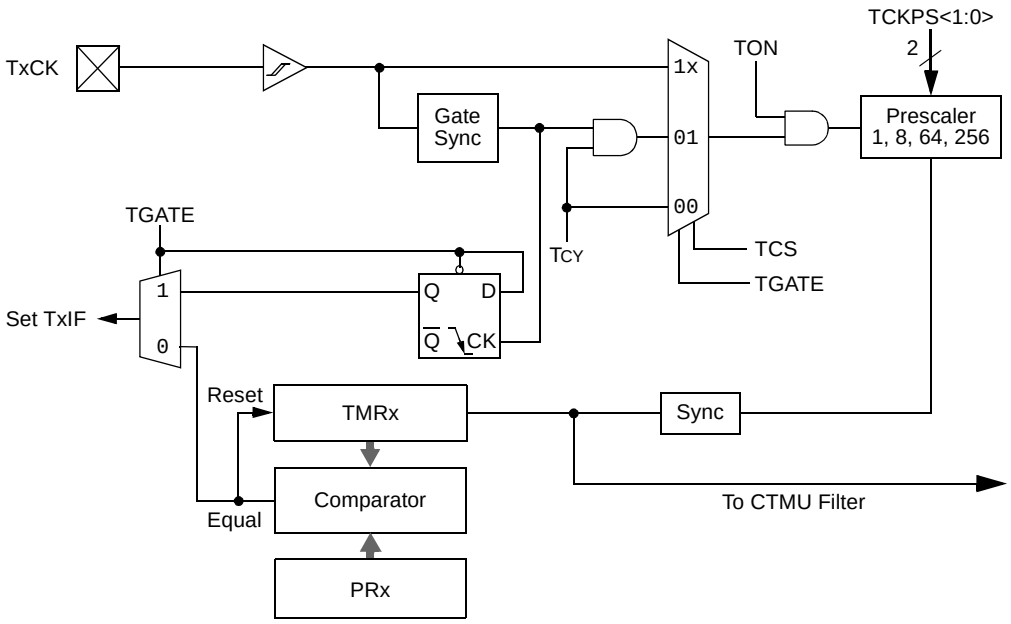
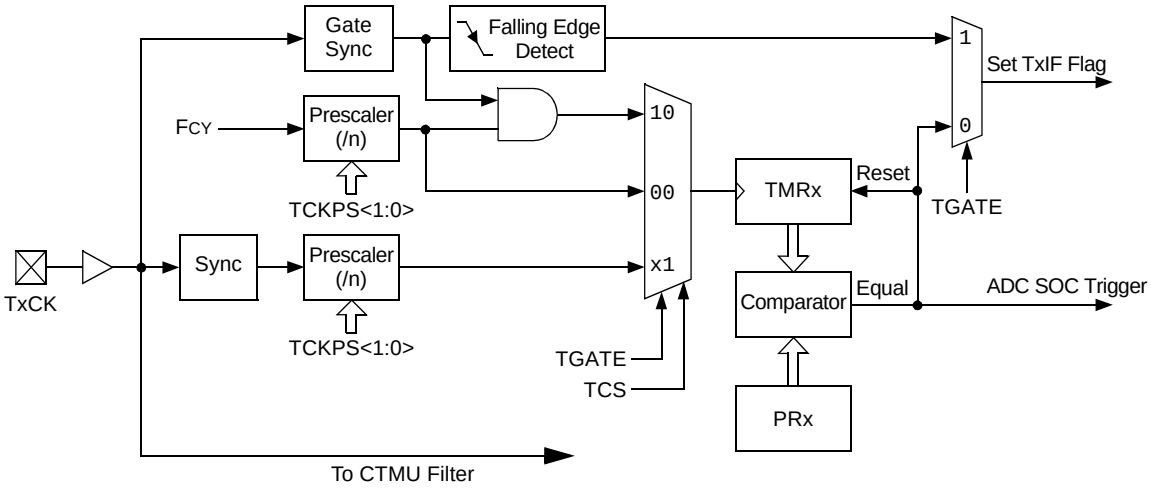


FIGURE 12-2: TIMER2 AND TIMER4 (16-BIT) BLOCK DIAGRAM(1)



Note 1: Timer4 is available in dsPIC33FJ32(GP/MC)10X devices only.

FIGURE 12-3: TIMER3 AND TIMER5 (16-BIT) BLOCK DIAGRAM(1)



Note 1: Timer5 is available in dsPIC33FJ32(GP/MC)10X devices only.

NOTES:

REGISTER 20-4: CMxMSKCON: COMPARATOR x MASK GATING CONTROL REGISTER (CONTINUED)

bit 3 **ABEN:** AND Gate A1 B Input Inverted Enable bit
1 = MBI is connected to AND gate
0 = MBI is not connected to AND gate

bit 2 **ABNEN:** AND Gate A1 B Input Inverted Enable bit
1 = Inverted MBI is connected to AND gate
0 = Inverted MBI is not connected to AND gate

bit 1 **AAEN:** AND Gate A1 A Input Enable bit
1 = MAI is connected to AND gate
0 = MAI is not connected to AND gate

bit 0 **AANEN:** AND Gate A1 A Input Inverted Enable bit
1 = Inverted MAI is connected to AND gate
0 = Inverted MAI is not connected to AND gate

23.2 On-Chip Voltage Regulator

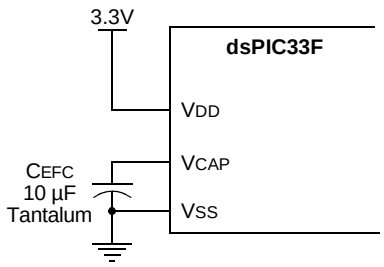
All of the dsPIC33FJ16(GP/MC)101/102 and dsPIC33FJ32(GP/MC)101/102/104 devices power their core digital logic at a nominal 2.5V. This can create a conflict for designs that are required to operate at a higher typical voltage, such as 3.3V. To simplify system design, all devices in the dsPIC33FJ16(GP/MC)101/102 and dsPIC33FJ32(GP/MC)101/102/104 family incorporate an on-chip regulator that allows the device to run its core logic from VDD.

The regulator provides power to the core from the other VDD pins. When the regulator is enabled, a low-ESR (less than 5 ohms) capacitor (such as tantalum or ceramic) must be connected to the VCAP pin (Figure 23-1). This helps to maintain the stability of the regulator. The recommended value for the filter capacitor is provided in Table 26-14 located in **Section 26.1 "DC Characteristics"**.

Note:	It is important for low-ESR capacitors to be placed as close as possible to the VCAP pin.

On a POR, it takes approximately 20 μs for the on-chip voltage regulator to generate an output voltage. During this time, designated as TSTARTUP, code execution is disabled. TSTARTUP is applied every time the device resumes operation after any power-down.

FIGURE 23-1: CONNECTIONS FOR THE ON-CHIP VOLTAGE REGULATOR(1,2,3)



Note 1: These are typical operating voltages. Refer to Table 26-14 located in **Section 26.1 "DC Characteristics"** for the full operating ranges of VDD and VCAP.

2: It is important for low-ESR capacitors to be placed as close as possible to the VCAP pin.

3: Typical VCAP pin voltage = 2.5V when VDD ≥ VDDMIN.

23.3 BOR: Brown-out Reset

The Brown-out Reset (BOR) module is based on an internal voltage reference circuit that monitors the regulated supply voltage, VCAP. The main purpose of the BOR module is to generate a device Reset when a brown-out condition occurs. Brown-out conditions are generally caused by glitches on the AC mains (for example, missing portions of the AC cycle waveform due to bad power transmission lines or voltage sags due to excessive current draw when a large inductive load is turned on).

A BOR generates a Reset pulse, which resets the device. The BOR selects the clock source, based on the device Configuration bit values (FNOSC<2:0> and POSCMD<1:0>).

If an Oscillator mode is selected, the BOR activates the Oscillator Start-up Timer (OST). The system clock is held until OST expires. If the PLL is used, the clock is held until the LOCK bit (OSCCON<5>) is '1'.

Concurrently, the PWRT Time-out (TPWRT) is applied before the internal Reset is released. If TPWRT = 0 and a crystal oscillator is being used, then a nominal delay of TFSCM = 100 is applied. The total delay in this case is TFSCM.

The BOR status bit (RCON<1>) is set to indicate that a BOR has occurred. The BOR circuit continues to operate while in Sleep or Idle modes and resets the device should VDD fall below the BOR threshold voltage.

TABLE 24-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax		Description	# of Words	# of Cycles	Status Flags Affected
9	BTG	BTG	f,#bit4	Bit Toggle f	1	1	None
		BTG	Ws,#bit4	Bit Toggle Ws	1	1	None
10	BTSC	BTSC	f,#bit4	Bit Test f, Skip if Clear	1	1 (2 or 3)	None
		BTSC	Ws,#bit4	Bit Test Ws, Skip if Clear	1	1 (2 or 3)	None
11	BTSS	BTSS	f,#bit4	Bit Test f, Skip if Set	1	1 (2 or 3)	None
		BTSS	Ws,#bit4	Bit Test Ws, Skip if Set	1	1 (2 or 3)	None
12	BTST	BTST	f,#bit4	Bit Test f	1	1	Z
		BTST.C	Ws,#bit4	Bit Test Ws to C	1	1	C
		BTST.Z	Ws,#bit4	Bit Test Ws to Z	1	1	Z
		BTST.C	Ws,Wb	Bit Test Ws<Wb> to C	1	1	C
		BTST.Z	Ws,Wb	Bit Test Ws<Wb> to Z	1	1	Z
13	BTSTS	BTSTS	f,#bit4	Bit Test then Set f	1	1	Z
		BTSTS.C	Ws,#bit4	Bit Test Ws to C, then Set	1	1	C
		BTSTS.Z	Ws,#bit4	Bit Test Ws to Z, then Set	1	1	Z
14	CALL	CALL	lit23	Call subroutine	2	2	None
		CALL	Wn	Call indirect subroutine	1	2	None
15	CLR	CLR	f	f = 0x0000	1	1	None
		CLR	WREG	WREG = 0x0000	1	1	None
		CLR	Ws	Ws = 0x0000	1	1	None
		CLR	Acc,Wx,Wxd,Wy,Wyd,AWB	Clear Accumulator	1	1	OA,OB,SA,SB
16	CLRWDT	CLRWDT		Clear Watchdog Timer	1	1	WDTO,Sleep
17	COM	COM	f	$f = \overline{f}$	1	1	N,Z
		COM	f,WREG	$WREG = \overline{f}$	1	1	N,Z
		COM	Ws,Wd	$Wd = \overline{Ws}$	1	1	N,Z
18	CP	CP	f	Compare f with WREG	1	1	C,DC,N,OV,Z
		CP	Wb,#lit5	Compare Wb with lit5	1	1	C,DC,N,OV,Z
		CP	Wb,Ws	Compare Wb with Ws (Wb – Ws)	1	1	C,DC,N,OV,Z
19	CP0	CP0	f	Compare f with 0x0000	1	1	C,DC,N,OV,Z
		CP0	Ws	Compare Ws with 0x0000	1	1	C,DC,N,OV,Z
20	CPB	CPB	f	Compare f with WREG, with Borrow	1	1	C,DC,N,OV,Z
		CPB	Wb,#lit5	Compare Wb with lit5, with Borrow	1	1	C,DC,N,OV,Z
		CPB	Wb,Ws	Compare Wb with Ws, with Borrow ($Wb – Ws – \overline{C}$)	1	1	C,DC,N,OV,Z
21	CPSEQ	CPSEQ	Wb, Wn	Compare Wb with Wn, skip if =	1	1 (2 or 3)	None
22	CPSGT	CPSGT	Wb, Wn	Compare Wb with Wn, skip if >	1	1 (2 or 3)	None
23	CPSLT	CPSLT	Wb, Wn	Compare Wb with Wn, skip if <	1	1 (2 or 3)	None
24	CPSNE	CPSNE	Wb, Wn	Compare Wb with Wn, skip if ≠	1	1 (2 or 3)	None
25	DAW	DAW	Wn	Wn = decimal adjust Wn	1	1	C
26	DEC	DEC	f	f = f – 1	1	1	C,DC,N,OV,Z
		DEC	f,WREG	WREG = f – 1	1	1	C,DC,N,OV,Z
		DEC	Ws,Wd	Wd = Ws – 1	1	1	C,DC,N,OV,Z
27	DEC2	DEC2	f	f = f – 2	1	1	C,DC,N,OV,Z
		DEC2	f,WREG	WREG = f – 2	1	1	C,DC,N,OV,Z
		DEC2	Ws,Wd	Wd = Ws – 2	1	1	C,DC,N,OV,Z
28	DISI	DISI	#lit14	Disable Interrupts for k instruction cycles	1	1	None

26.1 DC Characteristics

TABLE 26-1: OPERATING MIPS vs. VOLTAGE

Characteristic	VDD Range (in Volts)	Temp Range (in °C)	Max MIPS
			dsPIC33FJ16(GP/MC)101/102 and dsPIC33FJ32(GP/MC)101/102/104
DC5	VBOR-3.6V(1)	-40°C to +85°C	16
	VBOR-3.6V(1)	-40°C to +125°C	16

Note 1: Overall functional device operation at VBOR < VDD < VDDMIN is ensured but not characterized. All device analog modules, such as the ADC, etc., will function but with degraded performance below VDDMIN.

TABLE 26-2: THERMAL OPERATING CONDITIONS

Rating	Symbol	Min	Typ	Max	Unit
Industrial Temperature Devices					
Operating Junction Temperature Range	TJ	-40	—	+125	°C
Operating Ambient Temperature Range	TA	-40	—	+85	°C
Extended Temperature Devices					
Operating Junction Temperature Range	TJ	-40	—	+140	°C
Operating Ambient Temperature Range	TA	-40	—	+125	°C
Power Dissipation: Internal Chip Power Dissipation: PINT = VDD x (IDD – Σ IOH) I/O Pin Power Dissipation: I/O = Σ ({VDD – VOH} x IOH) + Σ (VOL x IOL)	PD	PINT + PIO			W
Maximum Allowed Power Dissipation	PDMAX	(TJ – TA)/θJA			W

TABLE 26-3: THERMAL PACKAGING CHARACTERISTICS

Characteristic	Symbol	Typ	Max	Unit	Notes
Package Thermal Resistance, 18-pin PDIP	θJA	50	—	°C/W	**1**
Package Thermal Resistance, 20-pin PDIP	θJA	50	—	°C/W	**1**
Package Thermal Resistance, 28-pin SPDIP	θJA	50	—	°C/W	**1**
Package Thermal Resistance, 18-pin SOIC	θJA	63	—	°C/W	**1**
Package Thermal Resistance, 20-pin SOIC	θJA	63	—	°C/W	**1**
Package Thermal Resistance, 28-pin SOIC	θJA	55	—	°C/W	**1**
Package Thermal Resistance, 20-pin SSOP	θJA	90	—	°C/W	**1**
Package Thermal Resistance, 28-pin SSOP	θJA	71	—	°C/W	**1**
Package Thermal Resistance, 28-pin QFN (6x6 mm)	θJA	37	—	°C/W	**1**
Package Thermal Resistance, 36-pin VTLA (5x5 mm)	θJA	31.1	—	°C/W	**1**
Package Thermal Resistance, 44-pin TQFP	θJA	45	—	°C/W	**1, 2**
Package Thermal Resistance, 44-pin QFN	θJA	32	—	°C/W	**1, 2**
Package Thermal Resistance, 44-pin VTLA	θJA	30	—	°C/W	**1, 2**

Note 1: Junction to ambient thermal resistance; Theta-JA (θJA) numbers are achieved by package simulations.

2: This package is available in dsPIC33FJ32(GP/MC)104 devices only.

TABLE 26-44: SPIx SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0) TIMING REQUIREMENTS FOR dsPIC33FJ32(GP/MC)10X

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic(1)**	**Min**	**Typ(2)**	**Max**	**Units**	**Conditions**
SP70	TscP	Maximum SCKx Input Frequency	—	—	11	MHz	See **Note 3**
SP72	TscF	SCKx Input Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP73	TscR	SCKx Input Rise Time	—	—	—	ns	See Parameter DO31 and **Note 4**
SP30	TdoF	SDOx Data Output Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP31	TdoR	SDOx Data Output Rise Time	—	—	—	ns	See Parameter DO31 and **Note 4**
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SSx}$ ↓ to SCKx ↑ or SCKx Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{SSx}$ ↑ to SDOx Output High-Impedance	10	—	50	ns	See **Note 4**
SP52	TscH2ssH TscL2ssH	$\overline{SSx}$ after SCKx Edge	1.5 TCY + 40	—	—	ns	See **Note 4**

Note 1: These parameters are characterized, but are not tested in manufacturing.

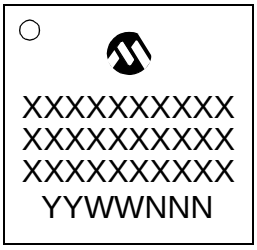
2: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCKx is 91 ns. Therefore, the SCKx clock generated by the Master must not violate this specification.

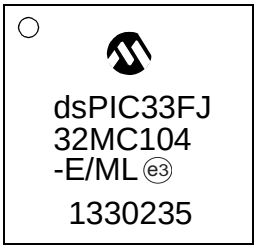
4: Assumes 50 pF load on all SPIx pins.

28.1 Package Marking Information (Continued)

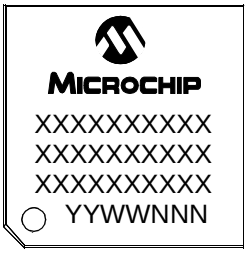
44-Lead QFN



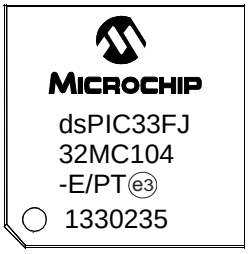
Example



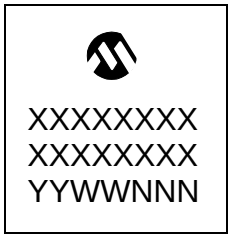
44-Lead TQFP



Example



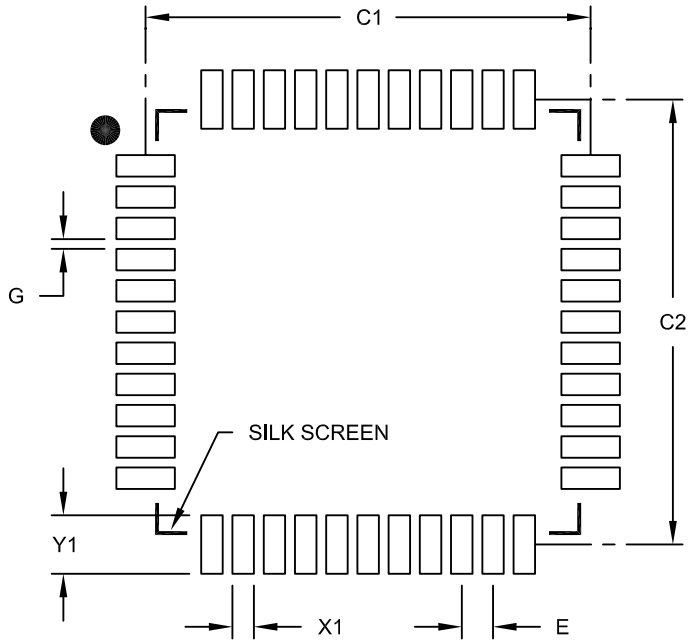
44-Lead VTLA



Example

44-Lead Plastic Thin Quad Flatpack (PT) 10X10X1 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.80 BSC	
Contact Pad Spacing	C1		11.40	
Contact Pad Spacing	C2		11.40	
Contact Pad Width (X44)	X1			0.55
Contact Pad Length (X44)	Y1			1.50
Distance Between Pads	G	0.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2076B

APPENDIX A: REVISION HISTORY

Revision A (January 2011)

This is the initial released version of the document.

Revision B (February 2011)

All major changes are referenced by their respective section in Table A-1.

In addition, minor text and formatting changes were incorporated throughout the document.

TABLE A-1: MAJOR SECTION UPDATES

Section Name	Update Description
High-Performance, Ultra Low Cost 16-bit Digital Signal Controllers	Pin diagram updates (see **"Pin Diagrams"**): • 20-pin PDIP/SOIC/SSOP (dsPIC33FJ16MC101): Removed the $\overline{\text{FLTB1}}$ pin from pin 10 • 28-pin SPDIP/SOIC/SSOP (dsPIC33FJ16MC102): Relocated the $\overline{\text{FLTB1}}$ pin from pin 12 to pin 14; relocated the $\overline{\text{FLTA1}}$ pin from pin 16 to pin 15 • 28-pin QFN (dsPIC33FJ16MC102): Relocated the $\overline{\text{FLTA1}}$ pin from pin 13 to pin 12; relocated the $\overline{\text{FLTB1}}$ pin from pin 9 to pin 11 • 36-pin TLA (dsPIC33FJ16MC102): Relocated the $\overline{\text{FLTA1}}$ pin from pin 17 to pin 16; relocated the $\overline{\text{FLTB1}}$ pin from pin 10 to pin 15
Section 1.0 "Device Overview"	Added Notes 1, 2, and 3 regarding the $\overline{\text{FLTA1}}$ and $\overline{\text{FLTB1}}$ pins to the Pinout I/O Descriptions (see Table 1-1). Added **Section ""**.
Section 4.0 "Memory Organization"	Updated All Resets value for PxFLTACON and PxFLTABCON to the 6-Output PWM1 Register Map (see Table 4-9). Added Note 1 to the PMD Register Map (see Table 4-29).
Section 6.0 "Resets"	Removed Reset timing sequence information from **Section 6.2 "System Reset"**, as this information is provided in Figure 6-2.
Section 15.0 "Motor Control PWM Module"	Added Note 2 and Note 3 regarding the $\overline{\text{FLTA1}}$ and $\overline{\text{FLTB1}}$ pins to the 6-channel PWM Module Block Diagram (see Figure 15-1). Added **Section 15.2 "PWM Faults"** and **Section 15.3 "Write-protected Registers"**. Added Note 2 and Note 3 regarding the $\overline{\text{FLTA1}}$ and $\overline{\text{FLTB1}}$ pins to the note boxes located below the PxFLTACON and PxFLTBCON registers (see Register 15-9 and Register 15-10).
Section 17.0 "Inter-Integrated Circuit™ (I^2C™)"	Updated the descriptions for the conditional If STREN = 1 and If STREN = 0 statements for the SCLREL bit in the I2Cx Control Register (see Register 17-1).
Section 23.0 "Special Features"	Added the RTSP Effect column to the dsPIC33F Configuration Bits Description (see Table 23-3).
Section 26.0 "Electrical Characteristics"	Added Parameters 300 and D305 (see Table 26-42 and Table 26-43).
Section 27.0 "Packaging Information"	Modified the pending TLA packaging page.

Revision D (April 2012)

This revision includes updates in support of the following new devices:

- dsPIC33FJ32GP101
- dsPIC33FJ32GP102
- dsPIC33FJ32GP104
- dsPIC33FJ32MC101
- dsPIC33FJ32MC102
- dsPIC33FJ32MC104

Also, where applicable, new sections were added to peripheral chapters that provide information and links to the related resources, as well as helpful tips. For examples, see **Section 18.1 "UART Helpful Tips"** and **Section 18.2 "UART Resources"**.

This revision includes text and formatting changes that were incorporated throughout the document.

All other major changes are referenced by their respective section in Table A-3.

TABLE A-3: MAJOR SECTION UPDATES

Section Name	Update Description
"16-Bit Digital Signal Controllers (up to 32-Kbyte Flash and 2-Kbyte SRAM)"	The content on the first page of this section was extensively reworked to provide the reader with the key features and functionality of this device family in an "at-a-glance" format. **TABLE 2: "dsPIC33FJ32(GP/MC)101/102/104 Device Features"** was added, which provides a feature overview of the new devices. All pin diagrams were updated (see **"Pin Diagrams"**).
Section 1.0 "Device Overview"	Updated the notes in the device family block diagram (see Figure 1-1). Updated the following pinout I/O descriptions (Table 1-1): • ANx • CNx • RAx • RCx • CVREFIN (formerly CVREF) Relocated **1.1 "Referenced Sources"** to the previous chapter (see **"Referenced Sources"**).
Section 2.0 "Guidelines for Getting Started with 16-bit Digital Signal Controllers"	Updated the Recommended Minimum Connection diagram (see Figure 2-1).
Section 4.0 "Memory Organization"	Updated the existing Program Memory Map (see Figure 4-1) and added the Program Memory Map for dsPIC33FJ16(GP/MC)101/102 Devices (see Figure 4-1). Updated the existing Data Memory Map (see Figure 4-4) and added the Data Memory Map for dsPIC33FJ32(GP/MC)101/102/104 Devices with 2-Kbyte RAM (see Figure 4-5). The following Special Function Register maps were updated or added: • TABLE 4-5: Change Notification Register Map for dsPIC33FJ32(GP/MC)104 Devices • TABLE 4-6: Interrupt Controller Register Map • TABLE 4-8: Timers Register Map for dsPIC33FJ32(GP/MC)10X Devices • TABLE 4-15: ADC1 Register Map for dsPIC33FJXX(GP/MC)101 Devices • TABLE 4-17: ADC1 Register Map for dsPIC33FJ32(GP/MC)104 Devices • TABLE 4-22: Peripheral Pin Select Input Register Map • TABLE 4-26: Peripheral Pin Select Output Register Map for dsPIC33FJ32(GP/MC)104 Devices • TABLE 4-28: PORTA Register Map for dsPIC33FJ32(GP/MC)101/102 Devices • TABLE 4-29: PORTA Register Map for dsPIC33FJ32(GP/MC)104 Devices • TABLE 4-36: PORTC Register Map for dsPIC33FJ32(GP/MC)104 Devices • TABLE 4-39: PMD Register Map