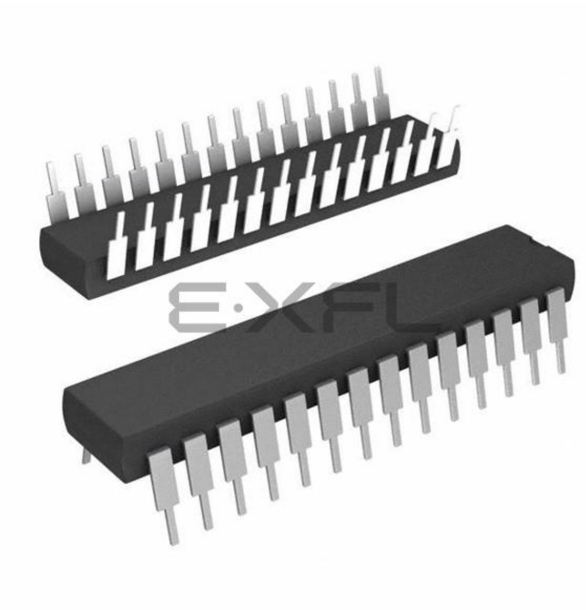

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	16 MIPs
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, Motor Control PWM, POR, PWM, WDT
Number of I/O	21
Program Memory Size	32KB (11K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj32mc102-i-sp

TABLE 2: dsPIC33FJ32(GP/MC)101/102/104 DEVICE FEATURES

Device	Pins	Program Flash (Kbyte)	RAM (Kbytes)	Remappable Peripherals							Motor Control PWM	PWM Faults	10-Bit, 1.1 Msps ADC	RTCC	I^2C™	Comparators	CTMU	I/O Pins	Packages
				Remappable Pins	16-bit Timer(1,2)	Input Capture	Output Compare	UART	External Interrupts(3)	SPI									
dsPIC33FJ32GP101	18	32	2	8	5	3	2	1	3	1	—	—	1 ADC, 6-ch	Y	1	3	Y	13	PDIP, SOIC
	20	32	2	8	5	3	2	1	3	1	—	—	1 ADC, 6-ch	Y	1	3	Y	15	SSOP
dsPIC33FJ32GP102	28	32	2	16	5	3	2	1	3	1	—	—	1 ADC, 8-ch	Y	1	3	Y	21	SPDIP, SOIC, SSOP, QFN
	36	32	2	16	5	3	2	1	3	1	—	—	1 ADC, 8-ch	Y	1	3	Y	21	VTLA
dsPIC33FJ32GP104	44	32	2	26	5	3	2	1	3	1	—	—	1 ADC, 14-ch	Y	1	3	Y	35	TQFP, QFN, VTLA
dsPIC33FJ32MC101	20	32	2	10	5	3	2	1	3	1	6-ch	1	1 ADC, 6-ch	Y	1	3	Y	15	PDIP, SOIC, SSOP
dsPIC33FJ32MC102	28	32	2	16	5	3	2	1	3	1	6-ch	2	1 ADC, 8-ch	Y	1	3	Y	21	SPDIP, SOIC, SSOP, QFN
	36	32	2	16	5	3	2	1	3	1	6-ch	2	1 ADC, 8-ch	Y	1	3	Y	21	VTLA
dsPIC33FJ32MC104	44	32	2	26	5	3	2	1	3	1	6-ch	2	1 ADC, 14-ch	Y	1	3	Y	35	TQFP, QFN, VTLA

Note 1: Four out of five timers are remappable.
2: Two pairs can be combined to have up to two 32-bit timers.
3: Two out of three interrupts are remappable.

3.6.1 MULTIPLIER

The 17-bit x 17-bit multiplier is capable of signed or unsigned operation and can multiplex its output using a scaler to support either 1.31 fractional (Q31) or 32-bit integer results. Unsigned operands are zero-extended into the 17th bit of the multiplier input value. Signed operands are sign-extended into the 17th bit of the multiplier input value. The output of the 17-bit x 17-bit multiplier/scaler is a 33-bit value that is sign-extended to 40 bits. Integer data is inherently represented as a signed 2's complement value, where the Most Significant bit (MSb) is defined as a sign bit. The range of an N-bit 2's complement integer is -2^{N-1} to $2^{N-1} – 1$.

- For a 16-bit integer, the data range is -32768 (0x8000) to 32767 (0x7FFF) including 0.
- For a 32-bit integer, the data range is -2,147,483,648 (0x8000 0000) to 2,147,483,647 (0x7FFF FFFF).

When the multiplier is configured for fractional multiplication, the data is represented as a 2's complement fraction, where the MSb is defined as a sign bit and the radix point is implied to lie just after the sign bit (QX format). The range of an N-bit 2's complement fraction with this implied radix point is -1.0 to $(1 – 2^{1-N})$. For a 16-bit fraction, the Q15 data range is -1.0 (0x8000) to 0.999969482 (0x7FFF) including 0 and has a precision of 3.01518×10^{-5}. In Fractional mode, the 16 x 16 multiply operation generates a 1.31 product that has a precision of 4.65661×10^{-10}.

The same multiplier is used to support the MCU multiply instructions, which include integer 16-bit signed, unsigned and mixed sign multiply operations.

The `MUL` instruction can be directed to use byte or word-sized operands. Byte operands will direct a 16-bit result and word operands will direct a 32-bit result to the specified register(s) in the W array.

3.6.2 DATA ACCUMULATORS AND ADDER/SUBTRACTER

The data accumulator consists of a 40-bit adder/subtracter with automatic sign extension logic. It can select one of two accumulators (A or B) as its pre-accumulation source and post-accumulation destination. For the `ADD` and `LAC` instructions, the data to be accumulated or loaded can be optionally scaled using the barrel shifter prior to accumulation.

3.6.2.1 Adder/Subtracter, Overflow and Saturation

The adder/subtracter is a 40-bit adder with an optional zero input into one side and either true or complement data into the other input.

- In the case of addition, the Carry/$\overline{\text{Borrow}}$ input is active-high and the other input is true data (not complemented).
- In the case of subtraction, the Carry/$\overline{\text{Borrow}}$ input is active-low and the other input is complemented.

The adder/subtracter generates Overflow Status bits, SA/SB and OA/OB, which are latched and reflected in the STATUS Register:

- Overflow from bit 39: this is a catastrophic overflow in which the sign of the accumulator is destroyed.
- Overflow into guard bits 32 through 39: this is a recoverable overflow. This bit is set whenever all the guard bits are not identical to each other.

The adder has an additional saturation block that controls accumulator data saturation, if selected. It uses the result of the adder, the Overflow Status bits described previously, and the SAT<A:B> (CORCON<7:6>) and ACCSAT (CORCON<4>) mode control bits to determine when and to what value, to saturate.

Six STATUS Register bits support saturation and overflow:

- OA: ACCA overflowed into guard bits
- OB: ACCB overflowed into guard bits
- SA: ACCA saturated (bit 31 overflow and saturation)

  or

  ACCA overflowed into guard bits and saturated (bit 39 overflow and saturation)
- SB: ACCB saturated (bit 31 overflow and saturation)

  or

  ACCB overflowed into guard bits and saturated (bit 39 overflow and saturation)
- OAB: Logical OR of OA and OB
- SAB: Logical OR of SA and SB

The OA and OB bits are modified each time data passes through the adder/subtracter. When set, they indicate that the most recent operation has overflowed into the accumulator guard bits (bits 32 through 39). The OA and OB bits can also optionally generate an arithmetic warning trap when OA and OB are set and the corresponding Overflow Trap Flag Enable bits (OVATE, OVBTE) in the INTCON1 register are set (refer to **Section 7.0 "Interrupt Controller"**). This allows the user application to take immediate action; for example, to correct system gain.

TABLE 4-2: CHANGE NOTIFICATION REGISTER MAP FOR dsPIC33FJXXGP101 DEVICES

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CNEN1	0060	—	—	—	CN12IE	CN11IE	—	—	—	—	—	CN5IE	CN4IE	CN3IE	CN2IE	CN1IE	CN0IE	0000
CNEN2	0062	—	CN30IE	CN29IE	—	—	—	—	—	CN23IE	CN22IE	CN21IE	—	—	—	—	—	0000
CNPU1	0068	—	—	—	CN12PUE	CN11PUE	—	—	—	—	—	CN5PUE	CN4PUE	CN3PUE	CN2PUE	CN1PUE	CN0PUE	0000
CNPU2	006A	—	CN30PUE	CN29PUE	—	—	—	—	—	CN23PUE	CN22PUE	CN21PUE	—	—	—	—	—	0000

Legend: — = unimplemented, read as ‘0’. Reset values are shown in hexadecimal.

TABLE 4-3: CHANGE NOTIFICATION REGISTER MAP FOR dsPIC33FJXXMC101 DEVICES

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CNEN1	0060	—	CN14IE	CN13IE	CN12IE	CN11IE	—	—	—	—	—	CN5IE	CN4IE	CN3IE	CN2IE	CN1IE	CN0IE	0000
CNEN2	0062	—	CN30IE	CN29IE	—	—	—	—	—	CN23IE	CN22IE	CN21IE	—	—	—	—	—	0000
CNPU1	0068	—	CN14PUE	CN13PUE	CN12PUE	CN11PUE	—	—	—	—	—	CN5PUE	CN4PUE	CN3PUE	CN2PUE	CN1PUE	CN0PUE	0000
CNPU2	006A	—	CN30PUE	CN29PUE	—	—	—	—	—	CN23PUE	CN22PUE	CN21PUE	—	—	—	—	—	0000

Legend: — = unimplemented, read as ‘0’. Reset values are shown in hexadecimal.

TABLE 4-4: CHANGE NOTIFICATION REGISTER MAP FOR dsPIC33FJXX(GP/MC)102 DEVICES

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CNEN1	0060	CN15IE	CN14IE	CN13IE	CN12IE	CN11IE	—	—	—	CN7IE	CN6IE	CN5IE	CN4IE	CN3IE	CN2IE	CN1IE	CN0IE	0000
CNEN2	0062	—	CN30IE	CN29IE	—	CN27IE	—	—	CN24IE	CN23IE	CN22IE	CN21IE	—	—	—	—	CN16IE	0000
CNPU1	0068	CN15PUE	CN14PUE	CN13PUE	CN12PUE	CN11PUE	—	—	—	CN7PUE	CN6PUE	CN5PUE	CN4PUE	CN3PUE	CN2PUE	CN1PUE	CN0PUE	0000
CNPU2	006A	—	CN30PUE	CN29PUE	—	CN27PUE	—	—	CN24PUE	CN23PUE	CN22PUE	CN21PUE	—	—	—	—	CN16PUE	0000

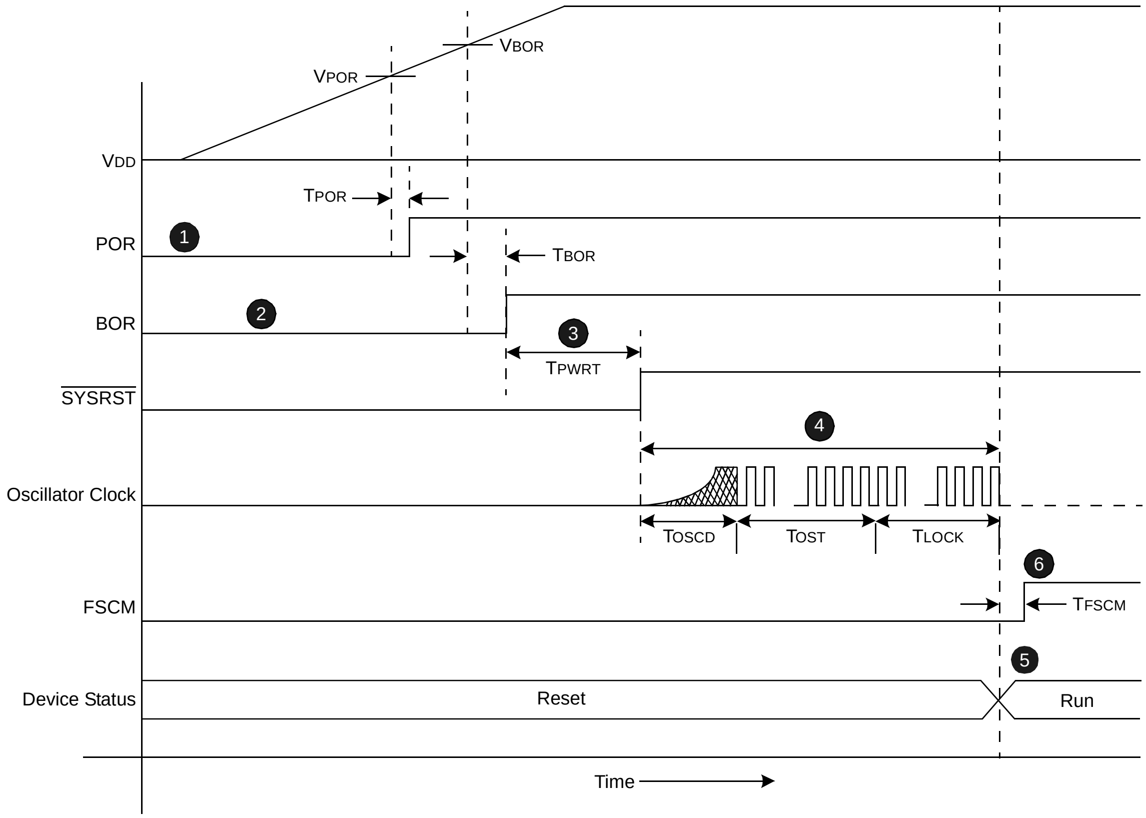
Legend: — = unimplemented, read as ‘0’. Reset values are shown in hexadecimal.

TABLE 4-5: CHANGE NOTIFICATION REGISTER MAP FOR dsPIC33FJ32(GP/MC)104 DEVICES

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CNEN1	0060	CN15IE	CN13IE	CN13IE	CN12IE	CN11IE	CN10IE	CN9IE	CN8IE	CN7IE	CN6IE	CN5IE	CN4IE	CN3IE	CN2IE	CN1IE	CN0IE	0000
CNEN2	0062	—	CN30IE	CN29IE	CN28IE	CN27IE	CN26IE	CN25IE	CN24IE	CN23IE	CN22IE	CN21IE	CN20IE	CN19IE	CN18IE	CN17IE	CN16IE	0000
CNPU1	0068	CN15PUE	CN13PUE	CN13PUE	CN12PUE	CN11PUE	CN10PUE	CN9PUE	CN8PUE	CN7PUE	CN6PUE	CN5PUE	CN4PUE	CN3PUE	CN2PUE	CN1PUE	CN0PUE	0000
CNPU2	006A	—	CN30PUE	CN29PUE	CN28PUE	CN27PUE	CN26PUE	CN25PUE	CN24PUE	CN23PUE	CN22PUE	CN21PUE	CN20PUE	CN19PUE	CN18PUE	CN17PUE	CN16PUE	0000

Legend: — = unimplemented, read as ‘0’. Reset values are shown in hexadecimal.

FIGURE 6-2: SYSTEM RESET TIMING



1. **POR:** A POR circuit holds the device in Reset when the power supply is turned on. The POR circuit is active until V_{DD} crosses the V_{POR} threshold and the delay, T_{POR}, has elapsed.
2. **BOR:** The on-chip voltage regulator has a BOR circuit that keeps the device in Reset until V_{DD} crosses the V_{BOR} threshold and the delay, T_{BOR}, has elapsed. The delay, T_{BOR}, ensures the voltage regulator output becomes stable.
3. **PWRT Timer:** The Power-up Timer continues to hold the processor in Reset for a specific period of time (T_{PWRT}) after a BOR. The delay, T_{PWRT}, ensures that the system power supplies have stabilized at the appropriate level for full-speed operation. After the delay, T_{PWRT}, has elapsed, the $\overline{SYSRST}$ becomes inactive, which in turn, enables the selected oscillator to start generating clock cycles.
4. **Oscillator Delay:** The total delay for the clock to be ready for various clock source selections is given in Table 6-1. Refer to **Section 8.0 "Oscillator Configuration"** for more information.
5. When the oscillator clock is ready, the processor begins execution from location, 0x000000. The user application programs a `GOTO` instruction at the Reset address, which redirects program execution to the appropriate start-up routine.
6. The Fail-Safe Clock Monitor (FSCM), if enabled, begins to monitor the system clock when the system clock is ready and the delay, T_{FSCM}, has elapsed.

TABLE 6-2: OSCILLATOR PARAMETERS

Symbol	Parameter	Value
V_{POR}	POR Threshold	1.8V nominal
T_{POR}	POR Extension Time	30 µs maximum
V_{BOR}	BOR Threshold	2.5V nominal
T_{BOR}	BOR Extension Time	100 µs maximum
T_{PWRT}	Power-up Time Delay	64 ms nominal
T_{FSCM}	Fail-Safe Clock Monitor Delay	900 µs maximum

Note: When the device exits the Reset condition (begins normal operation), the device operating parameters (voltage, frequency, temperature, etc.) must be within their operating ranges; otherwise, the device may not function correctly. The user application must ensure that the delay between the time power is first applied, and the time $\overline{SYSRST}$ becomes inactive, is long enough to get all operating parameters within specification.

6.5 External Reset (EXTR)

The External Reset is generated by driving the $\overline{\text{MCLR}}$ pin low. The $\overline{\text{MCLR}}$ pin is a Schmitt trigger input with an additional glitch filter. Reset pulses that are longer than the minimum pulse width will generate a Reset. Refer to **Section 26.0 "Electrical Characteristics"** for minimum pulse-width specifications. The External Reset pin ($\overline{\text{MCLR}}$) bit (EXTR) in the Reset Control (RCON) register is set to indicate the $\overline{\text{MCLR}}$ Reset.

6.5.1 EXTERNAL SUPERVISORY CIRCUIT

Many systems have external supervisory circuits that generate Reset signals to reset multiple devices in the system. This External Reset signal can be directly connected to the $\overline{\text{MCLR}}$ pin to reset the device when the rest of the system is reset.

6.5.2 INTERNAL SUPERVISORY CIRCUIT

When using the internal power supervisory circuit to reset the device, the External Reset pin ($\overline{\text{MCLR}}$) should be tied directly or resistively to V_{DD}. In this case, the $\overline{\text{MCLR}}$ pin will not be used to generate a Reset. The External Reset pin ($\overline{\text{MCLR}}$) does not have an internal pull-up and must not be left unconnected.

6.6 Software RESET Instruction (SWR)

Whenever the RESET instruction is executed, the device will assert $\overline{\text{SYSRST}}$, placing the device in a special Reset state. This Reset state will not re-initialize the clock. The clock source in effect prior to the RESET instruction will remain as the source. $\overline{\text{SYSRST}}$ is released at the next instruction cycle and the Reset vector fetch will commence.

The Software RESET (Instruction) Flag (SWR) bit in the Reset Control (RCON<6>) register is set to indicate the Software Reset.

6.7 Watchdog Timer Time-out Reset (WDTO)

Whenever a Watchdog Timer Time-out Reset occurs, the device will asynchronously assert $\overline{\text{SYSRST}}$. The clock source will remain unchanged. A WDT time-out during Sleep or Idle mode will wake-up the processor, but will not reset the processor.

The Watchdog Timer Time-out Flag (WDTO) bit in the Reset Control (RCON<4>) register is set to indicate the Watchdog Timer Reset. Refer to **Section 23.4 "Watchdog Timer (WDT)"** for more information on the Watchdog Timer Reset.

6.8 Trap Conflict Reset

If a lower priority hard trap occurs while a higher priority trap is being processed, a hard Trap Conflict Reset occurs. The hard traps include exceptions of Priority Level 13 through Level 15, inclusive. The address error (Level 13) and oscillator error (Level 14) traps fall into this category.

The Trap Reset Flag (TRAPR) bit in the Reset Control (RCON<15>) register is set to indicate the Trap Conflict Reset. Refer to **Section 7.0 "Interrupt Controller"** for more information on Trap Conflict Resets.

6.9 Configuration Mismatch Reset

To maintain the integrity of the Peripheral Pin Select Control registers, they are constantly monitored with shadow registers in hardware. If an unexpected change in any of the registers occurs (such as cell disturbances caused by ESD or other external events), a Configuration Mismatch Reset occurs.

The Configuration Mismatch Flag (CM) bit in the Reset Control (RCON<9>) register is set to indicate the Configuration Mismatch Reset. Refer to **Section 10.0 "I/O Ports"** for more information on the Configuration Mismatch Reset.

Note:	The Configuration Mismatch feature and associated Reset flag is not available on all devices.

6.10 Illegal Condition Device Reset

An Illegal Condition Device Reset occurs due to the following sources:

- Illegal Opcode Reset
- Uninitialized W Register Reset
- Security Reset

The Illegal Opcode or Uninitialized W Access Reset Flag (IOPUWR) bit in the Reset Control (RCON<14>) register is set to indicate the Illegal Condition Device Reset.

6.10.1 ILLEGAL OPCODE RESET

A device Reset is generated if the device attempts to execute an illegal opcode value that is fetched from program memory.

The Illegal Opcode Reset function can prevent the device from executing program memory sections that are used to store constant data. To take advantage of the Illegal Opcode Reset, use only the lower 16 bits of each program memory section to store the data values. The upper 8 bits should be programmed with 0x3F, which is an illegal opcode value.

REGISTER 7-11: IEC1: INTERRUPT ENABLE CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
—	—	INT2IE	T5IE(1)	T4IE(1)	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	INT1IE	CNIE	CMIE	MI2C1IE	SI2C1IE
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13 **INT2IE:** External Interrupt 2 Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 12 **T5IE:** Timer5 Interrupt Enable bit(1)
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 11 **T4IE:** Timer4 Interrupt Enable bit(1)
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 10-5 **Unimplemented:** Read as ‘0’

bit 4 **INT1IE:** External Interrupt 1 Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 3 **CNIE:** Input Change Notification Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 2 **CMIE:** Comparator Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 1 **MI2C1IE:** I2C1 Master Events Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 0 **SI2C1IE:** I2C1 Slave Events Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

Note 1: These bits are available in dsPIC33FJ32(GP/MC)10X devices only.

REGISTER 10-15: RPOR4: PERIPHERAL PIN SELECT OUTPUT REGISTER 4

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	RP9R<4:0>				
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	RP8R<4:0>				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-13 **Unimplemented:** Read as ‘0’

bit 12-8 **RP9R<4:0>:** Peripheral Output Function is Assigned to RP9 Output Pin bits (see Table 10-2 for peripheral function numbers)

bit 7-5 **Unimplemented:** Read as ‘0’

bit 4-0 **RP8R<4:0>:** Peripheral Output Function is Assigned to RP8 Output Pin bits (see Table 10-2 for peripheral function numbers)

REGISTER 10-16: RPOR5: PERIPHERAL PIN SELECT OUTPUT REGISTER 5

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	RP11R<4:0>(1)				
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	RP10R<4:0>(1)				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-13 **Unimplemented:** Read as ‘0’

bit 12-8 **RP11R<4:0>:** Peripheral Output Function is Assigned to RP11 Output Pin bits(1) (see Table 10-2 for peripheral function numbers)

bit 7-5 **Unimplemented:** Read as ‘0’

bit 4-0 **RP10R<4:0>:** Peripheral Output Function is Assigned to RP10 Output Pin bits(1) (see Table 10-2 for peripheral function numbers)

Note 1: These bits are not available in dsPIC33FJXX(GP/MC)101 devices.

REGISTER 12-4: T5CON: TIMER5 CONTROL REGISTER(1)

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
TON(3)	—	TSIDL(2)	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	U-0
—	TGATE(3)	TCKPS1(3)	TCKPS0(3)	—	—	TCS(3)	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **TON:** Timer5 On bit(3)
1 = Starts 16-bit Timer3
0 = Stops 16-bit Timer3

bit 14 **Unimplemented:** Read as '0'

bit 13 **TSIDL:** Timer5 Stop in Idle Mode bit(2)
1 = Discontinues timer operation when device enters Idle mode
0 = Continues timer operation in Idle mode

bit 12-7 **Unimplemented:** Read as '0'

bit 6 **TGATE:** Timer5 Gated Time Accumulation Enable bit(3)
When TCS = 1:
This bit is ignored.
When TCS = 0:
1 = Gated time accumulation is enabled
0 = Gated time accumulation is disabled

bit 5-4 **TCKPS<1:0>:** Timer5 Input Clock Prescale Select bits(3)
11 = 1:256 prescale value
10 = 1:64 prescale value
01 = 1:8 prescale value
00 = 1:1 prescale value

bit 3-2 **Unimplemented:** Read as '0'

bit 1 **TCS:** Timer5 Clock Source Select bit(3)
1 = External clock from T5CK pin
0 = Internal clock (FOSC/2)

bit 0 **Unimplemented:** Read as '0'

Note 1: This register is available in dsPIC33FJ32(GP/MC)10X devices only.
2: When 32-bit timer operation is enabled (T32 = 1) in the Timer4 Control register (T4CON<3>), the TSIDL bit must be cleared to operate the 32-bit timer in Idle mode.
3: When the 32-bit timer operation is enabled (T32 = 1) in the Timer4 Control register (T4CON<3>), these bits have no effect.

16.1 SPI Helpful Tips

1. In Frame mode, if there is a possibility that the master may not be initialized before the slave:
   a) If FRMPOL (SPIxCON2<13>) = `1`, use a pull-down resistor on $\overline{\text{SSx}}$.
   b) If FRMPOL = `0`, use a pull-up resistor on $\overline{\text{SSx}}$.

Note:	This insures that the first frame transmission after initialization is not shifted or corrupted.

2. In Non-Framed 3-Wire mode (i.e., not using $\overline{\text{SSx}}$ from a master):
   a) If CKP (SPIxCON1<6>) = `1`, always place a pull-up resistor on $\overline{\text{SSx}}$.
   b) If CKP = `0`, always place a pull-down resistor on $\overline{\text{SSx}}$.

Note:	This will insure that during power-up and initialization, the master/slave will not lose sync due to an errant SCK transition that would cause the slave to accumulate data shift errors for both transmit and receive, appearing as corrupted data.

3. FRMEN (SPIxCON2<15>) = `1` and SSEN (SPIxCON1<7>) = `1` are exclusive and invalid. In Frame mode, SCKx is continuous and the Frame Sync pulse is active on the $\overline{\text{SSx}}$ pin, which indicates the start of a data frame.

Note:	Not all third-party devices support Frame mode timing. Refer to the SPI electrical characteristics for details.

4. In Master mode only, set the SMP bit (SPIxCON1<9>) to a '1' for the fastest SPI data rate possible. The SMP bit can only be set at the same time or after the MSTEN bit (SPIxCON1<5>) is set.
5. To avoid invalid slave read data to the master, the user's master software must ensure enough time for slave software to fill its write buffer before the user application initiates a master write/read cycle. It is always advisable to preload the SPIxBUF Transmit register in advance of the next master transaction cycle. SPIxBUF is transferred to the SPIx Shift register and is empty once the data transmission begins.
6. The SPI related pins (SDI1, SDO1, SCK1) are located at fixed positions in the dsPIC33FJ16(GP/MC)10X devices. The same pins are remappable in the dsPIC33FJ32(GP/MC)10X devices.

16.2 SPI Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en554109

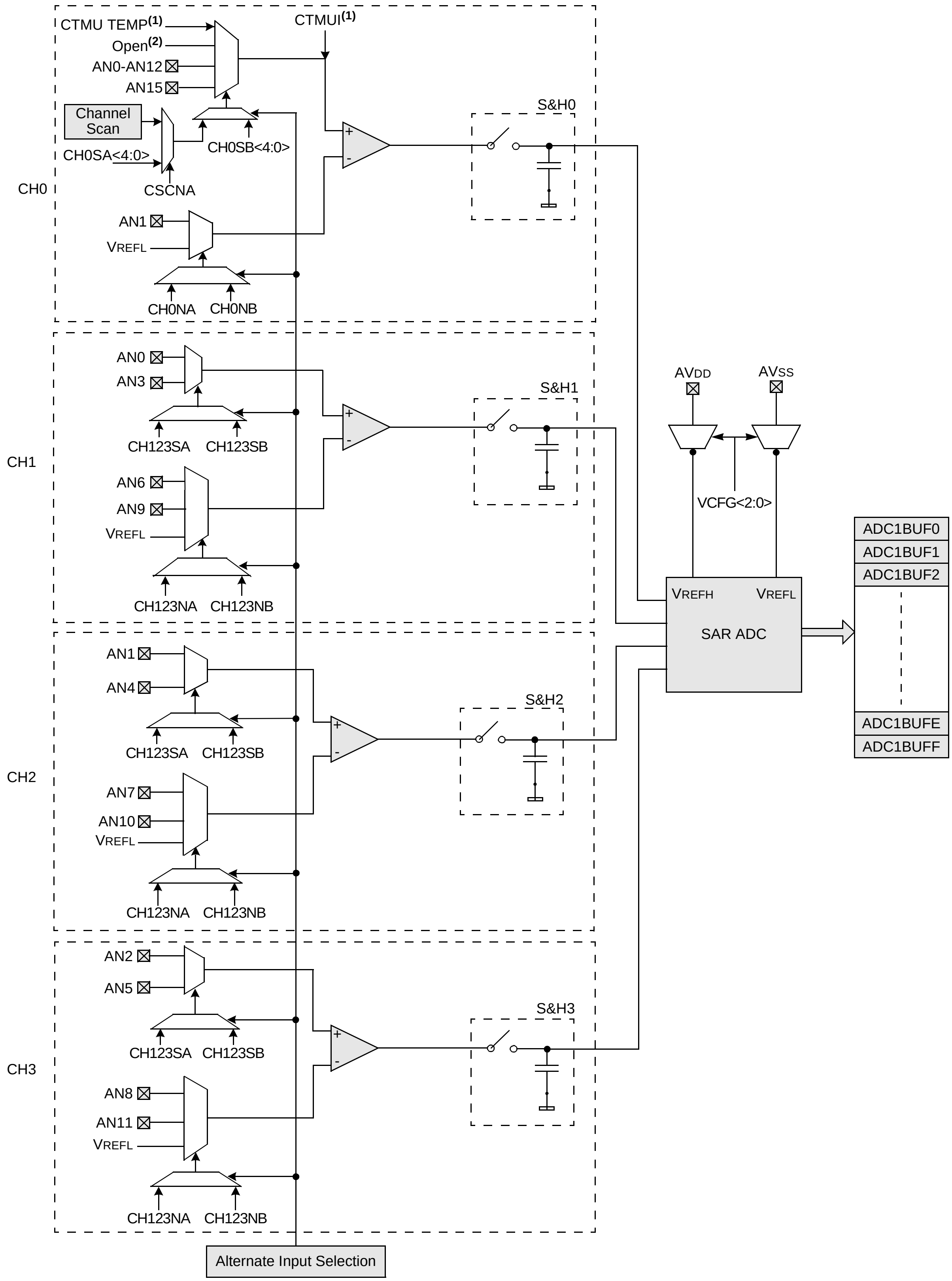
16.2.1 KEY RESOURCES

- **"Serial Peripheral Interface (SPI)"** (DS70206) in the "*dsPIC33/PIC24 Family Reference Manual*".
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related "*dsPIC33/PIC24 Family Reference Manual*" sections
- Development Tools

REGISTER 17-1: I2CxCON: I2Cx CONTROL REGISTER (CONTINUED)

bit 6	**STREN:** SCLx Clock Stretch Enable bit (when operating as I^2C slave) Used in conjunction with the SCLREL bit. 1 = Enables software or receives clock stretching 0 = Disables software or receives clock stretching
bit 5	**ACKDT:** Acknowledge Data bit (when operating as I^2C master, applicable during master receive) Value that will be transmitted when the software initiates an Acknowledge sequence. 1 = Sends NACK during Acknowledge 0 = Sends ACK during Acknowledge
bit 4	**ACKEN:** Acknowledge Sequence Enable bit (when operating as I^2C master, applicable during master receive) 1 = Initiates Acknowledge sequence on SDAx and SCLx pins and transmits ACKDT data bit; hardware clears at end of master Acknowledge sequence 0 = Acknowledge sequence is not in progress
bit 3	**RCEN:** Receive Enable bit (when operating as I^2C master) 1 = Enables Receive mode for I^2C; hardware clears at end of eighth bit of the master receive data byte 0 = Receive sequence is not in progress
bit 2	**PEN:** Stop Condition Enable bit (when operating as I^2C master) 1 = Initiates Stop condition on SDAx and SCLx pins; hardware clears at end of the master Stop sequence 0 = Stop condition not in progress
bit 1	**RSEN:** Repeated Start Condition Enable bit (when operating as I^2C master) 1 = Initiates Repeated Start condition on SDAx and SCLx pins; hardware clears at end of the master Repeated Start sequence 0 = Repeated Start condition is not in progress
bit 0	**SEN:** Start Condition Enable bit (when operating as I^2C master) 1 = Initiates Start condition on SDAx and SCLx pins; hardware clears at end of master Start sequence 0 = Start condition is not in progress

FIGURE 19-3: ADC1 BLOCK DIAGRAM FOR dsPIC33FJ32(GP/MC)104 DEVICES



Note 1: Internally connected to the CTMU module.

2: This selection is only used with CTMU capacitive and time measurement.

22.1 CTMU Control Registers

REGISTER 22-1: CTMUCON1: CTMU CONTROL REGISTER 1

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CTMUEN	—	CTMUSIDL	TGEN(1)	EDGEN	EDGSEQEN	IDISSEN(2)	CTTRIG
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **CTMUEN:** CTMU Enable bit
1 = Module is enabled
0 = Module is disabled

bit 14 **Unimplemented:** Read as ‘0’

bit 13 **CTMUSIDL:** CTMU Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12 **TGEN:** Time Generation Enable bit(1)
1 = Enables edge delay generation
0 = Disables edge delay generation

bit 11 **EDGEN:** Edge Enable bit
1 = Edges are not blocked
0 = Edges are blocked

bit 10 **EDGSEQEN:** Edge Sequence Enable bit
1 = Edge 1 event must occur before Edge 2 event can occur
0 = No edge sequence is needed

bit 9 **IDISSEN:** Analog Current Source Control bit(2)
1 = Analog current source output is grounded
0 = Analog current source output is not grounded

bit 8 **CTTRIG:** CTMU Trigger Control bit
1 = Trigger output is enabled
0 = Trigger output is disabled

bit 7-0 **Unimplemented:** Read as ‘0’

Note 1: If TGEN = 1, the peripheral inputs and outputs must be configured to an available RPn pin. For more information, see **Section 10.4 “Peripheral Pin Select (PPS)”**.

2: The ADC module S&H capacitor is not automatically discharged between sample/conversion cycles. Software using the ADC as part of a capacitance measurement must discharge the ADC capacitor before conducting the measurement. The IDISSEN bit, when set to ‘1’, performs this function. The ADC must be sampling while the IDISSEN bit is active to connect the discharge sink to the capacitor array.

23.0 SPECIAL FEATURES

> **Note 1:** This data sheet summarizes the features of the dsPIC33FJ16(GP/MC)101/102 and dsPIC33FJ32(GP/MC)101/102/104 devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Programming and Diagnostics"** (DS70207) and **"Device Configuration"** (DS70194) in the *"dsPIC33/PIC24 Family Reference Manual"*, which are available from the Microchip web site (www.microchip.com).
>
> **2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

dsPIC33FJ16(GP/MC)101/102 and dsPIC33FJ32(GP/MC)101/102/104 devices include several features intended to maximize application flexibility and reliability, and minimize cost through elimination of external components. These are:

- Flexible Configuration
- Watchdog Timer (WDT)
- Code Protection
- In-Circuit Serial Programming™ (ICSP™)
- In-Circuit Emulation

23.1 Configuration Bits

The Configuration Shadow register bits can be configured (read as '0') or left unprogrammed (read as '1') to select various device configurations. These read-only bits are mapped starting at program memory location, 0xF80000. A detailed explanation of the various bit functions is provided in Table 23-4.

Note that address, 0xF80000, is beyond the user program memory space and belongs to the configuration memory space (0x800000-0xFFFFFF), which can only be accessed using Table Reads.

In dsPIC33FJ16(GP/MC)101/102 and dsPIC33FJ32(GP/MC)101/102/104 devices, the Configuration bytes are implemented as volatile memory. This means that configuration data must be programmed each time the device is powered up. Configuration data is stored in the two words at the top of the on-chip program memory space, known as the Flash Configuration Words. Their specific locations are shown in Table 23-2. These are packed representations of the actual device Configuration bits, whose actual locations are distributed among several locations in configuration space. The configuration data is automatically loaded from the Flash Configuration Words to the proper Configuration registers during device Resets.

> **Note:** Configuration data is reloaded on all types of device Resets.

When creating applications for these devices, users should always specifically allocate the location of the Flash Configuration Word for configuration data. This is to make certain that program code is not stored in this address when the code is compiled.

The upper byte of all Flash Configuration Words in program memory should always be '1111 1111'. This makes them appear to be NOP instructions in the remote event that their locations are ever executed by accident. Since Configuration bits are not implemented in the corresponding locations, writing '1's to these locations has no effect on device operation.

> **Note:** Performing a page erase operation on the last page of program memory clears the Flash Configuration Words, enabling code protection as a result. Therefore, users should avoid performing page erase operations on the last page of program memory.

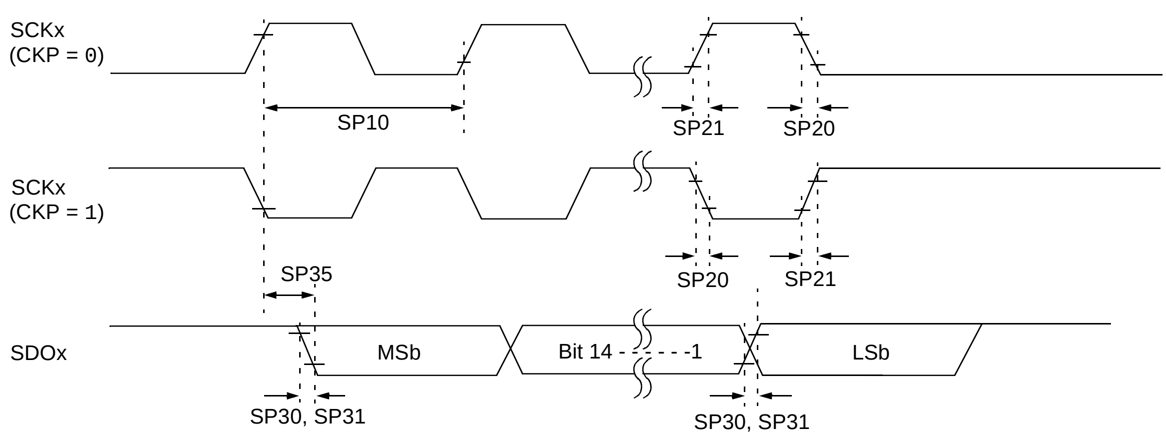
TABLE 24-2: INSTRUCTION SET OVERVIEW

Base Instr #	Assembly Mnemonic	Assembly Syntax		Description	# of Words	# of Cycles	Status Flags Affected
1	ADD	ADD	Acc	Add Accumulators	1	1	OA,OB,SA,SB
		ADD	f	f = f + WREG	1	1	C,DC,N,OV,Z
		ADD	f,WREG	WREG = f + WREG	1	1	C,DC,N,OV,Z
		ADD	#lit10,Wn	Wd = lit10 + Wd	1	1	C,DC,N,OV,Z
		ADD	Wb,Ws,Wd	Wd = Wb + Ws	1	1	C,DC,N,OV,Z
		ADD	Wb,#lit5,Wd	Wd = Wb + lit5	1	1	C,DC,N,OV,Z
		ADD	Wso,#Slit4,Acc	16-bit Signed Add to Accumulator	1	1	OA,OB,SA,SB
2	ADDC	ADDC	f	f = f + WREG + (C)	1	1	C,DC,N,OV,Z
		ADDC	f,WREG	WREG = f + WREG + (C)	1	1	C,DC,N,OV,Z
		ADDC	#lit10,Wn	Wd = lit10 + Wd + (C)	1	1	C,DC,N,OV,Z
		ADDC	Wb,Ws,Wd	Wd = Wb + Ws + (C)	1	1	C,DC,N,OV,Z
		ADDC	Wb,#lit5,Wd	Wd = Wb + lit5 + (C)	1	1	C,DC,N,OV,Z
3	AND	AND	f	f = f .AND. WREG	1	1	N,Z
		AND	f,WREG	WREG = f .AND. WREG	1	1	N,Z
		AND	#lit10,Wn	Wd = lit10 .AND. Wd	1	1	N,Z
		AND	Wb,Ws,Wd	Wd = Wb .AND. Ws	1	1	N,Z
		AND	Wb,#lit5,Wd	Wd = Wb .AND. lit5	1	1	N,Z
4	ASR	ASR	f	f = Arithmetic Right Shift f	1	1	C,N,OV,Z
		ASR	f,WREG	WREG = Arithmetic Right Shift f	1	1	C,N,OV,Z
		ASR	Ws,Wd	Wd = Arithmetic Right Shift Ws	1	1	C,N,OV,Z
		ASR	Wb,Wns,Wnd	Wnd = Arithmetic Right Shift Wb by Wns	1	1	N,Z
		ASR	Wb,#lit5,Wnd	Wnd = Arithmetic Right Shift Wb by lit5	1	1	N,Z
5	BCLR	BCLR	f,#bit4	Bit Clear f	1	1	None
		BCLR	Ws,#bit4	Bit Clear Ws	1	1	None
6	BRA	BRA	C,Expr	Branch if Carry	1	1 (2)	None
		BRA	GE,Expr	Branch if greater than or equal	1	1 (2)	None
		BRA	GEU,Expr	Branch if unsigned greater than or equal	1	1 (2)	None
		BRA	GT,Expr	Branch if greater than	1	1 (2)	None
		BRA	GTU,Expr	Branch if unsigned greater than	1	1 (2)	None
		BRA	LE,Expr	Branch if less than or equal	1	1 (2)	None
		BRA	LEU,Expr	Branch if unsigned less than or equal	1	1 (2)	None
		BRA	LT,Expr	Branch if less than	1	1 (2)	None
		BRA	LTU,Expr	Branch if unsigned less than	1	1 (2)	None
		BRA	N,Expr	Branch if Negative	1	1 (2)	None
		BRA	NC,Expr	Branch if Not Carry	1	1 (2)	None
		BRA	NN,Expr	Branch if Not Negative	1	1 (2)	None
		BRA	NOV,Expr	Branch if Not Overflow	1	1 (2)	None
		BRA	NZ,Expr	Branch if Not Zero	1	1 (2)	None
		BRA	OA,Expr	Branch if Accumulator A overflow	1	1 (2)	None
		BRA	OB,Expr	Branch if Accumulator B overflow	1	1 (2)	None
		BRA	OV,Expr	Branch if Overflow	1	1 (2)	None
		BRA	SA,Expr	Branch if Accumulator A saturated	1	1 (2)	None
		BRA	SB,Expr	Branch if Accumulator B saturated	1	1 (2)	None
		BRA	Expr	Branch Unconditionally	1	2	None
		BRA	Z,Expr	Branch if Zero	1	1 (2)	None
		BRA	Wn	Computed Branch	1	2	None
7	BSET	BSET	f,#bit4	Bit Set f	1	1	None
		BSET	Ws,#bit4	Bit Set Ws	1	1	None
8	BSW	BSW.C	Ws,Wb	Write C bit to Ws<Wb>	1	1	None
		BSW.Z	Ws,Wb	Write Z bit to Ws<Wb>	1	1	None

TABLE 26-29: SPIx MAXIMUM DATA/CLOCK RATE SUMMARY FOR dsPIC33FJ16(GP/MC)10X

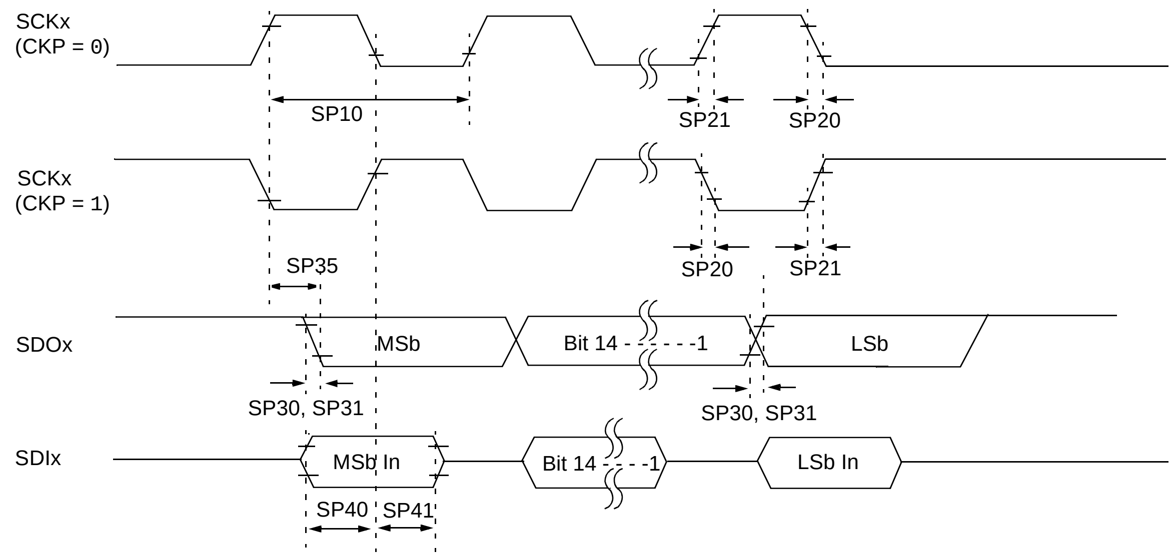
AC CHARACTERISTICS			Standard Operating Conditions: 2.4V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Maximum Data Rate	**Master Transmit Only (Half-Duplex)**	**Master Transmit/Receive (Full-Duplex)**	**Slave Transmit/Receive (Full-Duplex)**	**CKE**	**CKP**	**SMP**
15 MHz	Table 26-30	—	—	0,1	0,1	0,1
10 MHz	—	Table 26-31	—	1	0,1	1
10 MHz	—	Table 26-32	—	0	0,1	1
15 MHz	—	—	Table 26-33	1	0	0
11 MHz	—	—	Table 26-34	1	1	0
15 MHz	—	—	Table 26-35	0	1	0
11 MHz	—	—	Table 26-36	0	0	0

FIGURE 26-11: SPIx MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY, CKE = 0) TIMING CHARACTERISTICS FOR dsPIC33FJ16(GP/MC)10X



Note: Refer to Figure 26-1 for load conditions.

FIGURE 26-14: SPIx MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1) TIMING CHARACTERISTICS FOR dsPIC33FJ16(GP/MC)10X



Note: Refer to Figure 26-1 for load conditions.

TABLE 26-32: SPIx MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1) TIMING REQUIREMENTS FOR dsPIC33FJ16(GP/MC)10X

AC CHARACTERISTICS			Standard Operating Conditions: 2.4V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic(1)**	**Min**	**Typ(2)**	**Max**	**Units**	**Conditions**
SP10	TscP	Maximum SCKx Frequency	—	—	10	MHz	-40°C to +125°C, see **Note 3**
SP20	TscF	SCKx Output Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP21	TscR	SCKx Output Rise Time	—	—	—	ns	See Parameter DO31 and **Note 4**
SP30	TdoF	SDOx Data Output Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP31	TdoR	SDOx Data Output Rise Time	—	—	—	ns	See Parameter DO31 and **Note 4**
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	—	—	ns	

Note 1: These parameters are characterized, but are not tested in manufacturing.
2: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.
3: The minimum clock period for SCKx is 100 ns. The clock generated in Master mode must not violate this specification.
4: Assumes 50 pF load on all SPIx pins.

TABLE 26-44: SPIx SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0) TIMING REQUIREMENTS FOR dsPIC33FJ32(GP/MC)10X

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic(1)**	**Min**	**Typ(2)**	**Max**	**Units**	**Conditions**
SP70	TscP	Maximum SCKx Input Frequency	—	—	11	MHz	See **Note 3**
SP72	TscF	SCKx Input Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP73	TscR	SCKx Input Rise Time	—	—	—	ns	See Parameter DO31 and **Note 4**
SP30	TdoF	SDOx Data Output Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP31	TdoR	SDOx Data Output Rise Time	—	—	—	ns	See Parameter DO31 and **Note 4**
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{\text{SSx}}$ ↓ to SCKx ↑ or SCKx Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{\text{SSx}}$ ↑ to SDOx Output High-Impedance	10	—	50	ns	See **Note 4**
SP52	TscH2ssH TscL2ssH	$\overline{\text{SSx}}$ after SCKx Edge	1.5 TCY + 40	—	—	ns	See **Note 4**

Note 1: These parameters are characterized, but are not tested in manufacturing.
2: Data in “Typ” column is at 3.3V, +25°C unless otherwise stated.
3: The minimum clock period for SCKx is 91 ns. Therefore, the SCKx clock generated by the Master must not violate this specification.
4: Assumes 50 pF load on all SPIx pins.

TABLE 26-45: I2Cx BUS DATA TIMING REQUIREMENTS (MASTER MODE)

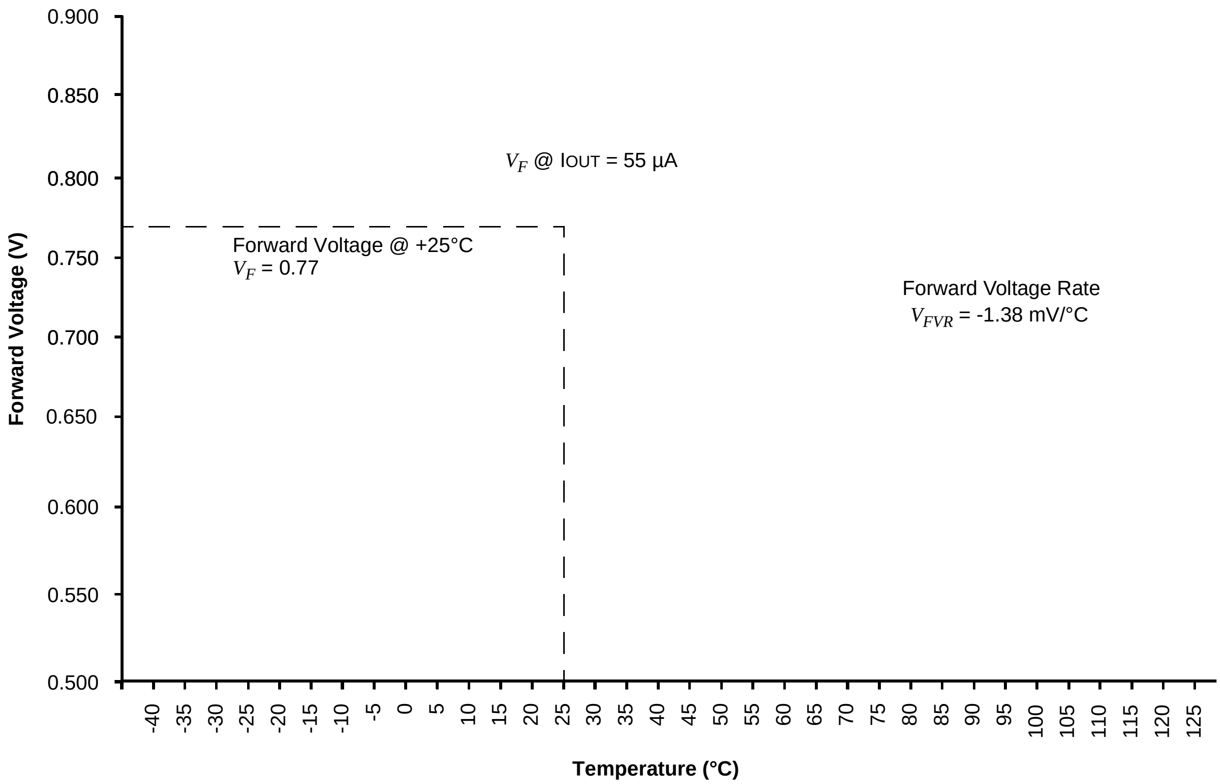
<table>
<tr><td colspan="4">AC CHARACTERISTICS</td><td colspan="4">Standard Operating Conditions: 3.0V to 3.6V
(unless otherwise stated)
Operating temperature -40°C ≤ TA ≤ +85°C for Industrial
-40°C ≤ TA ≤ +125°C for Extended</td></tr>
<tr><th>Param No.</th><th>Symbol</th><th colspan="2">Characteristic</th><th>Min(1)</th><th>Max</th><th>Units</th><th>Conditions</th></tr>
<tr><td rowspan="3">IM10</td><td rowspan="3">TLO:SCL</td><td rowspan="3">Clock Low Time</td><td>100 kHz mode</td><td>TCY/2 (BRG + 1)</td><td>—</td><td>μs</td><td></td></tr>
<tr><td>400 kHz mode</td><td>TCY/2 (BRG + 1)</td><td>—</td><td>μs</td><td></td></tr>
<tr><td>1 MHz mode(2)</td><td>TCY/2 (BRG + 1)</td><td>—</td><td>μs</td><td></td></tr>
<tr><td rowspan="3">IM11</td><td rowspan="3">THI:SCL</td><td rowspan="3">Clock High Time</td><td>100 kHz mode</td><td>TCY/2 (BRG + 1)</td><td>—</td><td>μs</td><td></td></tr>
<tr><td>400 kHz mode</td><td>TCY/2 (BRG + 1)</td><td>—</td><td>μs</td><td></td></tr>
<tr><td>1 MHz mode(2)</td><td>TCY/2 (BRG + 1)</td><td>—</td><td>μs</td><td></td></tr>
<tr><td rowspan="3">IM20</td><td rowspan="3">TF:SCL</td><td rowspan="3">SDAx and SCLx Fall Time</td><td>100 kHz mode</td><td>—</td><td>300</td><td>ns</td><td rowspan="3">CB is specified to be from 10 to 400 pF</td></tr>
<tr><td>400 kHz mode</td><td>20 + 0.1 CB</td><td>300</td><td>ns</td></tr>
<tr><td>1 MHz mode(2)</td><td>—</td><td>100</td><td>ns</td></tr>
<tr><td rowspan="3">IM21</td><td rowspan="3">TR:SCL</td><td rowspan="3">SDAx and SCLx Rise Time</td><td>100 kHz mode</td><td>—</td><td>1000</td><td>ns</td><td rowspan="3">CB is specified to be from 10 to 400 pF</td></tr>
<tr><td>400 kHz mode</td><td>20 + 0.1 CB</td><td>300</td><td>ns</td></tr>
<tr><td>1 MHz mode(2)</td><td>—</td><td>300</td><td>ns</td></tr>
<tr><td rowspan="3">IM25</td><td rowspan="3">TSU:DAT</td><td rowspan="3">Data Input Setup Time</td><td>100 kHz mode</td><td>250</td><td>—</td><td>ns</td><td rowspan="3"></td></tr>
<tr><td>400 kHz mode</td><td>100</td><td>—</td><td>ns</td></tr>
<tr><td>1 MHz mode(2)</td><td>40</td><td>—</td><td>ns</td></tr>
<tr><td rowspan="3">IM26</td><td rowspan="3">THD:DAT</td><td rowspan="3">Data Input Hold Time</td><td>100 kHz mode</td><td>0</td><td>—</td><td>μs</td><td rowspan="3"></td></tr>
<tr><td>400 kHz mode</td><td>0</td><td>0.9</td><td>μs</td></tr>
<tr><td>1 MHz mode(2)</td><td>0.2</td><td>—</td><td>μs</td></tr>
<tr><td rowspan="3">IM30</td><td rowspan="3">TSU:STA</td><td rowspan="3">Start Condition Setup Time</td><td>100 kHz mode</td><td>TCY/2 (BRG + 1)</td><td>—</td><td>μs</td><td rowspan="3">Only relevant for Repeated Start condition</td></tr>
<tr><td>400 kHz mode</td><td>TCY/2 (BRG + 1)</td><td>—</td><td>μs</td></tr>
<tr><td>1 MHz mode(2)</td><td>TCY/2 (BRG + 1)</td><td>—</td><td>μs</td></tr>
<tr><td rowspan="3">IM31</td><td rowspan="3">THD:STA</td><td rowspan="3">Start Condition Hold Time</td><td>100 kHz mode</td><td>TCY/2 (BRG + 1)</td><td>—</td><td>μs</td><td rowspan="3">After this period the first clock pulse is generated</td></tr>
<tr><td>400 kHz mode</td><td>TCY/2 (BRG + 1)</td><td>—</td><td>μs</td></tr>
<tr><td>1 MHz mode(2)</td><td>TCY/2 (BRG + 1)</td><td>—</td><td>μs</td></tr>
<tr><td rowspan="3">IM33</td><td rowspan="3">TSU:STO</td><td rowspan="3">Stop Condition Setup Time</td><td>100 kHz mode</td><td>TCY/2 (BRG + 1)</td><td>—</td><td>μs</td><td rowspan="3"></td></tr>
<tr><td>400 kHz mode</td><td>TCY/2 (BRG + 1)</td><td>—</td><td>μs</td></tr>
<tr><td>1 MHz mode(2)</td><td>TCY/2 (BRG + 1)</td><td>—</td><td>μs</td></tr>
<tr><td rowspan="3">IM34</td><td rowspan="3">THD:STO</td><td rowspan="3">Stop Condition Hold Time</td><td>100 kHz mode</td><td>TCY/2 (BRG + 1)</td><td>—</td><td>ns</td><td rowspan="3"></td></tr>
<tr><td>400 kHz mode</td><td>TCY/2 (BRG + 1)</td><td>—</td><td>ns</td></tr>
<tr><td>1 MHz mode(2)</td><td>TCY/2 (BRG + 1)</td><td>—</td><td>ns</td></tr>
<tr><td rowspan="3">IM40</td><td rowspan="3">TAA:SCL</td><td rowspan="3">Output Valid from Clock</td><td>100 kHz mode</td><td>—</td><td>3500</td><td>ns</td><td></td></tr>
<tr><td>400 kHz mode</td><td>—</td><td>1000</td><td>ns</td><td></td></tr>
<tr><td>1 MHz mode(2)</td><td>—</td><td>400</td><td>ns</td><td></td></tr>
<tr><td rowspan="3">IM45</td><td rowspan="3">TBF:SDA</td><td rowspan="3">Bus Free Time</td><td>100 kHz mode</td><td>4.7</td><td>—</td><td>μs</td><td rowspan="3">Time the bus must be free before a new transmission can start</td></tr>
<tr><td>400 kHz mode</td><td>1.3</td><td>—</td><td>μs</td></tr>
<tr><td>1 MHz mode(2)</td><td>0.5</td><td>—</td><td>μs</td></tr>
<tr><td>IM50</td><td>CB</td><td colspan="2">Bus Capacitive Loading</td><td>—</td><td>400</td><td>pF</td><td></td></tr>
<tr><td>IM51</td><td>TPGD</td><td colspan="2">Pulse Gobbler Delay</td><td>65</td><td>390</td><td>ns</td><td>See Note 3</td></tr>
</table>

Note 1: BRG is the value of the I²C™ Baud Rate Generator. Refer to **"Inter-Integrated Circuit (I²C™)"** (DS70195) in the "*dsPIC33/PIC24 Family Reference Manual*". Please see the Microchip web site for the latest *"dsPIC33/PIC24 Family Reference Manual"* sections.

2: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

3: Typical value for this parameter is 130 ns.

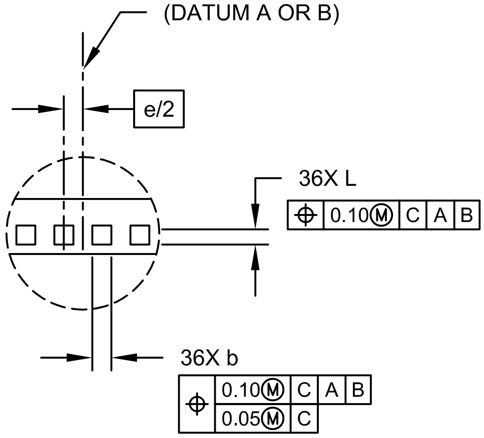
FIGURE 26-33: FORWARD VOLTAGE VERSUS TEMPERATURE



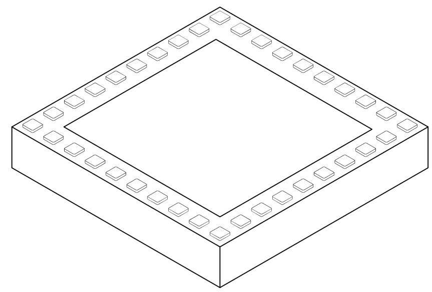
Note: This graph is a statistical summary based on a limited number of samples and this data is characterized but not tested in manufacturing.

36-Terminal Very Thin Thermal Leadless Array Package (TL) – 5x5x0.9 mm Body with Exposed Pad [VTLA]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



DETAIL A



Units		MILLIMETERS		
Dimension	Limits	MIN	NOM	MAX
Number of Pins	N		36	
Number of Pins per Side	ND		10	
Number of Pins per Side	NE		8	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.025	-	0.075
Overall Width	E		5.00 BSC	
Exposed Pad Width	E2	3.60	3.75	3.90
Overall Length	D		5.00 BSC	
Exposed Pad Length	D2	3.60	3.75	3.90
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.20	0.25	0.30
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-187C Sheet 2 of 2