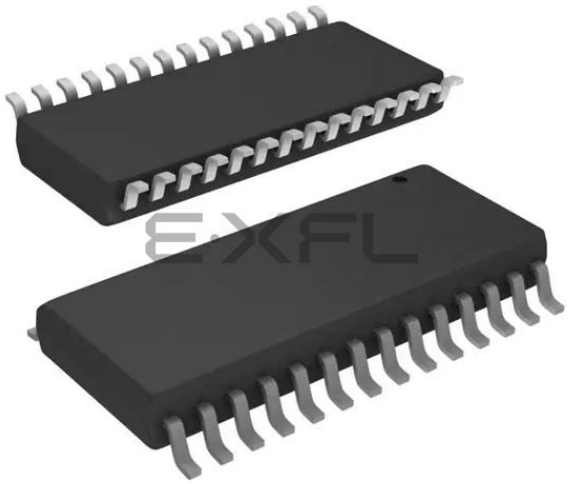
# Microchip Technology - DSPIC33FJ32MC102T-I/SO Datasheet



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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | dsPIC |
| Core Size | 16-Bit |
| Speed | 16 MIPs |
| Connectivity | I²C, IrDA, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, Motor Control PWM, POR, PWM, WDT |
| Number of I/O | 21 |
| Program Memory Size | 32KB (11K x 24) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 1K x 16 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 3.6V |
| Data Converters | A/D 8x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 28-SOIC (0.295", 7.50mm Width) |
| Supplier Device Package | 28-SOIC |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj32mc102t-i-so |

**TABLE 4-1: CPU CORE REGISTER MAP**

| SFR Name | SFR Addr | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| WREG0 | 0000 | Working Register 0 | | | | | | | | | | | | | | | | xxxx |
| WREG1 | 0002 | Working Register 1 | | | | | | | | | | | | | | | | xxxx |
| WREG2 | 0004 | Working Register 2 | | | | | | | | | | | | | | | | xxxx |
| WREG3 | 0006 | Working Register 3 | | | | | | | | | | | | | | | | xxxx |
| WREG4 | 0008 | Working Register 4 | | | | | | | | | | | | | | | | xxxx |
| WREG5 | 000A | Working Register 5 | | | | | | | | | | | | | | | | xxxx |
| WREG6 | 000C | Working Register 6 | | | | | | | | | | | | | | | | xxxx |
| WREG7 | 000E | Working Register 7 | | | | | | | | | | | | | | | | xxxx |
| WREG8 | 0010 | Working Register 8 | | | | | | | | | | | | | | | | xxxx |
| WREG9 | 0012 | Working Register 9 | | | | | | | | | | | | | | | | xxxx |
| WREG10 | 0014 | Working Register 10 | | | | | | | | | | | | | | | | xxxx |
| WREG11 | 0016 | Working Register 11 | | | | | | | | | | | | | | | | xxxx |
| WREG12 | 0018 | Working Register 12 | | | | | | | | | | | | | | | | xxxx |
| WREG13 | 001A | Working Register 13 | | | | | | | | | | | | | | | | xxxx |
| WREG14 | 001C | Working Register 14 | | | | | | | | | | | | | | | | xxxx |
| WREG15 | 001E | Working Register 15 | | | | | | | | | | | | | | | | 0800 |
| SPLIM | 0020 | Stack Pointer Limit Register | | | | | | | | | | | | | | | | xxxx |
| ACCAL | 0022 | Accumulator A Low Word Register | | | | | | | | | | | | | | | | xxxx |
| ACCAH | 0024 | Accumulator A High Word Register | | | | | | | | | | | | | | | | xxxx |
| ACCAU | 0026 | Accumulator A Upper Word Register | | | | | | | | | | | | | | | | xxxx |
| ACCBL | 0028 | Accumulator B Low Word Register | | | | | | | | | | | | | | | | xxxx |
| ACCBH | 002A | Accumulator B High Word Register | | | | | | | | | | | | | | | | xxxx |
| ACCBU | 002C | Accumulator B Upper Word Register | | | | | | | | | | | | | | | | xxxx |
| PCL | 002E | Program Counter Low Word Register | | | | | | | | | | | | | | | | 0000 |
| PCH | 0030 | — | — | — | — | — | — | — | — | Program Counter High Byte Register | | | | | | | | 0000 |
| TBLPAG | 0032 | — | — | — | — | — | — | — | — | Table Page Address Pointer Register | | | | | | | | 0000 |
| PSVPAG | 0034 | — | — | — | — | — | — | — | — | Program Memory Visibility Page Address Pointer Register | | | | | | | | 0000 |
| RCOUNT | 0036 | Repeat Loop Counter Register | | | | | | | | | | | | | | | | xxxx |
| DCOUNT | 0038 | DCOUNT<15:0> | | | | | | | | | | | | | | | | xxxx |
| DOSTARTL | 003A | DOSTARTL<15:1> | | | | | | | | | | | | | | | 0 | xxxx |
| DOSTARTH | 003C | — | — | — | — | — | — | — | — | — | — | DOSTARTH<5:0> | | | | | | 00xx |
| DOENDL | 003E | DOENDL<15:1> | | | | | | | | | | | | | | | 0 | xxxx |
| DOENDH | 0040 | — | — | — | — | — | — | — | — | — | — | DOENDH | | | | | | 00xx |
| SR | 0042 | OA | OB | SA | SB | OAB | SAB | DA | DC | IPL2 | IPL1 | IPL0 | RA | N | OV | Z | C | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.



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**TABLE 4-17: ADC1 REGISTER MAP FOR dsPIC33FJ32(GP/MC)104 DEVICES**

| File Name | SFR Addr | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ADC1BUF0 | 0300 | ADC1 Data Buffer 0 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUF1 | 0302 | ADC1 Data Buffer 1 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUF2 | 0304 | ADC1 Data Buffer 2 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUF3 | 0306 | ADC1 Data Buffer 3 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUF4 | 0308 | ADC1 Data Buffer 4 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUF5 | 030A | ADC1 Data Buffer 5 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUF6 | 030C | ADC1 Data Buffer 6 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUF7 | 030E | ADC1 Data Buffer 7 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUF8 | 0310 | ADC1 Data Buffer 8 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUF9 | 0312 | ADC1 Data Buffer 9 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUFA | 0314 | ADC1 Data Buffer 10 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUFB | 0316 | ADC1 Data Buffer 11 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUFC | 0318 | ADC1 Data Buffer 12 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUFD | 031A | ADC1 Data Buffer 13 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUFE | 031C | ADC1 Data Buffer 14 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUFF | 031E | ADC1 Data Buffer 15 | | | | | | | | | | | | | | | | xxxx |
| AD1CON1 | 0320 | ADON | — | ADSIDL | — | — | — | FORM1 | FORM0 | SSRC2 | SSRC1 | SSRC0 | — | SIMSAM | ASAM | SAMP | DONE | 0000 |
| AD1CON2 | 0322 | VCFG2 | VCFG1 | VCFG0 | — | — | CSCNA | CHPS1 | CHPS0 | BUFS | — | SMPI3 | SMPI2 | SMPI1 | SMPI0 | BUFM | ALTS | 0000 |
| AD1CON3 | 0324 | ADRC | — | — | SAMC4 | SAMC3 | SAMC2 | SAMC1 | SAMC0 | ADCS7 | ADCS6 | ADCS5 | ADCS4 | ADCS3 | ADCS2 | ADCS1 | ADCS0 | 0000 |
| AD1CHS123 | 0326 | — | — | — | — | — | CH123NB1 | CH123NB0 | CH123SB | — | — | — | — | — | CH123NA1 | CH123NA0 | CH123SA | 0000 |
| AD1CHS0 | 0328 | CH0NB | — | — | CH0SB4 | CH0SB3 | CH0SB2 | CH0SB1 | CH0SB0 | CH0NA | — | — | CH0SA4 | CH0SA3 | CH0SA2 | CH0SA1 | CH0SA0 | 0000 |
| AD1PCFGL | 032C | PCFG15 | — | — | PCFG<12:0>(1) | | | | | | | | | | | | | 0000 |
| AD1CSSL | 0330 | CSS15 | — | — | CSS12:0>(1) | | | | | | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** The PCFG<10:9> and CSS<10:9> bits are available in dsPIC33FJ32(GP/MC)104 devices only.

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**REGISTER 6-1: RCON: RESET CONTROL REGISTER(1) (CONTINUED)**

bit 2 **IDLE:** Wake-up from Idle Flag bit
1 = Device has been in Idle mode
0 = Device has not been in Idle mode

bit 1 **BOR:** Brown-out Reset Flag bit
1 = A Brown-out Reset has occurred
0 = A Brown-out Reset has not occurred

bit 0 **POR:** Power-on Reset Flag bit
1 = A Power-on Reset has occurred
0 = A Power-on Reset has not occurred

**Note 1:** All of the Reset status bits can be set or cleared in software. Setting one of these bits in software does not cause a device Reset.

**2:** If the FWDTEN Configuration bit is set to '1' (unprogrammed), the WDT is always enabled, regardless of the SWDTEN bit setting.

**TABLE 7-1: INTERRUPT VECTORS**

| Vector Number | Interrupt Request (IRQ) Number | IVT Address | AIVT Address | Interrupt Source |
|---|---|---|---|---|
| 8 | 0 | 0x000014 | 0x000114 | INT0 – External Interrupt 0 |
| 9 | 1 | 0x000016 | 0x000116 | IC1 – Input Capture 1 |
| 10 | 2 | 0x000018 | 0x000118 | OC1 – Output Compare 1 |
| 11 | 3 | 0x00001A | 0x00011A | T1 – Timer1 |
| 12 | 4 | 0x00001C | 0x00011C | Reserved |
| 13 | 5 | 0x00001E | 0x00011E | IC2 – Input Capture 2 |
| 14 | 6 | 0x000020 | 0x000120 | OC2 – Output Compare 2 |
| 15 | 7 | 0x000022 | 0x000122 | T2 – Timer2 |
| 16 | 8 | 0x000024 | 0x000124 | T3 – Timer3 |
| 17 | 9 | 0x000026 | 0x000126 | SPI1E – SPI1 Error |
| 18 | 10 | 0x000028 | 0x000128 | SPI1 – SPI1 Transfer Done |
| 19 | 11 | 0x00002A | 0x00012A | U1RX – UART1 Receiver |
| 20 | 12 | 0x00002C | 0x00012C | U1TX – UART1 Transmitter |
| 21 | 13 | 0x00002E | 0x00012E | ADC1 – ADC1 |
| 22-23 | 14-15 | 0x000030-0x000032 | 0x000130-0x000132 | Reserved |
| 24 | 16 | 0x000034 | 0x000134 | SI2C1 – I2C1 Slave Events |
| 25 | 17 | 0x000036 | 0x000136 | MI2C1 – I2C1 Master Events |
| 26 | 18 | 0x000038 | 0x000138 | CMP – Comparator Interrupt |
| 27 | 19 | 0x00003A | 0x00013A | Change Notification Interrupt |
| 28 | 20 | 0x00003C | 0x00013C | INT1 – External Interrupt 1 |
| 29-34 | 21-26 | 0x00003E-0x000038 | 0x00013E-0x000138 | Reserved |
| 35 | 27 | 0x00004A | 0x00014A | T4 – Timer4(2) |
| 36 | 28 | 0x00004C | 0x00014C | T5 – Timer5(2) |
| 37 | 29 | 0x00004E | 0x00014E | INT2 – External Interrupt 2 |
| 38-44 | 30-36 | 0x000050-0x00005C | 0x000150-0x00015C | Reserved |
| 45 | 37 | 0x00005E | 0x00015E | IC3 – Input Capture 3 |
| 46-64 | 38-56 | 0x000060-0x000084 | 0x000160-0x000184 | Reserved |
| 65 | 57 | 0x000086 | 0x000186 | PWM1 – PWM1 Period Match(1) |
| 66-69 | 58-61 | 0x000088-0x00008E | 0x000188-0x00018E | Reserved |
| 70 | 62 | 0x000090 | 0x000190 | RTCC – Real-Time Clock and Calendar |
| 71 | 63 | 0x000092 | 0x000192 | $\overline{\text{FLTA1}}$ – PWM1 Fault A(1) |
| 72 | 64 | 0x000094 | 0x000194 | $\overline{\text{FLTB1}}$ – PWM1 Fault B(3) |
| 73 | 65 | 0x000096 | 0x000196 | U1E – UART1 Error |
| 74-84 | 66-76 | 0x000098-0x0000AC | 0x000198-0x0001AC | Reserved |
| 85 | 77 | 0x0000AE | 0x0001AE | CTMU – Charge Time Measurement Unit |
| 86-125 | 78-117 | 0x0000B0-0x0000FE | 0x0001B0-0x0001FE | Reserved |

**Note 1:** This interrupt vector is available in dsPIC33FJ(16/32)MC10X devices only.

**2:** This interrupt vector is available in dsPIC33FJ32(GP/MC)10X devices only.

**3:** This interrupt vector is available in dsPIC33FJ(16/32)MC102/104 devices only.

**REGISTER 10-7: RPINR11: PERIPHERAL PIN SELECT INPUT REGISTER 11**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
|---|---|---|---|---|---|---|---|
| — | — | — | OCFAR4 | OCFAR3 | OCFAR2 | OCFAR1 | OCFAR0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-5 **Unimplemented:** Read as ‘0’

bit 4-0 **OCFAR<4:0>:** Assign Output Capture A (OCFA) to the Corresponding RPn Pin bits

11111 = Input tied to Vss
11110 = Reserved
.
.
.
11010 = Reserved
11001 = Input tied to RP25
.
.
.
00001 = Input tied to RP1
00000 = Input tied to RP0

**REGISTER 10-11: RPOR0: PERIPHERAL PIN SELECT OUTPUT REGISTER 0**

| U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | RP1R<4:0> | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | RP0R<4:0> | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-13 **Unimplemented:** Read as ‘0’

bit 12-8 **RP1R<4:0>:** Peripheral Output Function is Assigned to RP1 Output Pin bits
(see Table 10-2 for peripheral function numbers)

bit 7-5 **Unimplemented:** Read as ‘0’

bit 4-0 **RP0R<4:0>:** Peripheral Output Function is Assigned to RP0 Output Pin bits
(see Table 10-2 for peripheral function numbers)

**REGISTER 10-12: RPOR1: PERIPHERAL PIN SELECT OUTPUT REGISTER 1**

| U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | RP3R<4:0>(1) | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | RP2R<4:0>(1) | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-13 **Unimplemented:** Read as ‘0’

bit 12-8 **RP3R<4:0>:** Peripheral Output Function is Assigned to RP3 Output Pin bits(1)
(see Table 10-2 for peripheral function numbers)

bit 7-5 **Unimplemented:** Read as ‘0’

bit 4-0 **RP2R<4:0>:** Peripheral Output Function is Assigned to RP2 Output Pin bits(1)
(see Table 10-2 for peripheral function numbers)

**Note 1:** These bits are not available in dsPIC33FJXX(GP/MC)101 devices.

## 11.1 Timer1 Control Register

**REGISTER 11-1: T1CON: TIMER1 CONTROL REGISTER**

| R/W-0 | U-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| TON(1) | — | TSIDL | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | TGATE | TCKPS1 | TCKPS0 | — | TSYNC | TCS(1) | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **TON:** Timer1 On bit(1)
1 = Starts 16-bit Timer1
0 = Stops 16-bit Timer1

bit 14 **Unimplemented:** Read as '0'

bit 13 **TSIDL:** Timer1 Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12-7 **Unimplemented:** Read as '0'

bit 6 **TGATE:** Timer1 Gated Time Accumulation Enable bit
When TCS = 1:
This bit is ignored.
When TCS = 0:
1 = Gated time accumulation is enabled
0 = Gated time accumulation is disabled

bit 5-4 **TCKPS<1:0>** Timer1 Input Clock Prescale Select bits
11 = 1:256
10 = 1:64
01 = 1:8
00 = 1:1

bit 3 **Unimplemented:** Read as '0'

bit 2 **TSYNC:** Timer1 External Clock Input Synchronization Select bit
When TCS = 1:
1 = Synchronizes external clock input
0 = Does not synchronize external clock input
When TCS = 0:
This bit is ignored.

bit 1 **TCS:** Timer1 Clock Source Select bit(1)
1 = External clock from pin, T1CK (on the rising edge)
0 = Internal clock (FCY)

bit 0 **Unimplemented:** Read as '0'

**Note 1:** When TCS = 1 and TON = 1, writes to the TMR1 register are inhibited from the CPU.


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**NOTES:**


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**REGISTER 15-4: PxSECMP: PWMx SPECIAL EVENT COMPARE REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| SEVTDIR(1) | SEVTCMP<14:8>(2) | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| SEVTCMP<7:0>(2) | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15 **SEVTDIR:** Special Event Trigger Time Base Direction bit(1)
1 = A Special Event Trigger will occur when the PWMx time base is counting down
0 = A Special Event Trigger will occur when the PWMx time base is counting up

bit 14-0 **SEVTCMP<14:0>:** Special Event Compare Value bits(2)

**Note 1:** SEVTDIR is compared with PTDIR (PxTMR<15>) to generate the Special Event Trigger.
**2:** PxSECMP<14:0> is compared with PxTMR<14:0> to generate the Special Event Trigger.

**REGISTER 15-8: PxDTCON2: PWMx DEAD-TIME CONTROL REGISTER 2**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | DTS3A | DTS3I | DTS2A | DTS2I | DTS1A | DTS1I |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-6 **Unimplemented:** Read as ‘0’

bit 5 **DTS3A:** Dead-Time Select for PWM3 Signal Going Active bit
1 = Dead time provided from Unit B
0 = Dead time provided from Unit A

bit 4 **DTS3I:** Dead-Time Select for PWM3 Signal Going Inactive bit
1 = Dead time provided from Unit B
0 = Dead time provided from Unit A

bit 3 **DTS2A:** Dead-Time Select for PWM2 Signal Going Active bit
1 = Dead time provided from Unit B
0 = Dead time provided from Unit A

bit 2 **DTS2I:** Dead-Time Select for PWM2 Signal Going Inactive bit
1 = Dead time provided from Unit B
0 = Dead time provided from Unit A

bit 1 **DTS1A:** Dead-Time Select for PWM1 Signal Going Active bit
1 = Dead time provided from Unit B
0 = Dead time provided from Unit A

bit 0 **DTS1I:** Dead-Time Select for PWM1 Signal Going Inactive bit
1 = Dead time provided from Unit B
0 = Dead time provided from Unit A

## 18.1 UART Helpful Tips

1. In multi-node, direct connect UART networks, UART receive inputs react to the complementary logic level defined by the URXINV bit (UxMODE<4>), which defines the Idle state, the default of which is logic high (i.e., URXINV = 0). Because remote devices do not initialize at the same time, it is likely that one of the devices, because the RX line is floating, will trigger a Start bit detection and will cause the first byte received after the device has been initialized to be invalid. To avoid this situation, the user should use a pull-up or pull-down resistor on the RX pin depending on the value of the URXINV bit.
   a) If URXINV = 0, use a pull-up resistor on the RX pin.
   b) If URXINV = 1, use a pull-down resistor on the RX pin.
2. The first character received on a wake-up from Sleep mode caused by activity on the UxRX pin of the UART module will be invalid. In Sleep mode, peripheral clocks are disabled. By the time the oscillator system has restarted and stabilized from Sleep mode, the baud rate bit sampling clock, relative to the incoming UxRX bit timing, is no longer synchronized, resulting in the first character being invalid; this is to be expected.

## 18.2 UART Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

| | |
|---|---|
| **Note:** | In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en554109 |

### 18.2.1 KEY RESOURCES

- **"UART"** (DS70188) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related *"dsPIC33/PIC24 Family Reference Manual"* sections
- Development Tools


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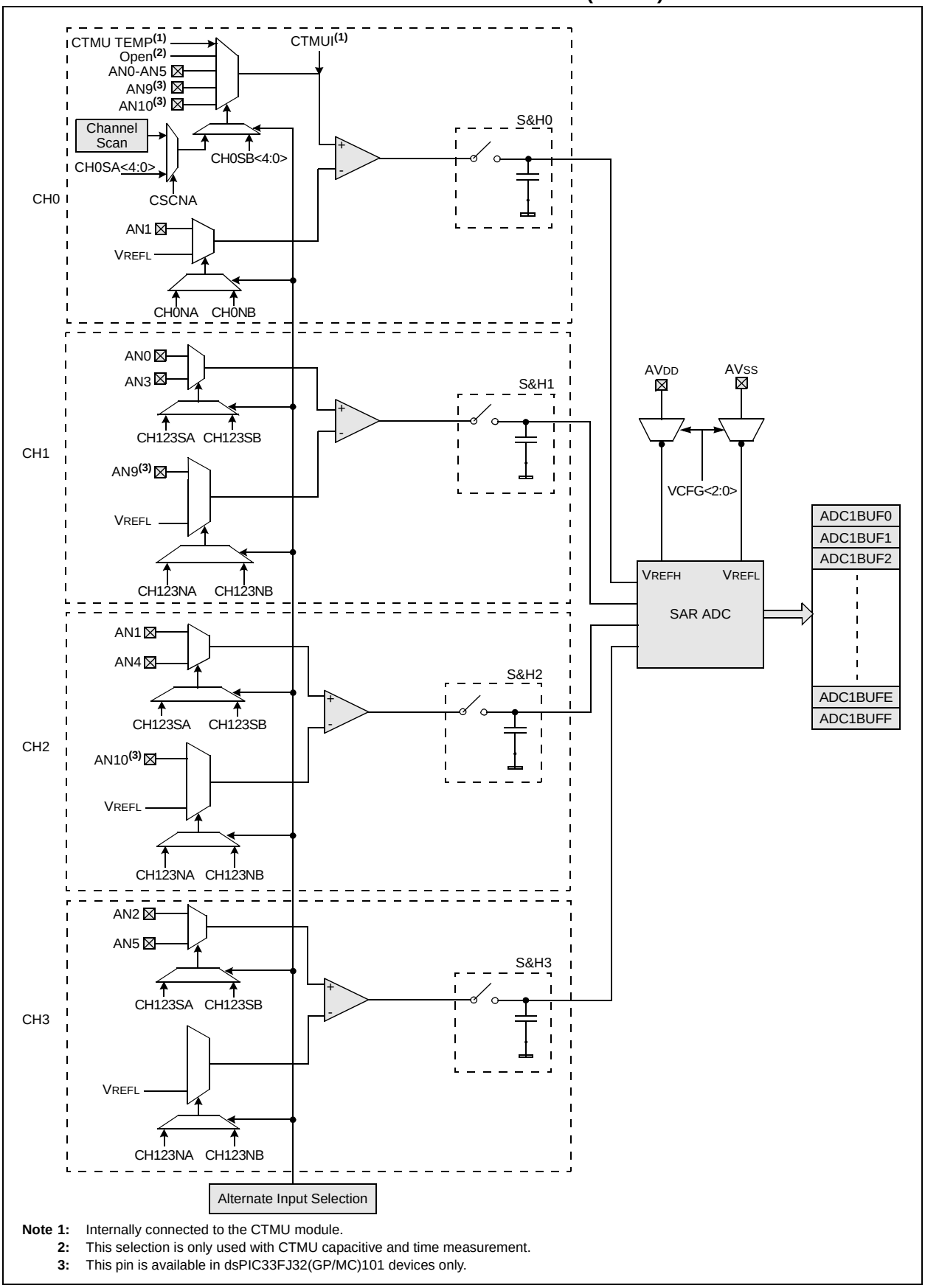
**FIGURE 19-2: ADC1 BLOCK DIAGRAM FOR dsPIC33FJXX(GP/MC)102 DEVICES**




**Note 1:** Internally connected to the CTMU module.
**2:** This selection is only used with CTMU capacitive and time measurement.
**3:** This pin is available in dsPIC33FJ32(GP/MC)101 devices only.

**REGISTER 20-3: CMxMSKSRC: COMPARATOR x MASK SOURCE SELECT REGISTER (CONTINUED)**

bit 3-0 **SELSRCA<3:0>:** Mask A Input Select bits

1111 = Reserved
1110 = Reserved
1101 = Reserved
1100 = Reserved
1011 = Reserved
1010 = Reserved
1001 = Reserved
1000 = Reserved
0111 = Reserved
0110 = Reserved
0101 = PWM1H3
0100 = PWM1L3
0011 = PWM1H2
0010 = PWM1L2
0001 = PWM1H1
0000 = PWM1L1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## 21.2 RTCC Control Registers

**REGISTER 21-1: RCFGCAL: RTCC CALIBRATION AND CONFIGURATION REGISTER(1)**

| R/W-0 | U-0 | R/W-0 | R-0 | R-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| RTCEN(2) | — | RTCWREN | RTCSYNC | HALFSEC(3) | RTCOE | RTCPTR1 | RTCPTR0 |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| CAL7 | CAL6 | CAL5 | CAL4 | CAL3 | CAL2 | CAL1 | CAL0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **RTCEN:** RTCC Enable bit(2)
1 = RTCC module is enabled
0 = RTCC module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **RTCWREN:** RTCC Value Registers Write Enable bit
1 = RTCVALH and RTCVALL registers can be written to by the user
0 = RTCVALH and RTCVALL registers are locked out from being written to by the user

bit 12 **RTCSYNC:** RTCC Value Registers Read Synchronization bit
1 = RTCVALH, RTCVALL and ALCFGRPT registers can change while reading, due to a rollover ripple, resulting in an invalid data read. If the register is read twice and the results are the same data, the data can be assumed to be valid.
0 = RTCVALH, RTCVALL or ALCFGRPT registers can be read without concern over a rollover ripple

bit 11 **HALFSEC:** Half-Second Status bit(3)
1 = Second half period of a second
0 = First half period of a second

bit 10 **RTCOE:** RTCC Output Enable bit
1 = RTCC output is enabled
0 = RTCC output is disabled

bit 9-8 **RTCPTR<1:0>:** RTCC Value Register Window Pointer bits
Points to the corresponding RTCC Value registers when reading RTCVALH and RTCVALL registers; the RTCPTR<1:0> value decrements on every read or write of RTCVALH until it reaches '00'.
RTCVAL<15:8>:
00 = MINUTES
01 = WEEKDAY
10 = MONTH
11 = Reserved
RTCVAL<7:0>:
00 = SECONDS
01 = HOURS
10 = DAY
11 = YEAR

**Note 1:** The RCFGCAL register is only affected by a POR.
**2:** A write to the RTCEN bit is only allowed when RTCWREN = 1.
**3:** This bit is read-only; it is cleared to '0' on a write to the lower half of the MINSEC register.

**REGISTER 21-6: RTCVAL (WHEN RTCPTR<1:0> = 01): RTCC WEEKDAY AND HOURS VALUE REGISTER(1)**

| U-0 | U-0 | U-0 | U-0 | U-0 | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | WDAY2 | WDAY1 | WDAY0 |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| — | — | HRTEN1 | HRTEN0 | HRONE3 | HRONE2 | HRONE1 | HRONE0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-11 **Unimplemented:** Read as '0'

bit 10-8 **WDAY<2:0>:** Binary Coded Decimal Value of Weekday Digit bits
Contains a value from 0 to 6.

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **HRTEN<1:0>:** Binary Coded Decimal Value of Hour's Tens Digit bits
Contains a value from 0 to 2.

bit 3-0 **HRONE<3:0>:** Binary Coded Decimal Value of Hour's Ones Digit bits
Contains a value from 0 to 9.

**Note 1:** A write to this register is only allowed when RTCWREN = 1.


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**REGISTER 23-1: DEVID: DEVICE ID REGISTER**

| R | R | R | R | R | R | R | R |
|---|---|---|---|---|---|---|---|
| DEVID<23:16>(1) | | | | | | | |
| bit 23 | | | | | | | bit 16 |

| R | R | R | R | R | R | R | R |
|---|---|---|---|---|---|---|---|
| DEVID<15:8>(1) | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R | R | R | R | R | R | R | R |
|---|---|---|---|---|---|---|---|
| DEVID<7:0>(1) | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | R = Read-Only bit | U = Unimplemented bit |
|---|---|---|

bit 23-0 **DEIDV<23:0>:** Device Identifier bits(1)

**Note 1:** Refer to the *"dsPIC33F Flash Programming Specification for Devices with Volatile Configuration Bits"* (DS70659) for the list of device ID values.

**REGISTER 23-2: DEVREV: DEVICE REVISION REGISTER**

| R | R | R | R | R | R | R | R |
|---|---|---|---|---|---|---|---|
| DEVREV<23:16>(1) | | | | | | | |
| bit 23 | | | | | | | bit 16 |

| R | R | R | R | R | R | R | R |
|---|---|---|---|---|---|---|---|
| DEVREV<15:8>(1) | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R | R | R | R | R | R | R | R |
|---|---|---|---|---|---|---|---|
| DEVREV<7:0>(1) | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | R = Read-only bit | U = Unimplemented bit |
|---|---|---|

bit 23-0 **DEVREV<23:0>:** Device Revision bits(1)

**Note 1:** Refer to the *"dsPIC33F Flash Programming Specification for Devices with Volatile Configuration Bits"* (DS70659) for the list of device revision values.

**TABLE 26-6: DC CHARACTERISTICS: OPERATING CURRENT (IDD)**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | |
|---|---|---|---|---|---|---|
| **Parameter No.** | **Typical(1)** | **Max** | **Units** | **Conditions** | | |
| **Operating Current (IDD)(2) – dsPIC33FJ16(GP/MC)10X Devices** | | | | | | |
| DC20d | 0.7 | 1.7 | mA | -40°C | 3.3V | LPRC (32.768 kHz)(3) |
| DC20a | 0.7 | 1.7 | mA | +25°C | | |
| DC20b | 1.0 | 1.7 | mA | +85°C | | |
| DC20c | 1.3 | 1.7 | mA | +125°C | | |
| DC21d | 1.9 | 2.6 | mA | -40°C | 3.3V | 1 MIPS(3) |
| DC21a | 1.9 | 2.6 | mA | +25°C | | |
| DC21b | 1.9 | 2.6 | mA | +85°C | | |
| DC21c | 2.0 | 2.6 | mA | +125°C | | |
| DC22d | 6.5 | 8.5 | mA | -40°C | 3.3V | 4 MIPS(3) |
| DC22a | 6.5 | 8.5 | mA | +25°C | | |
| DC22b | 6.5 | 8.5 | mA | +85°C | | |
| DC22c | 6.5 | 8.5 | mA | +125°C | | |
| DC23d | 12.2 | 16 | mA | -40°C | 3.3V | 10 MIPS(3) |
| DC23a | 12.2 | 16 | mA | +25°C | | |
| DC23b | 12.2 | 16 | mA | +85°C | | |
| DC23c | 12.2 | 16 | mA | +125°C | | |
| DC24d | 16 | 21 | mA | -40°C | 3.3V | 16 MIPS |
| DC24a | 16 | 21 | mA | +25°C | | |
| DC24b | 16 | 21 | mA | +85°C | | |
| DC24c | 16 | 21 | mA | +125°C | | |

**Note 1:** Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

**2:** IDD is primarily a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. The test conditions for all IDD measurements are as follows:

- Oscillator is configured in EC mode, OSC1 is driven with external square wave from rail-to-rail
- CLKO is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{MCLR}$ = VDD, WDT and FSCM are disabled
- CPU, SRAM, program memory and data memory are operational
- No peripheral modules are operating; however, every peripheral is being clocked (PMDx bits are all zeroed)
- CPU executing `while(1)` statement

**3:** These parameters are characterized, but not tested in manufacturing.


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**TABLE 26-17: PLL CLOCK TIMING SPECIFICATIONS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ(1)** | **Max** | **Units** | **Conditions** |
| OS50 | FPLLI | PLL Voltage Controlled Oscillator (VCO) Input Frequency Range(2) | 3.0 | — | 8 | MHz | ECPLL and MSPLL modes |
| OS51 | FSYS | On-Chip VCO System Frequency(3) | 12 | — | 32 | MHz | |
| OS52 | TLOCK | PLL Start-up Time (Lock Time)(3) | — | — | 2 | mS | |
| OS53 | DCLK | CLKO Stability (Jitter)(3) | -2 | 1 | +2 | % | |

**Note 1:** Data in "Typ" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**2:** These parameters are characterized by similarity, but are tested in manufacturing at 7.7 MHz input only.

**3:** These parameters are characterized by similarity, but are not tested in manufacturing. This specification is based on clock cycle by clock cycle measurements. The effective jitter for individual time bases, or communication clocks used by the user application, are derived from dividing the CLKO stability specification by the square root of "N" (where "N" is equal to FOSC, divided by the peripheral data rate clock). For example, if FOSC = 32 MHz and the SPI bit rate is 5 MHz, the effective jitter of the SPI clock is equal to:

$$\frac{DCLK}{\sqrt{\frac{32}{5}}} = \frac{2\%}{2.53} = 0.79\%$$

**TABLE 26-18: AC CHARACTERISTICS: INTERNAL FAST RC (FRC) ACCURACY**

| AC CHARACTERISTICS | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Characteristic** | **Min** | **Typ** | **Max** | **Units** | **Conditions** | |
| | **Internal FRC Accuracy @ 7.37 MHz(1)** | | | | | | |
| F20a | FRC | -2 | ±0.25 | +2 | % | -40°C ≤ TA ≤ -10°C | VDD 3.0-3.6V |
| F20b | FRC | -1 | ±0.25 | +1 | % | -10°C ≤ TA ≤ +85°C | VDD 3.0-3.6V |
| F20c | FRC | -5 | ±0.25 | +5 | % | +85°C ≤ TA ≤ +125°C | VDD 3.0-3.6V |

**Note 1:** Frequency is calibrated at +25°C and 3.3V. TUNx bits may be used to compensate for temperature drift.

**TABLE 26-19: INTERNAL LOW-POWER RC (LPRC) ACCURACY**

| AC CHARACTERISTICS | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Characteristic** | **Min** | **Typ** | **Max** | **Units** | **Conditions** | |
| | **LPRC @ 32.768 kHz(1,2)** | | | | | | |
| F21a | LPRC | -30 | ±10 | +20 | % | -40°C ≤ TA ≤ -10°C | VDD 3.0-3.6V |
| F21b | LPRC | -20 | ±10 | +30 | % | -10°C ≤ TA ≤ +85°C | VDD 3.0-3.6V |
| F21c | LPRC | -35 | ±10 | +35 | % | +85°C ≤ TA ≤ +125°C | VDD 3.0-3.6V |

**Note 1:** Change of LPRC frequency as VDD changes.

**2:** LPRC accuracy impacts the Watchdog Timer Time-out Period (TWDT1). See **Section 23.4 "Watchdog Timer (WDT)"** for more information.


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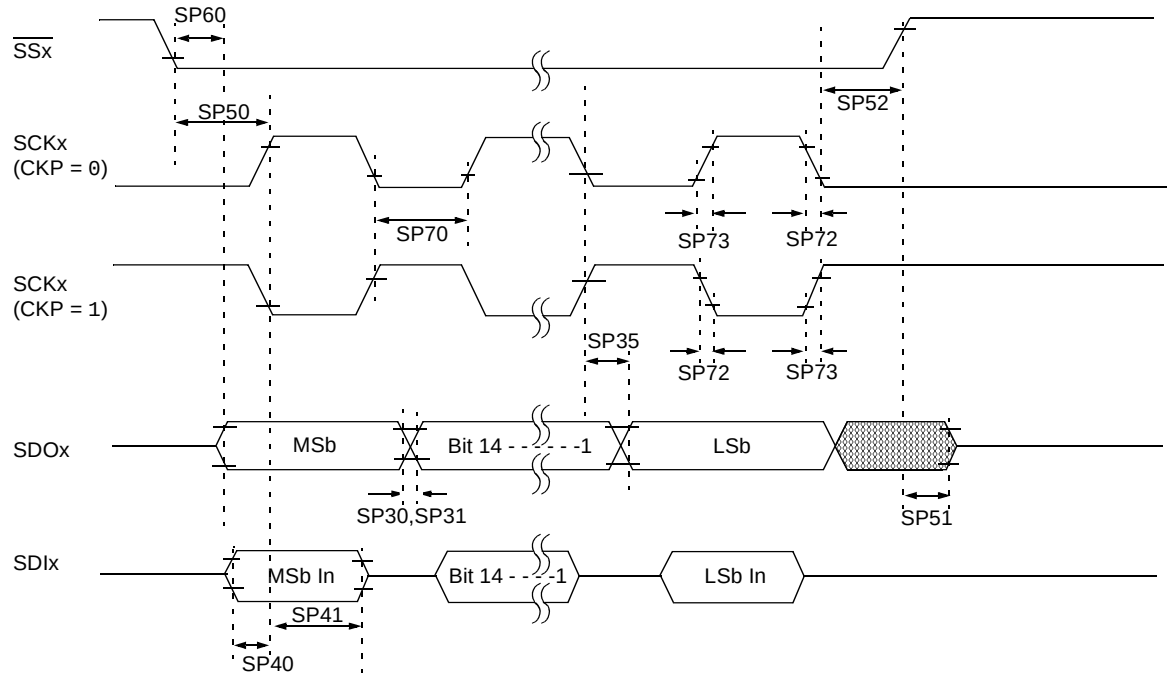
**FIGURE 26-23: SPIx SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0) TIMING CHARACTERISTICS FOR dsPIC33FJ32(GP/MC)10X**




**Note:** Refer to Figure 26-1 for load conditions.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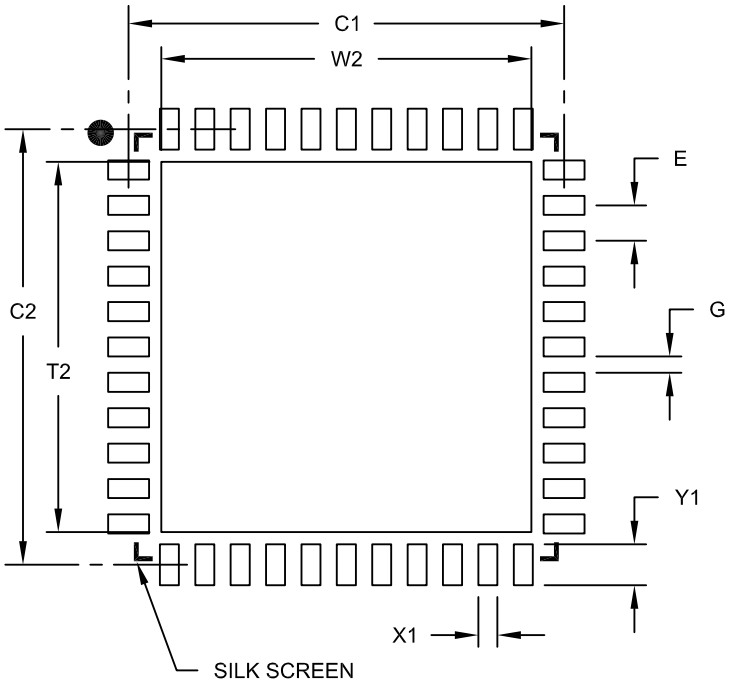
### 44-Lead Plastic Quad Flat, No Lead Package (ML) – 8x8 mm Body [QFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.65 BSC | |
| Optional Center Pad Width | W2 | | | 6.80 |
| Optional Center Pad Length | T2 | | | 6.80 |
| Contact Pad Spacing | C1 | | 8.00 | |
| Contact Pad Spacing | C2 | | 8.00 | |
| Contact Pad Width (X44) | X1 | | | 0.35 |
| Contact Pad Length (X44) | Y1 | | | 0.80 |
| Distance Between Pads | G | 0.25 | | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2103A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