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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	16 MIPs
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, Motor Control PWM, POR, PWM, WDT
Number of I/O	35
Program Memory Size	32KB (11K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 14x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj32mc104t-i-pt

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Pin Diagrams (Continued)



Referenced Sources

This device data sheet is based on the following individual chapters of the *"dsPIC33/PIC24 Family Reference Manual"*. These documents should be considered as the primary reference for the operation of a particular module or device feature.

Note 1: To access the documents listed below, browse to the documentation section of the dsPIC33FJ16MC102 product page of the Microchip Web site (www.microchip.com). In addition to parameters, features and other documentation, the resulting page provides links to the related family reference manual sections.

- "CPU" (DS70204)
- "Data Memory" (DS70202)
- "Program Memory" (DS70203)
- "Flash Programming" (DS70191)
- "Reset" (DS70192)
- "Watchdog Timer and Power-Saving Modes" (DS70196)
- "Timers" (DS70205)
- "Input Capture" (DS70198)
- "Output Compare" (DS70209)
- "Motor Control PWM" (DS70187)
- "Analog-to-Digital Converter (ADC)" (DS70183)
- "UART" (DS70188)
- "Serial Peripheral Interface (SPI)" (DS70206)
- "Inter-Integrated Circuit™ (I²C™)" (DS70195)
- "CodeGuard Security" (DS70199)
- "Programming and Diagnostics" (DS70207)
- "Device Configuration" (DS70194)
- "I/O Ports with Peripheral Pin Select (PPS)" (DS70190)
- "Real-Time Clock and Calendar (RTCC)" (DS70301)
- "Introduction (Part VI)" (DS70655)
- "Oscillator (Part VI)" (DS70644)
- "Interrupts (Part VI)" (DS70633)
- "Comparator with Blanking" (DS70647)
- "Charge Time Measurement Unit (CTMU)" (DS70635)

TABLE	4-7:	TIME	RS REC	GISTER	MAP F	OR dsPl	IC33FJ1	6(GP/M	C)10X [DEVICE	S							
SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TMR1	0100		Timer1 Register 00									0000						
PR1	0102								Period F	Register 1								FFFF
T1CON	0104	TON	—	TSIDL	—	_	_	_	_	—	TGATE	TCKPS1	TCKPS0	_	TSYNC	TCS	—	0000
TMR2	0106								Timer2	Register								0000
TMR3HLD	0108		Timer3 Holding Register (for 32-bit timer operations only)								xxxx							
TMR3	010A								Timer3	Register								0000
PR2	010C								Period F	Register 2								FFFF
PR3	010E								Period F	Register 3								FFFF
T2CON	0110	TON	_	TSIDL	—	_	_	—		—	TGATE	TCKPS1	TCKPS0	T32	—	TCS	—	0000
T3CON	0112	TON	_	TSIDL	—	_	_	_	_	_	TGATE	TCKPS1	TCKPS0	_	_	TCS	_	0000
	4-8:	TIME Bit 15	Bit 14	Bit 13	MAP FO	OR DSP Bit 11	IC33FJ	32(GP/N Bit 9	IC)10X	DEVICE Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All
Name	Addr											l						Resets
IMR1	0100								Limer1	Register								0000
PR1	0102	TON		TOIDI					Period F	Register 1	TOATE	TOKDOA	TOKDOO		TOVALO	TOO		FFFF
TICON	0104	TON	_	TSIDL							IGAIE	TCKPS1	TCKP50	_	ISTNC	105	_	0000
	0106						T :	a vO I I a lalia a	Timer2	Register								0000
TMR3HLD	0108						IIm	er3 Holding	Register (fo	Desister	er operations	oniy)						XXXX
	010A								Doriod [Register 2								0000
	0100								Period	Cegister 2								FFFF
T2CON	0110	TON	_	TSIDI	_			_			TGATE	TCKPS1	TCKPS0	T32	_	TCS	_	0000
T3CON	0112	TON		TSIDI							TGATE	TCKPS1	TCKPS0		_	TCS	_	0000
TMR4	0114	TON		TOIDE					Timer4	Register	10/112		1014 00			100		0000
TMR5HLD	0116						Г	Timer5 Holdi	na Register	(for 32-bit o	perations or	lv)						****
TMR5	0118								Timer5	Register		<i>(</i> t ¹)						0000
PR4	011A								Period F	Register 4								FFFF
PR5	011C								Period F	Register 5								FFFF
T4CON	011E	TON	_	TSIDL	_	_	_	—	_	_	TGATE	TCKPS1	TCKPS0	T32	_	TCS	_	0000
				TOUDI						1			TOUDOO	-		TOO		
T5CON	0120	TON	—	ISIDL	—	—	—		—		TGATE	TCKPS1	TCKPS0	—		ICS	—	0000

.

Legend: x = unknown value on Reset, --- = unimplemented, read as '0'. Reset values are shown in hexadecimal.

5.2 RTSP Operation

The dsPIC33FJ16(GP/MC)101/102 and dsPIC33FJ32(GP/MC)101/102/104 Flash program memory array is organized into rows of 64 instructions or 192 bytes. RTSP allows the user application to erase a page of memory, which consists of eight rows (512 instructions); and to program one word. Table 26-12 shows typical erase and programming times. The 8-row erase pages are edge-aligned from the beginning of program memory, on boundaries of 1536 bytes.

5.3 Programming Operations

A complete programming sequence is necessary for programming or erasing the internal Flash in RTSP mode. The processor stalls (waits) until the operation is finished.

The programming time depends on the FRC accuracy (see Table 26-18) and the value of the FRC Oscillator Tuning register (see Register 8-3). Use the following formula to calculate the minimum and maximum values for the Word write time and page erase time (see Parameters D138a and D138b, and Parameters D137a and D137b in Table 26-12, respectively).

EQUATION 5-1: PROGRAMMING TIME

 $\frac{T}{7.37 \text{ MHz} \times (FRC \text{ Accuracy})\% \times (FRC \text{ Tuning})\%}$

For example, if the device is operating at +125°C, the FRC accuracy will be $\pm 2\%$. If the TUN<5:0> bits (see Register 8-3) are set to `b000000, the minimum row write time is equal to Equation 5-2.

EQUATION 5-2: MINIMUM ROW WRITE TIME

 $T_{RW} = \frac{355 \ Cycles}{7.37 \ MHz \times (1 + 0.02) \times (1 - 0.00375)} = 47.4 \mu s$

The maximum row write time is equal to Equation 5-3.

EQUATION 5-3: MAXIMUM ROW WRITE TIME

$$T_{RW} = \frac{355 \ Cycles}{7.37 \ MHz \times (1 - 0.02) \times (1 - 0.00375)} = 49.3 \mu s$$

Setting the WR bit (NVMCON<15>) starts the operation and the WR bit is automatically cleared when the operation is finished.

5.3.1 PROGRAMMING ALGORITHM FOR FLASH PROGRAM MEMORY

Programmers can program one word (24 bits) of program Flash memory at a time. To do this, it is necessary to erase the 8-row erase page that contains the desired address of the location the user wants to change.

For protection against accidental operations, the write initiate sequence for NVMKEY must be used to allow any erase or program operation to proceed. After the programming command has been executed, the user application must wait for the programming time until programming is complete. The two instructions following the start of the programming sequence should be NOPS.

Note:	Performing a page erase operation on the							
	last page of program memory will clear the							
	Flash Configuration Words, thereby							
	enabling code protection as a result.							
	Therefore, users should avoid performing							
	page erase operations on the last page of							
	program memory.							

Refer to **"Flash Programming"** (DS70191) in the *"dsPIC33/PIC24 Family Reference Manual"* for details and codes examples on programming using RTSP.

5.4 Control Registers

Two SFRs are used to read and write the program Flash memory: NVMCON and NVMKEY.

The NVMCON register (Register 5-1) controls which blocks are to be erased, which memory type is to be programmed and the start of the programming cycle.

NVMKEY is a write-only register that is used for write protection. To start a programming or erase sequence, the user application must consecutively write 0x55 and 0xAA to the NVMKEY register. Refer to **Section 5.3 "Programming Operations"** for further details.

6.3 POR

A POR circuit ensures the device is reset from poweron. The POR circuit is active until VDD crosses the VPOR threshold and the delay, TPOR, has elapsed. The delay, TPOR, ensures that the internal device bias circuits become stable.

The device supply voltage characteristics must meet the specified starting voltage and rise rate requirements to generate the POR. Refer to **Section 26.0 "Electrical Characteristics"** for details.

The Power-on Reset (POR) status bit in the Reset Control (RCON<0>) register is set to indicate the Power-on Reset.

6.4 BOR and PWRT

The on-chip regulator has a BOR circuit that resets the device when the VDD is too low (VDD < VBOR) for proper device operation. The BOR circuit keeps the device in Reset until VDD crosses the VBOR threshold and the delay, TBOR, has elapsed. The delay, TBOR, ensures the voltage regulator output becomes stable.

The Brown-out Reset (BOR) status bit in the Reset Control (RCON<1>) register is set to indicate the Brown-out Reset.

The device will not run at full speed after a BOR as the VDD should rise to acceptable levels for full-speed operation. The Power-up Timer (PWRT) provides power-up time delay (TPWRT) to ensure that the system power supplies have stabilized at the appropriate levels for full-speed operation before the SYSRST is released.

Refer to **Section 23.0 "Special Features"** for further details.

Figure 6-3 shows the typical brown-out scenarios. The Reset delay (TBOR + TPWRT) is initiated each time VDD rises above the VBOR trip point.



FIGURE 6-3: BROWN-OUT RESET SITUATIONS

U-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0	
	—	CTMUIF	—	—		—	—	
bit 15							bit 8	
U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	
	—	_	—	—		U1EIF	FLTB1IF ⁽¹⁾	
bit 7							bit 0	
Legend:								
R = Readable bit W = Writable bit			U = Unimplemented bit, read as '0'					
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unknown		
bit 15-14	Unimplemen	ted: Read as '	0'					
bit 13	CTMUIF: CTM	MU Interrupt Fla	ag Status bit					
	1 = Interrupt r	request has occ	curred					
	0 = Interrupt r	request has not	occurred					
bit 12-2	Unimplemen	ted: Read as '	0'					
bit 1	U1EIF: UART	1 Error Interru	ot Flag Status	bit				
	1 = Interrupt r	request has occ	curred					
	0 = Interrupt r	request has not	occurred					
bit 0	FLTB1IF: PW	/M1 Fault B Inte	errupt Flag Sta	atus bit ⁽¹⁾				
	1 = Interrupt r	request has occ	curred					
	0 = Interrupt r	request has not	occurred					

REGISTER 7-9: IFS4: INTERRUPT FLAG STATUS REGISTER 4

Note 1: This bit is available in dsPIC(16/32)MC102/104 devices only.

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	_	—			RP5R<4:0> ⁽¹)	
bit 15							bit 8
U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_	_	—			RP4R<4:0>		
bit 7	·						bit 0
Legend:							
R = Readable bit W = Writable b			bit	t U = Unimplemented bit, read as '0'			
-n = Value at F	alue at POR '1' = Bit is set '0' = Bit is cleared x = Bit			x = Bit is unkr	nown		

REGISTER 10-13: RPOR2: PERIPHERAL PIN SELECT OUTPUT REGISTER 2

bit 15-13	Unimplemented: Read as '0'
bit 12-8	RP5R<4:0>: Peripheral Output Function is Assigned to RP5 Output Pin bits ⁽¹⁾
	(see Table 10-2 for peripheral function numbers)
bit 7-5	Unimplemented: Read as '0'
bit 4-0	RP4R<4:0>: Peripheral Output Function is Assigned to RP4 Output Pin bits
	(see Table 10-2 for peripheral function numbers)

Note 1: These bits are not available in dsPIC33FJ(16/32)(GP/MC)101 devices.

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
—		—			RP7R<4:0>			
bit 15	•	·					bit 8	
U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
		—	RP6R<4:0> ⁽¹⁾					
bit 7							bit 0	
Legend:								
R = Readable bit W = Writable b			oit	bit U = Unimplemented bit, read as '0'				
-n = Value at POR '1' = Bit is set			'0' = Bit is cleared x = Bit is unknow			nown		
		1 - Dit 18 301						

REGISTER 10-14: RPOR3: PERIPHERAL PIN SELECT OUTPUT REGISTER 3

bit 15-13 Unimplemented: Read as '0'

bit 12-8 **RP7R<4:0>:** Peripheral Output Function is Assigned to RP7 Output Pin bits (see Table 10-2 for peripheral function numbers)

bit 7-5 Unimplemented: Read as '0'

bit 4-0 **RP6R<4:0>:** Peripheral Output Function is Assigned to RP6 Output Pin bits⁽¹⁾ (see Table 10-2 for peripheral function numbers)

Note 1: These bits are not available in dsPIC33FJ(16/32)(GP/MC)101 devices.

11.0 TIMER1

- Note 1: This data sheet summarizes the features of the dsPIC33FJ16(GP/MC)101/102 and dsPIC33FJ32(GP/MC)101/102/104 family devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Timers" (DS70205) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The Timer1 module is a 16-bit timer, which can serve as the time counter for the Real-Time Clock (RTC) or operate as a free-running interval timer/counter. Timer1 can operate in three modes:

- 16-Bit Timer
- 16-Bit Synchronous Counter
- 16-Bit Asynchronous Counter

Timer1 also supports these features:

- Timer gate operation
- · Selectable prescaler settings
- Timer operation during CPU Idle and Sleep modes
- Interrupt on 16-bit Period register match or falling edge of external gate signal

Figure 11-1 presents a block diagram of the 16-bit timer module.

To configure Timer1 for operation:

- 1. Load the timer value into the TMR1 register.
- 2. Load the timer period value into the PR1 register.
- 3. Select the timer prescaler ratio using the TCKPS<1:0> bits in the T1CON register.
- 4. Set the Clock and Gating modes using the TCS and TGATE bits in the T1CON register.
- 5. Set or clear the TSYNC bit in T1CON to select synchronous or asynchronous operation.
- 6. If interrupts are required, set the Timer1 Interrupt Enable bit, T1IE. Use the Timer1 Interrupt Priority bits, T1IP<2:0>, to set the interrupt priority.
- 7. Set the TON bit (= 1) in the T1CON register.



FIGURE 11-1: 16-BIT TIMER1 MODULE BLOCK DIAGRAM

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	POVD3H	POVD3L	POVD2H	POVD2L	POVD1H	POVD1L
bit 15							bit 8
U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	POUT3H	POUT3L	POUT2H	POUT2L	POUT1H	POUT1L
bit 7							bit 0
Legend:							

REGISTER 15-11: PXOVDCON: PWMx OVERRIDE CONTROL REGISTER

bit 15-14 Unimplemented: Read as '0'

R = Readable bit

-n = Value at POR

bit 13-8 POVD<3:1>H:POVD<3:1>L: PWMx Output Override bits

W = Writable bit

'1' = Bit is set

1 = Output on PWMx I/O pin is controlled by the PWMx generator

0 = Output on PWMx I/O pin is controlled by the value in the corresponding POUTxH:POUTxL bits

'0' = Bit is cleared

U = Unimplemented bit, read as '0'

x = Bit is unknown

bit 7-6 Unimplemented: Read as '0'

bit 5-0 POUT<3:1>H:POUT<3:1>L: PWM Manual Output bits

1 = PWMx I/O pin is driven active when the corresponding POVDxH:POVDxL bits are cleared

0 = PWMx I/O pin is driven inactive when the corresponding POVDxH:POVDxL bits are cleared

REGISTER 16-2: SPIXCON1: SPIX CONTROL REGISTER 1 (CONTINUED)

- bit 4-2 SPRE<2:0>: Secondary Prescale bits (Master mode)⁽³⁾
 - 111 = Secondary prescale 1:1
 - 110 = Secondary prescale 2:1
 - . .
 - 000 = Secondary prescale 8:1
- bit 1-0 **PPRE<1:0>:** Primary Prescale bits (Master mode)⁽³⁾
 - 11 = Primary prescale 1:1
 - 10 = Primary prescale 4:1
 - 01 = Primary prescale 16:1
 - 00 = Primary prescale 64:1
- **Note 1:** The CKE bit is not used in the Framed SPI modes. Program this bit to '0' for the Framed SPI modes (FRMEN = 1).
 - 2: This bit must be cleared when FRMEN = 1.
 - **3:** Do not set both primary and secondary prescalers to a value of 1:1.

18.0 UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART)

- Note 1: This data sheet summarizes the features of the dsPIC33FJ16(GP/MC)101/102 and dsPIC33FJ32(GP/MC)101/102/104 family devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "UART" (DS70188) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The Universal Asynchronous Receiver Transmitter (UART) module is one of the serial I/O modules available in the dsPIC33FJ16(GP/MC)101/102 and dsPIC33FJ32(GP/MC)101/102/104 device family. The UART is a full-duplex asynchronous system that can communicate with peripheral devices, such as personal computers, LIN/J2602, RS-232 and RS-485 interfaces. The module also supports a hardware flow control option with the UxCTS and UxRTS pins, and also includes an IrDA[®] encoder and decoder.

The primary features of the UART module are:

- Full-Duplex, 8-Bit or 9-Bit Data Transmission through the UxTX and UxRX Pins
- Even, Odd or No Parity options (for 8-bit data)
- One or Two Stop bits
- Hardware Flow Control Option with UxCTS and UxRTS Pins
- Fully Integrated Baud Rate Generator with 16-Bit Prescaler
- Baud Rates Ranging from 1 Mbps to 6 bps at 16x mode at 16 MIPS
- Baud Rates Ranging from 4 Mbps to 24.4 bps at 4x mode at 16 MIPS
- 4-Deep First-In First-Out (FIFO) Transmit Data Buffer
- 4-Deep FIFO Receive Data Buffer
- Parity, Framing and Buffer Overrun Error Detection
- Support for 9-bit mode with Address Detect (9th bit = 1)
- Transmit and Receive Interrupts
- A Separate Interrupt for all UART Error Conditions
- Loopback mode for Diagnostic Support
- Support for Sync and Break Characters
- Support for Automatic Baud Rate Detection
- IrDA[®] Encoder and Decoder Logic
- 16x Baud Clock Output for IrDA® Support

A simplified block diagram of the UART module is shown in Figure 18-1. The UART module consists of these key hardware elements:

- · Baud Rate Generator
- Asynchronous Transmitter
- Asynchronous Receiver

FIGURE 18-1: UARTX SIMPLIFIED BLOCK DIAGRAM



REGISTER 21-6: RTCVAL (WHEN RTCPTR<1:0> = 01): RTCC WEEKDAY AND HOURS VALUE REGISTER⁽¹⁾

U-0	U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x
—	—	—	—	—	WDAY2	WDAY1	WDAY0
bit 15							bit 8

U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-11 Unimplemented: Read as '0	,
-------------------------------------	---

- bit 10-8 **WDAY<2:0>:** Binary Coded Decimal Value of Weekday Digit bits Contains a value from 0 to 6.
- bit 7-6 Unimplemented: Read as '0'
- bit 5-4 HRTEN<1:0>: Binary Coded Decimal Value of Hour's Tens Digit bits Contains a value from 0 to 2.
- bit 3-0 **HRONE<3:0>:** Binary Coded Decimal Value of Hour's Ones Digit bits Contains a value from 0 to 9.
- **Note 1:** A write to this register is only allowed when RTCWREN = 1.

REGISTER 21-8: ALRMVAL (WHEN ALRMPTR<1:0> = 10): ALARM MONTH AND DAY VALUE REGISTER⁽¹⁾

U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
		—	MTHTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0
bit 15							bit 8

U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	DAYTEN1	DAYTEN0	DAYONE3	DAYONE2	DAYONE1	DAYONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13	Unimplemented: Read as '0'
bit 12	MTHTEN0: Binary Coded Decimal Value of Month's Tens Digit bit
	Contains a value of 0 or 1.
bit 11-8	MTHONE<3:0>: Binary Coded Decimal Value of Month's Ones Digit bits
	Contains a value from 0 to 9.
bit 7-6	Unimplemented: Read as '0'
bit 5-4	DAYTEN<1:0>: Binary Coded Decimal Value of Day's Tens Digit bits
	Contains a value from 0 to 3.
bit 3-0	DAYONE<3:0>: Binary Coded Decimal Value of Day's Ones Digit bits
	Contains a value from 0 to 9.

Note 1: A write to this register is only allowed when RTCWREN = 1.



FIGURE 26-15: SPIX SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0) TIMING CHARACTERISTICS FOR dsPIC33FJ16(GP/MC)10X

TABLE 26-36:SPIX SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0) TIMING
REQUIREMENTS FOR dsPIC33FJ16(GP/MC)10X

AC CHARACTERISTICS			Standard Op (unless othe Operating ter	erating erwise st mperatur	Conditi tated) 'e -40° -40°	ons: 2.4 C ≤ Ta ≤ C ≤ Ta ≤	V to 3.6V +85°C for Industrial +125°C for Extended
Param No.	Symbol	Characteristic ⁽¹⁾	Min	Тур ⁽²⁾	Max	Units	Conditions
SP70	TscP	Maximum SCKx Input Frequency	—	_	11	MHz	See Note 3
SP72	TscF	SCKx Input Fall Time	—			ns	See Parameter DO32 and Note 4
SP73	TscR	SCKx Input Rise Time	—			ns	See Parameter DO31 and Note 4
SP30	TdoF	SDOx Data Output Fall Time	—		_	ns	See Parameter DO32 and Note 4
SP31	TdoR	SDOx Data Output Rise Time	—	_	_	ns	See Parameter DO31 and Note 4
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30		_	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30		_	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30		_	ns	
SP50	TssL2scH, TssL2scL	$\overline{SSx} \downarrow$ to SCKx \uparrow or SCKx Input	120			ns	
SP51	TssH2doZ	SSx ↑ to SDOx Output High-Impedance	10	—	50	ns	See Note 4
SP52	TscH2ssH TscL2ssH	SSx after SCKx Edge	1.5 Tcy + 40	_	_	ns	See Note 4

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCKx is 91 ns. Therefore, the SCKx clock generated by the Master must not violate this specification.

4: Assumes 50 pF load on all SPIx pins.









28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	N	ILLIMETER	S	
Dimension	MIN	NOM	MAX	
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	С		9.40	
Contact Pad Width (X28)	X			0.60
Contact Pad Length (X28)	Y			2.00
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	7.40		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2052A

44-Lead Plastic Thin Quad Flatpack (PT) 10X10X1 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units			S
Dimension Limits		NOM	MAX
E	0.80 BSC		
C1		11.40	
C2		11.40	
X1			0.55
Y1			1.50
G	0.25		
	Units Limits C1 C2 X1 Y1 G	Units MIN E C1 C2 X1 G 0.25	Units MILLIMETER Limits MIN NOM E 0.80 BSC C1 11.40 C2 11.40 X1

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2076B

INDEX

1	١.
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Absolute Maximum Ratings	L
AC Characteristics	1
10-Bit ADC Specifications	3
ADC Specifications	2
Internal Fast RC (FRC) Accuracy	2
Internal Low-Power RC (LPRC) Accuracy 296, 342	2
Load Conditions	1
PLL Clock	3
Temperature and Voltage Specifications	ļ
ADC	
Control Registers 222	2
Helpful Tips 221	L
Initialization217	7
Key Features217	7
Resources221	L
Alternate Interrupt Vector Table (AIVT)	5
Analog-to-Digital Converter (ADC)217	7
Arithmetic Logic Unit (ALU)	3

В

Bit-Reversed Addressing	76
Example	77
Implementation	76
Sequence Table (16-Entry)	77
Block Diagrams	
16-Bit Timer1 Module	165
6-Channel PWM1 Module	182
ADC1 Conversion Clock Period	221
ADC1 for dsPIC33FJ32(GP/MC)104 Devices	220
ADC1 for dsPIC33FJXX(GP/MC)101 Devices	218
ADC1 for dsPIC33FJXX(GP/MC)102 Devices	219
Comparator I/O Operating Modes	231
Comparator Voltage Reference	232
Connections for On-Chip Voltage Regulator	266
CTMU Module	256
Digital Filter Interconnect	233
DSP Engine	44
dsPIC33FJXX(GP/MC)10X CPU Core	38
dsPIC33FJXX(GP/MC)10X Devices	28
I ² C Module	204
Input Capture x Module	175
MCLR Pin Connections	34
Multiplexing of Remappable Output for RPn	144
Oscillator System	125
Output Compare x Module	177
Real-Time Clock and Calendar (RTCC) Module	243
Recommended Minimum Connection	34
Remappable MUX Input for U1RX	142
Reset System	87
Shared Port Structure	140
SPIx Module	197
Timer2 and Timer4 (16-Bit)	169
Timer2/3 and Timer4/5 (32-Bit)	168
Timer3 and Timer5 (16-Bit)	169
UARTx Simplified	211
User-Programmable Blanking Function	232
Watchdog Timer (WDT)	267
Brown-out Reset (BOR)	266

С

Charge Time Measurement Unit. See CTMU.	
Clock Switching	132
Enabling	132
Sequence	132
Code Examples	
Assembly Code for Write-Protected Register	
Unlock, Fault Clearing Sequence	184
C Code for Write-Protected Register Unlock,	
Fault Clearing Sequence	184
Port Write/Read	141
PWRSAV Instruction Syntax	133
Setting the RTCWREN Bit	244
Comparator	231
, Control Registers	234
Configuration Bits	261
Description	263
CPU	
Control Registers	40
Data Addressing	
Overview	
DSP Engine	43
Adder/Subtracter	-
Overflow and Saturation	45
Barrel Shifter	47
Data Accumulators	
Write Back	46
Data Accumulators and Adder/Subtracter.	45
Multiplier	45
Overview	37
Special MCU Features	
CPU Clocking System	126
Clock Selection	126
Clock Sources	126
Configuration Bit Values for Clock Selection	127
PLL Configuration	127
CTMU	
Control Registers	257
Customer Change Notification Service	387
Customer Notification Service	387
Customer Support	387
	007

D

Data Address Space	. 52
Memory Map for dsPIC33FJ16(GP/MC)101/102	
Devices, 1-Kbyte RAM	. 53
Memory Map for dsPIC33FJ32(GP/MC)101/102/104	
Devices, 2-Kbyte RAM	54
Near Data Space	. 52
Organization and Alignment	. 52
SFR Space	. 52
Software Stack	. 73
Width	. 52
X and Y Spaces	. 55

NOTES: