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Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	50MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (2), 10/100Mbps (1)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 95°C (TA)
Security Features	-
Package / Case	357-BBGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc860dpvr50d4

- Up to 8 Kbytes of dual-port RAM
- 16 serial DMA (SDMA) channels
- Three parallel I/O registers with open-drain capability
- Four baud-rate generators (BRGs)
 - Independent (can be tied to any SCC or SMC)
 - Allows changes during operation
 - Autobaud support option
- Four serial communications controllers (SCCs)
 - Ethernet/IEEE 802.3® standard optional on SCC1–4, supporting full 10-Mbps operation (available only on specially programmed devices)
 - HDLC/SDLC (all channels supported at 2 Mbps)
 - HDLC bus (implements an HDLC-based local area network (LAN))
 - Asynchronous HDLC to support point-to-point protocol (PPP)
 - AppleTalk
 - Universal asynchronous receiver transmitter (UART)
 - Synchronous UART
 - Serial infrared (IrDA)
 - Binary synchronous communication (BISYNC)
 - Totally transparent (bit streams)
 - Totally transparent (frame-based with optional cyclic redundancy check (CRC))
- Two SMCs (serial management channels)
 - UART
 - Transparent
 - General circuit interface (GCI) controller
 - Can be connected to the time-division multiplexed (TDM) channels
- One SPI (serial peripheral interface)
 - Supports master and slave modes
 - Supports multimaster operation on the same bus
- One I²C (inter-integrated circuit) port
 - Supports master and slave modes
 - Multiple-master environment support
- Time-slot assigner (TSA)
 - Allows SCCs and SMCs to run in multiplexed and/or non-multiplexed operation
 - Supports T1, CEPT, PCM highway, ISDN basic rate, ISDN primary rate, user defined
 - 1- or 8-bit resolution
 - Allows independent transmit and receive routing, frame synchronization, and clocking

Features

- Allows dynamic changes
- Can be internally connected to six serial channels (four SCCs and two SMCs)
- Parallel interface port (PIP)
 - Centronics interface support
 - Supports fast connection between compatible ports on the MPC860 or the MC68360
- PCMCIA interface
 - Master (socket) interface, release 2.1 compliant
 - Supports two independent PCMCIA sockets
 - Supports eight memory or I/O windows
- Low power support
 - Full on—all units fully powered
 - Doze—core functional units disabled except time base decrementer, PLL, memory controller, RTC, and CPM in low-power standby
 - Sleep—all units disabled except RTC and PIT, PLL active for fast wake up
 - Deep sleep—all units disabled including PLL except RTC and PIT
 - Power down mode—all units powered down except PLL, RTC, PIT, time base, and decrementer
- Debug interface
 - Eight comparators: four operate on instruction address, two operate on data address, and two operate on data
 - Supports conditions: = ≠ < >
 - Each watchpoint can generate a break-point internally.
- 3.3-V operation with 5-V TTL compatibility except EXTAL and EXTCLK
- 357-pin ball grid array (BGA) package

7 Thermal Calculation and Measurement

For the following discussions, $P_D = (V_{DD} \times I_{DD}) + P_{I/O}$, where $P_{I/O}$ is the power dissipation of the I/O drivers.

7.1 Estimation with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J , in °C can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_A = ambient temperature (°C)

$R_{\theta JA}$ = package junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in package

The junction-to-ambient thermal resistance is an industry standard value which provides a quick and easy estimation of thermal performance. However, the answer is only an estimate; test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

7.2 Estimation with Junction-to-Case Thermal Resistance

Historically, the thermal resistance has frequently been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)

$R_{\theta CA}$ = case-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user adjusts the thermal environment to affect the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the airflow around the device, add a heat sink, change the mounting arrangement on the printed-circuit board, or change the thermal dissipation on the printed-circuit board surrounding the device. This thermal model is most useful for ceramic packages with heat sinks where some 90% of the heat flows through the case and the heat sink to the ambient environment. For most packages, a better model is required.

7.3 Estimation with Junction-to-Board Thermal Resistance

A simple package thermal model which has demonstrated reasonable accuracy (about 20%) is a two-resistor model consisting of a junction-to-board and a junction-to-case thermal resistance. The junction-to-case thermal resistance covers the situation where a heat sink is used or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed-circuit board. It has been observed that the thermal performance of most plastic packages, especially PBGA packages, is strongly dependent on the board temperature; see [Figure 2](#).

where:

Ψ_{JT} = thermal characterization parameter

T_T = thermocouple temperature on top of package

P_D = power dissipation in package

The thermal characterization parameter is measured per JEDEC JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

7.6 References

Semiconductor Equipment and Materials International (415) 964-5111
805 East Middlefield Rd.
Mountain View, CA 94043

MIL-SPEC and EIA/JESD (JEDEC) Specifications 800-854-7179 or
(Available from Global Engineering Documents) 303-397-7956

JEDEC Specifications <http://www.jedec.org>

1. C.E. Triplett and B. Joiner, "An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module," Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.
2. B. Joiner and V. Adams, "Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling," Proceedings of SemiTherm, San Diego, 1999, pp. 212–220.

8 Layout Practices

Each V_{DD} pin on the MPC860 should be provided with a low-impedance path to the board's supply. Each GND pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on the chip. The V_{DD} power supply should be bypassed to ground using at least four 0.1 μ F-bypass capacitors located as close as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to chip V_{DD} and GND should be kept to less than half an inch per capacitor lead. A four-layer board employing two inner layers as V_{CC} and GND planes is recommended.

All output pins on the MPC860 have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized in order to minimize undershoot and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data buses. Maximum PC trace lengths of 6 inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the V_{CC} and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.

Table 7. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B35	A(0:31), BADDR(28:30) to \overline{CS} valid—as requested by control bit BST4 in the corresponding word in UPM	5.58	—	4.25	—	3.00	—	1.79	—	ns
B35a	A(0:31), BADDR(28:30), and D(0:31) to \overline{BS} valid—as requested by control bit BST1 in the corresponding word in UPM	13.15	—	10.50	—	8.00	—	5.58	—	ns
B35b	A(0:31), BADDR(28:30), and D(0:31) to \overline{BS} valid—as requested by control bit BST2 in the corresponding word in UPM	20.73	—	16.75	—	13.00	—	9.36	—	ns
B36	A(0:31), BADDR(28:30), and D(0:31) to \overline{GPL} valid—as requested by control bit GxT4 in the corresponding word in UPM	5.58	—	4.25	—	3.00	—	1.79	—	ns
B37	UPWAIT valid to CLKOUT falling edge ⁹	6.00	—	6.00	—	6.00	—	6.00	—	ns
B38	CLKOUT falling edge to UPGATE valid ⁹	1.00	—	1.00	—	1.00	—	1.00	—	ns
B39	\overline{AS} valid to CLKOUT rising edge ¹⁰	7.00	—	7.00	—	7.00	—	7.00	—	ns
B40	A(0:31), TSIZ(0:1), RD/ \overline{WR} , \overline{BURST} , valid to CLKOUT rising edge	7.00	—	7.00	—	7.00	—	7.00	—	ns
B41	\overline{TS} valid to CLKOUT rising edge (setup time)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B42	CLKOUT rising edge to \overline{TS} valid (hold time)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B43	\overline{AS} negation to memory controller signals negation	—	TBD	—	TBD	—	TBD	—	TBD	ns

¹ Phase and frequency jitter performance results are only valid if the input jitter is less than the prescribed value.

² If the rate of change of the frequency of EXTAL is slow (that is, it does not jump between the minimum and maximum values in one cycle) or the frequency of the jitter is fast (that is, it does not stay at an extreme value for a long time) then the maximum allowed jitter on EXTAL can be up to 2%.

³ The timings specified in B4 and B5 are based on full strength clock.

⁴ The timing for \overline{BR} output is relevant when the MPC860 is selected to work with external bus arbiter. The timing for \overline{BG} output is relevant when the MPC860 is selected to work with internal bus arbiter.

⁵ The timing required for \overline{BR} input is relevant when the MPC860 is selected to work with internal bus arbiter. The timing for \overline{BG} input is relevant when the MPC860 is selected to work with external bus arbiter.

⁶ The D(0:31) and DP(0:3) input timings B18 and B19 refer to the rising edge of the CLKOUT in which the \overline{TA} input signal is asserted.

⁷ The D(0:31) and DP(0:3) input timings B20 and B21 refer to the falling edge of the CLKOUT. This timing is valid only for read accesses controlled by chip-selects under control of the UPM in the memory controller, for data beats where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

⁸ The timing B30 refers to \overline{CS} when ACS = 00 and to \overline{WE} (0:3) when CSNT = 0.

⁹ The signal UPGATE is considered asynchronous to the CLKOUT and synchronized internally. The timings specified in B37 and B38 are specified to enable the freeze of the UPM output signals as described in [Figure 18](#).

¹⁰ The \overline{AS} signal is considered asynchronous to the CLKOUT. The timing B39 is specified in order to allow the behavior specified in [Figure 21](#).

Figure 7 provides the timing for the synchronous input signals.

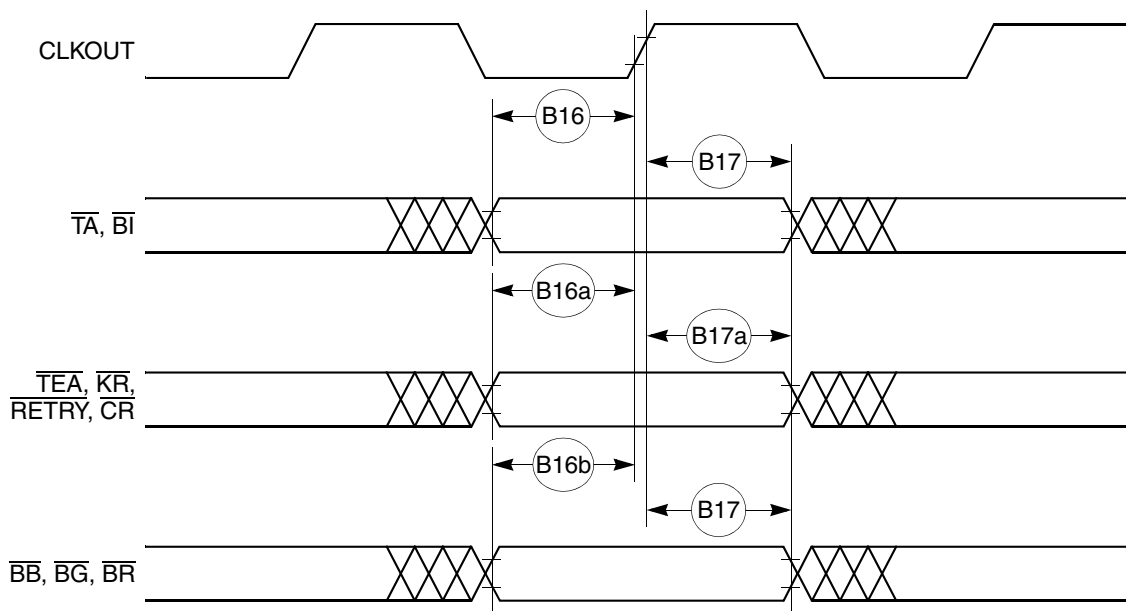


Figure 7. Synchronous Input Signals Timing

Figure 8 provides normal case timing for input data. It also applies to normal read accesses under the control of the UPM in the memory controller.

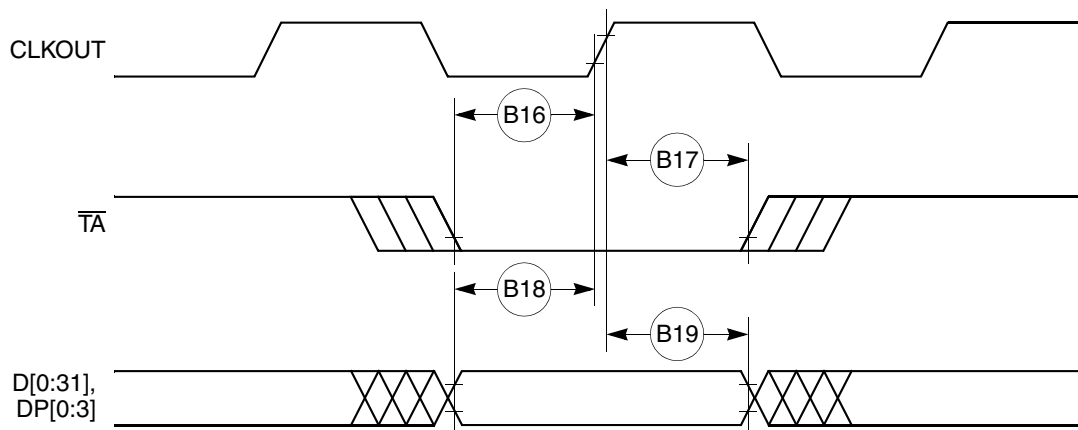


Figure 8. Input Data Timing in Normal Case

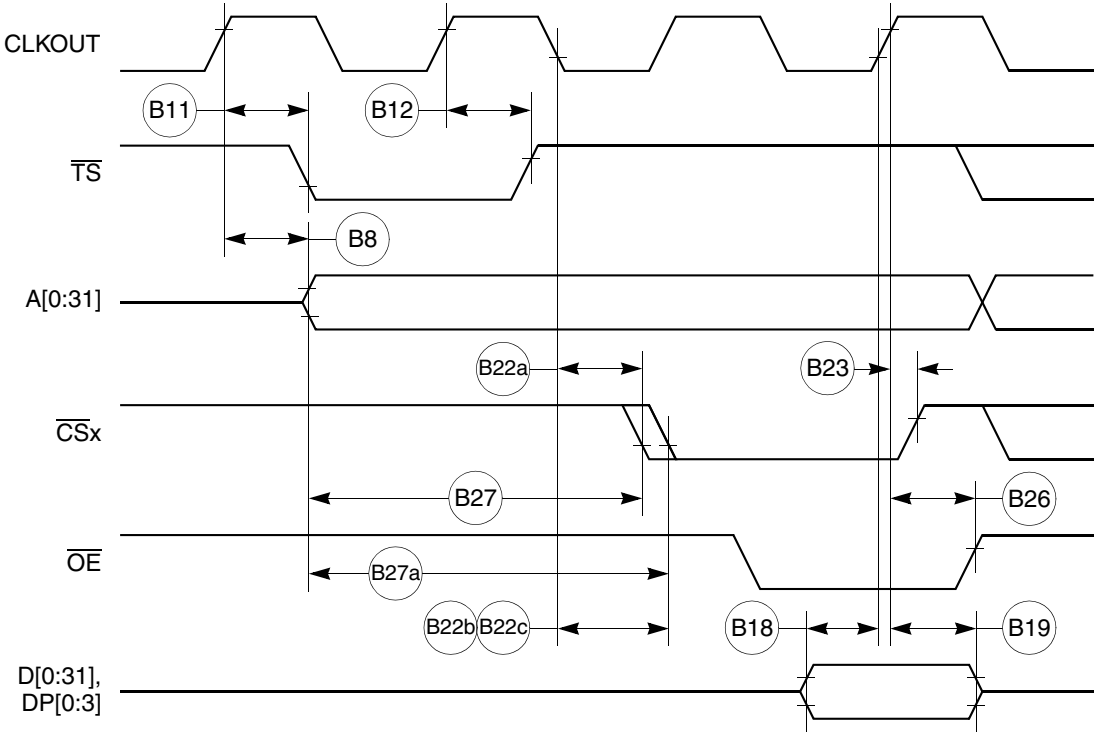


Figure 13. External Bus Read Timing (GPCM Controlled—TRLX = 0 or 1, ACS = 10, ACS = 11)

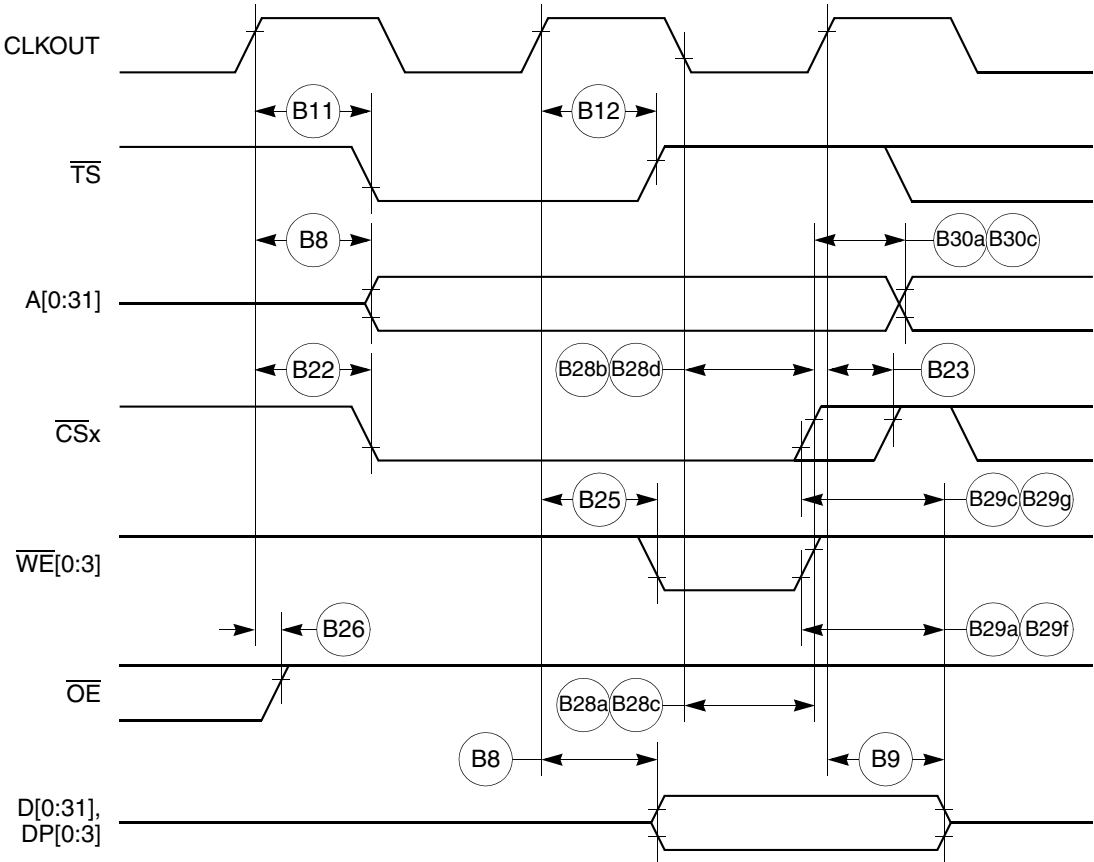


Figure 15. External Bus Write Timing (GPCM Controlled—TRLX = 0 or 1, CSNT = 1)

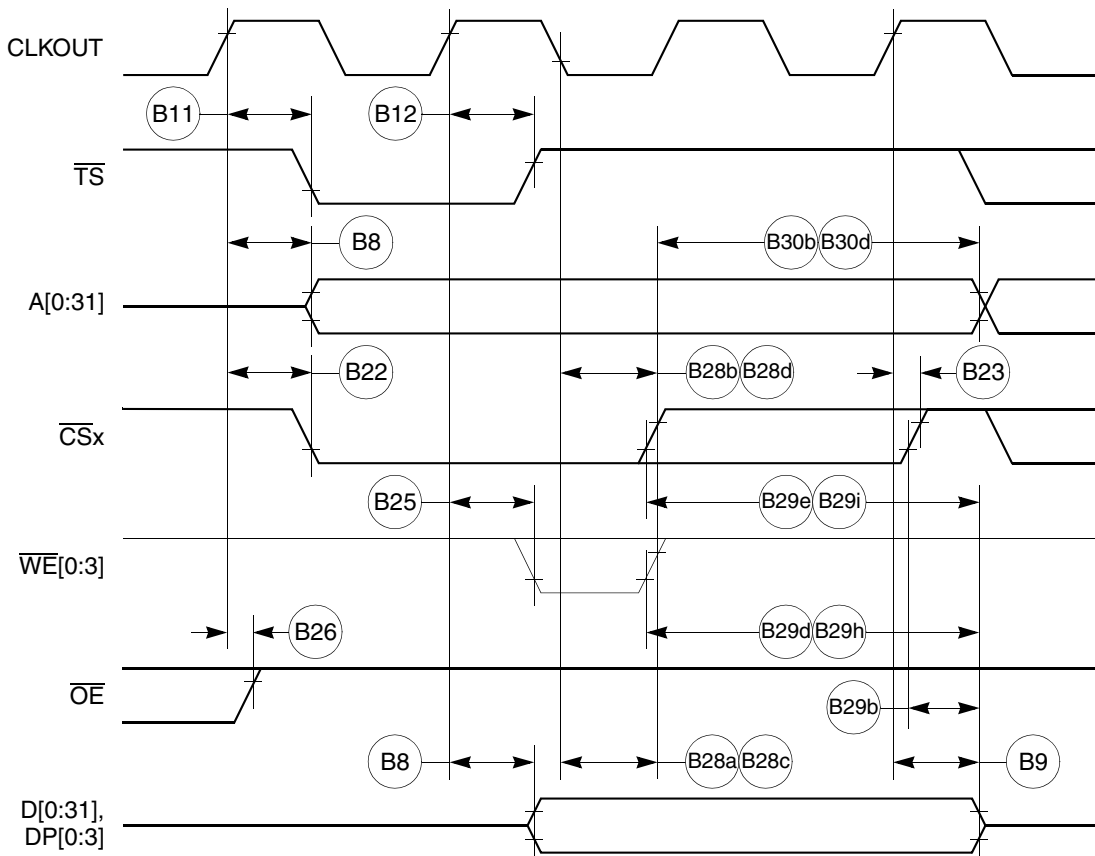


Figure 16. External Bus Write Timing (GPCM Controlled—TRLX = 0 or 1, CSNT = 1)

Figure 17 provides the timing for the external bus controlled by the UPM.

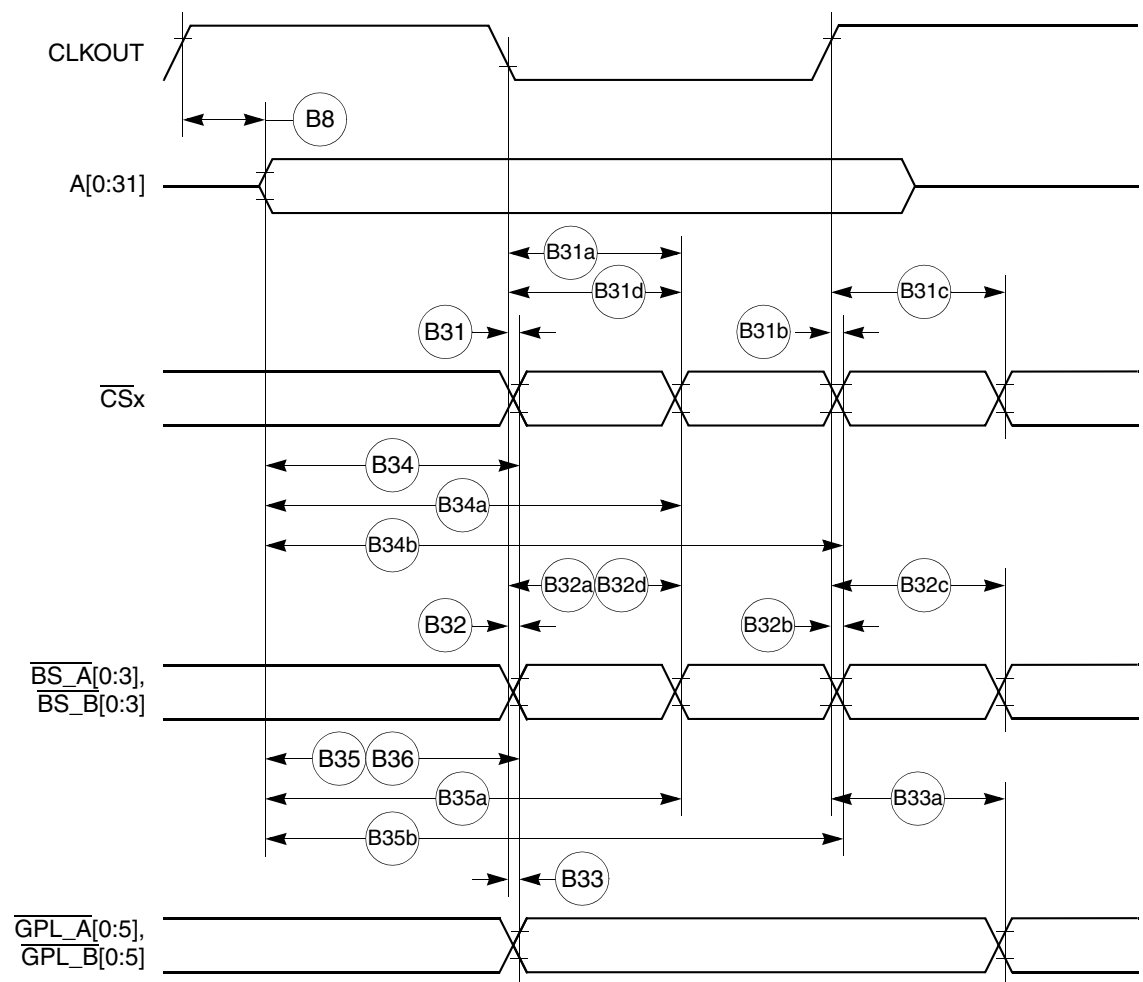


Figure 17. External Bus Timing (UPM Controlled Signals)

Table 9 shows the PCMCIA timing for the MPC860.

Table 9. PCMCIA Timing

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
P44	A(0:31), $\overline{\text{REG}}$ valid to PCMCIA Strobe asserted ¹	20.73	—	16.75	—	13.00	—	9.36	—	ns
P45	A(0:31), $\overline{\text{REG}}$ valid to ALE negation ¹	28.30	—	23.00	—	18.00	—	13.15	—	ns
P46	CLKOUT to $\overline{\text{REG}}$ valid	7.58	15.58	6.25	14.25	5.00	13.00	3.79	11.84	ns
P47	CLKOUT to $\overline{\text{REG}}$ invalid	8.58	—	7.25	—	6.00	—	4.84	—	ns
P48	CLKOUT to $\overline{\text{CE1}}$, $\overline{\text{CE2}}$ asserted	7.58	15.58	6.25	14.25	5.00	13.00	3.79	11.84	ns
P49	CLKOUT to $\overline{\text{CE1}}$, $\overline{\text{CE2}}$ negated	7.58	15.58	6.25	14.25	5.00	13.00	3.79	11.84	ns
P50	CLKOUT to $\overline{\text{PCOE}}$, $\overline{\text{IORD}}$, $\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ assert time	—	11.00		11.00	—	11.00	—	11.00	ns
P51	CLKOUT to $\overline{\text{PCOE}}$, $\overline{\text{IORD}}$, $\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ negate time	2.00	11.00	2.00	11.00	2.00	11.00	2.00	11.00	ns
P52	CLKOUT to ALE assert time	7.58	15.58	6.25	14.25	5.00	13.00	3.79	10.04	ns
P53	CLKOUT to ALE negate time	—	15.58		14.25	—	13.00	—	11.84	ns
P54	$\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ negated to D(0:31) invalid ¹	5.58	—	4.25	—	3.00	—	1.79	—	ns
P55	$\overline{\text{WAITA}}$ and $\overline{\text{WAITB}}$ valid to CLKOUT rising edge ¹	8.00	—	8.00	—	8.00	—	8.00	—	ns
P56	CLKOUT rising edge to $\overline{\text{WAITA}}$ and $\overline{\text{WAITB}}$ invalid ¹	2.00	—	2.00	—	2.00	—	2.00	—	ns

¹ PSST = 1. Otherwise add PSST times cycle time.

PSHT = 0. Otherwise add PSHT times cycle time.

These synchronous timings define when the $\overline{\text{WAITx}}$ signals are detected in order to freeze (or relieve) the PCMCIA current cycle. The $\overline{\text{WAITx}}$ assertion will be effective only if it is detected 2 cycles before the PSL timer expiration. See Chapter 16, “PCMCIA Interface,” in the *MPC860 PowerQUICC™ Family User's Manual*.

Table 10 shows the PCMCIA port timing for the MPC860.

Table 10. PCMCIA Port Timing

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
P57	CLKOUT to OPx valid	—	19.00	—	19.00	—	19.00	—	19.00	ns
P58	$\overline{\text{HRESET}}$ negated to OPx drive ¹	25.73	—	21.75	—	18.00	—	14.36	—	ns
P59	IP_Xx valid to CLKOUT rising edge	5.00	—	5.00	—	5.00	—	5.00	—	ns
P60	CLKOUT rising edge to IP_Xx invalid	1.00	—	1.00	—	1.00	—	1.00	—	ns

¹ OP2 and OP3 only.

Figure 28 provides the PCMCIA output port timing for the MPC860.

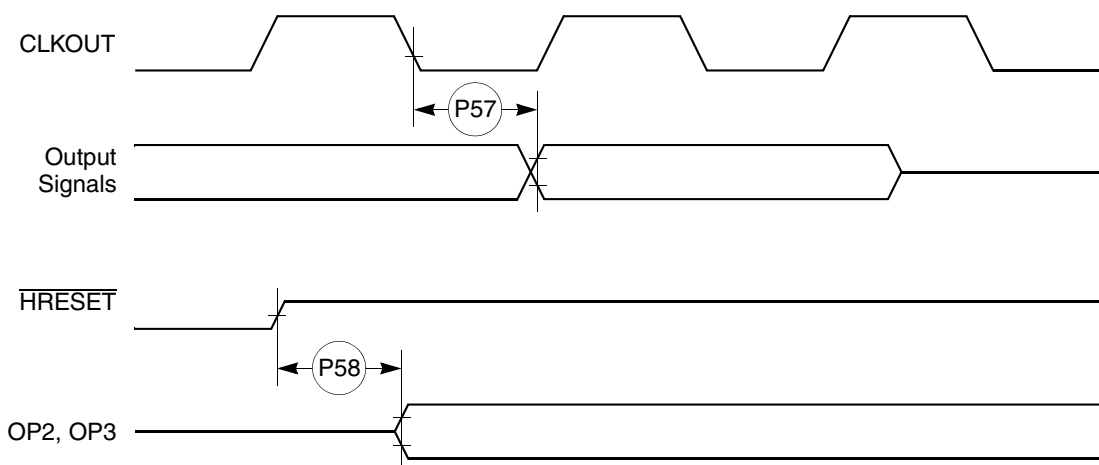


Figure 28. PCMCIA Output Port Timing

Figure 29 provides the PCMCIA output port timing for the MPC860.

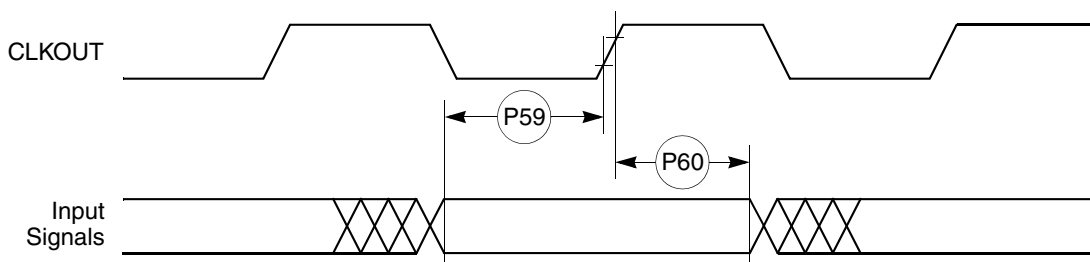


Figure 29. PCMCIA Input Port Timing

Table 12 shows the reset timing for the MPC860.

Table 12. Reset Timing

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
R69	CLKOUT to $\overline{\text{HRESET}}$ high impedance	—	20.00	—	20.00	—	20.00	—	20.00	ns
R70	CLKOUT to $\overline{\text{SRESET}}$ high impedance	—	20.00	—	20.00	—	20.00	—	20.00	ns
R71	$\overline{\text{RSTCONF}}$ pulse width	515.15	—	425.00	—	340.00	—	257.58	—	ns
R72	—	—	—	—	—	—	—	—	—	
R73	Configuration data to $\overline{\text{HRESET}}$ rising edge setup time	504.55	—	425.00	—	350.00	—	277.27	—	ns
R74	Configuration data to $\overline{\text{RSTCONF}}$ rising edge setup time	350.00	—	350.00	—	350.00	—	350.00	—	ns
R75	Configuration data hold time after $\overline{\text{RSTCONF}}$ negation	0.00	—	0.00	—	0.00	—	0.00	—	ns
R76	Configuration data hold time after $\overline{\text{HRESET}}$ negation	0.00	—	0.00	—	0.00	—	0.00	—	ns
R77	$\overline{\text{HRESET}}$ and $\overline{\text{RSTCONF}}$ asserted to data out drive	—	25.00	—	25.00	—	25.00	—	25.00	ns
R78	$\overline{\text{RSTCONF}}$ negated to data out high impedance	—	25.00	—	25.00	—	25.00	—	25.00	ns
R79	CLKOUT of last rising edge before chip three-state $\overline{\text{HRESET}}$ to data out high impedance	—	25.00	—	25.00	—	25.00	—	25.00	ns
R80	DSDI, DSCK setup	90.91	—	75.00	—	60.00	—	45.45	—	ns
R81	DSDI, DSCK hold time	0.00	—	0.00	—	0.00	—	0.00	—	ns
R82	$\overline{\text{SRESET}}$ negated to CLKOUT rising edge for DSDI and DSCK sample	242.42	—	200.00	—	160.00	—	121.21	—	ns

Table 16. IDMA Controller Timing (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
42	$\overline{\text{SDACK}}$ assertion delay from clock high	—	12	ns
43	$\overline{\text{SDACK}}$ negation delay from clock low	—	12	ns
44	$\overline{\text{SDACK}}$ negation delay from $\overline{\text{TA}}$ low	—	20	ns
45	$\overline{\text{SDACK}}$ negation delay from clock high	—	15	ns
46	$\overline{\text{TA}}$ assertion to rising edge of the clock setup time (applies to external $\overline{\text{TA}}$)	7	—	ns

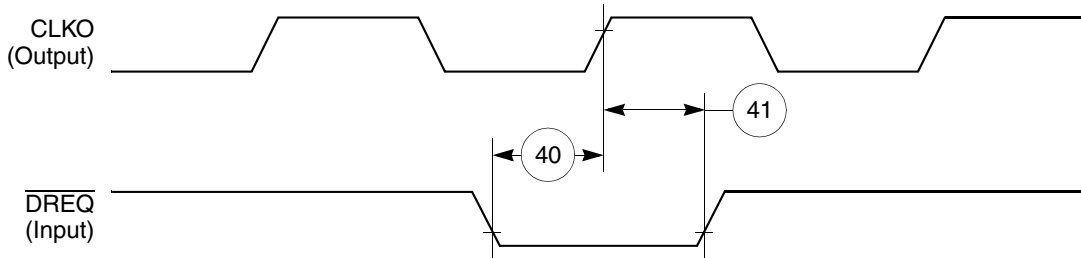


Figure 45. IDMA External Requests Timing Diagram

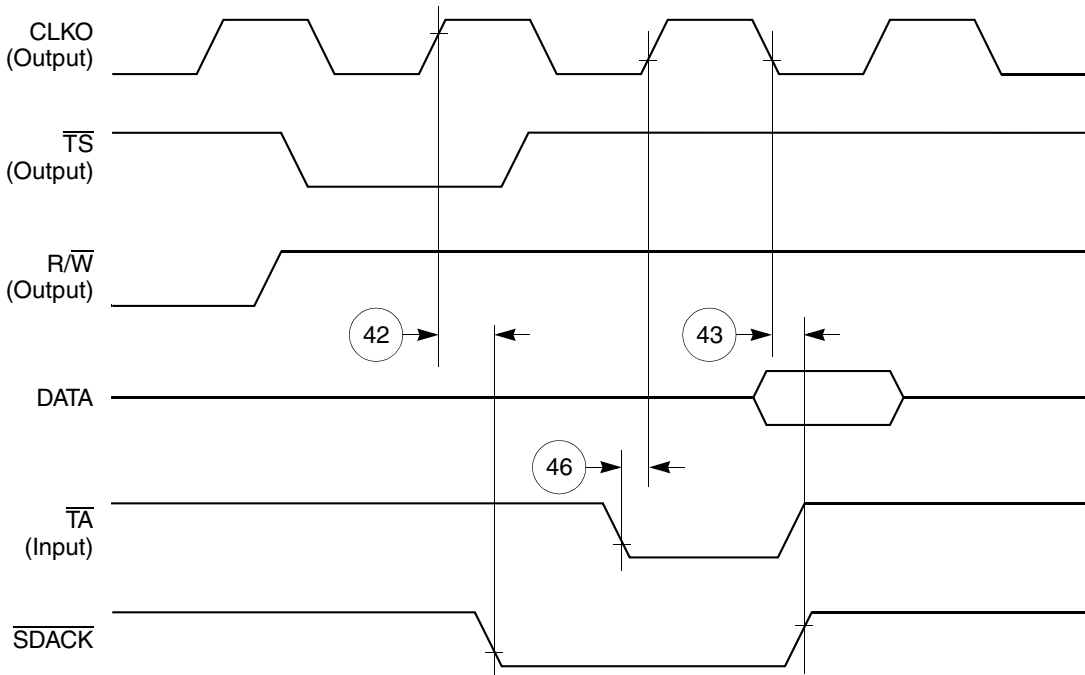


Figure 46. $\overline{\text{SDACK}}$ Timing Diagram—Peripheral Write, Externally-Generated $\overline{\text{TA}}$

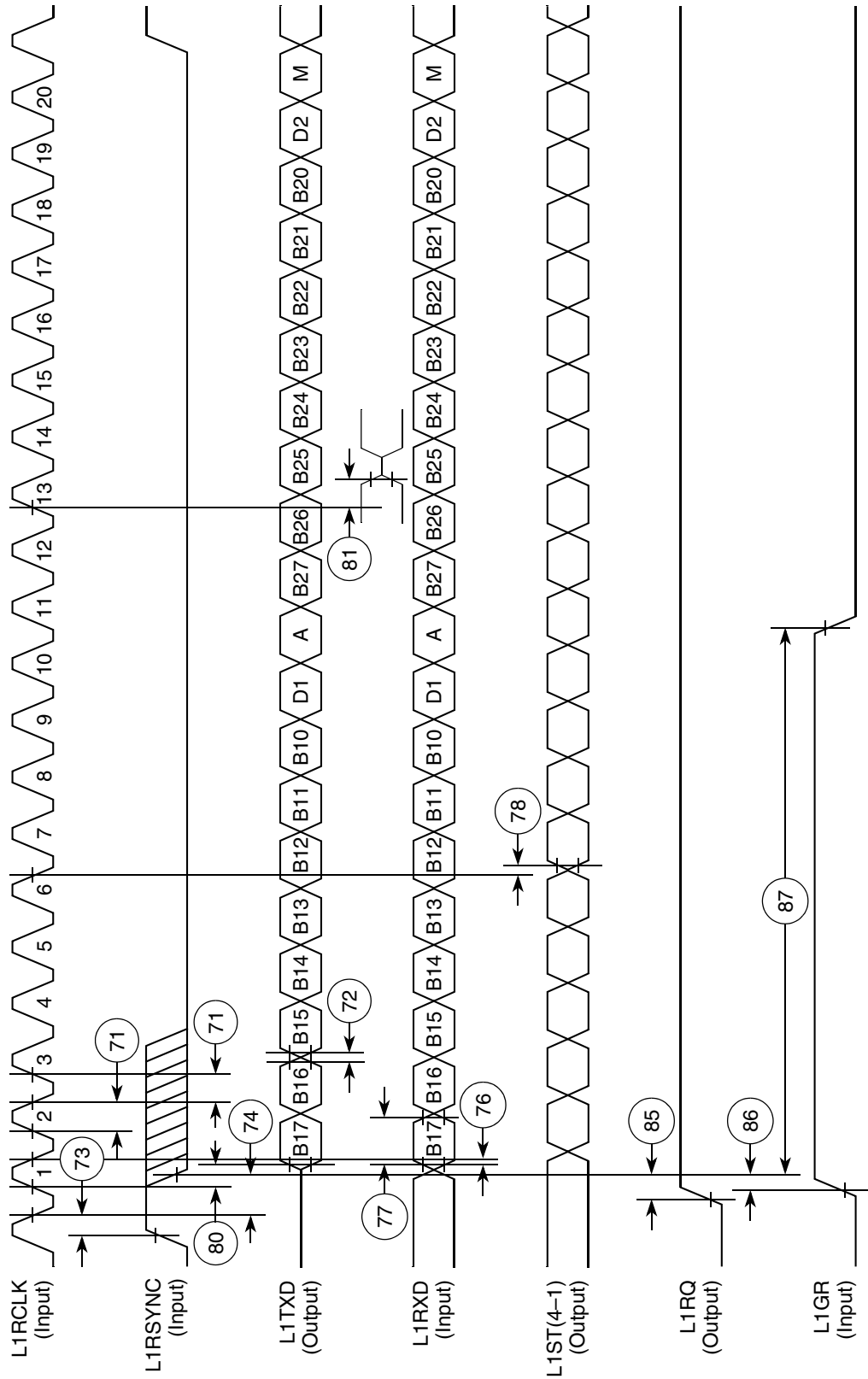


Figure 55. IDL Timing

11.7 SCC in NMSI Mode Electrical Specifications

Table 20 provides the NMSI external clock timing.

Table 20. NMSI External Clock Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
100	RCLK1 and TCLK1 width high ¹	1/SYNCCLK	—	ns
101	RCLK1 and TCLK1 width low	1/SYNCCLK + 5	—	ns
102	RCLK1 and TCLK1 rise/fall time	—	15.00	ns
103	TXD1 active delay (from TCLK1 falling edge)	0.00	50.00	ns
104	$\overline{\text{RTS1}}$ active/inactive delay (from TCLK1 falling edge)	0.00	50.00	ns
105	$\overline{\text{CTS1}}$ setup time to TCLK1 rising edge	5.00	—	ns
106	RXD1 setup time to RCLK1 rising edge	5.00	—	ns
107	RXD1 hold time from RCLK1 rising edge ²	5.00	—	ns
108	$\overline{\text{CD1}}$ setup Time to RCLK1 rising edge	5.00	—	ns

¹ The ratios SYNCCLK/RCLK1 and SYNCCLK/TCLK1 must be greater than or equal to 2.25/1.

² Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as external sync signals.

Table 21 provides the NMSI internal clock timing.

Table 21. NMSI Internal Clock Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
100	RCLK1 and TCLK1 frequency ¹	0.00	SYNCCLK/3	MHz
102	RCLK1 and TCLK1 rise/fall time	—	—	ns
103	TXD1 active delay (from TCLK1 falling edge)	0.00	30.00	ns
104	$\overline{\text{RTS1}}$ active/inactive delay (from TCLK1 falling edge)	0.00	30.00	ns
105	$\overline{\text{CTS1}}$ setup time to TCLK1 rising edge	40.00	—	ns
106	RXD1 setup time to RCLK1 rising edge	40.00	—	ns
107	RXD1 hold time from RCLK1 rising edge ²	0.00	—	ns
108	$\overline{\text{CD1}}$ setup time to RCLK1 rising edge	40.00	—	ns

¹ The ratios SYNCCLK/RCLK1 and SYNCCLK/TCLK1 must be greater than or equal to 3/1.

² Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as external sync signals.

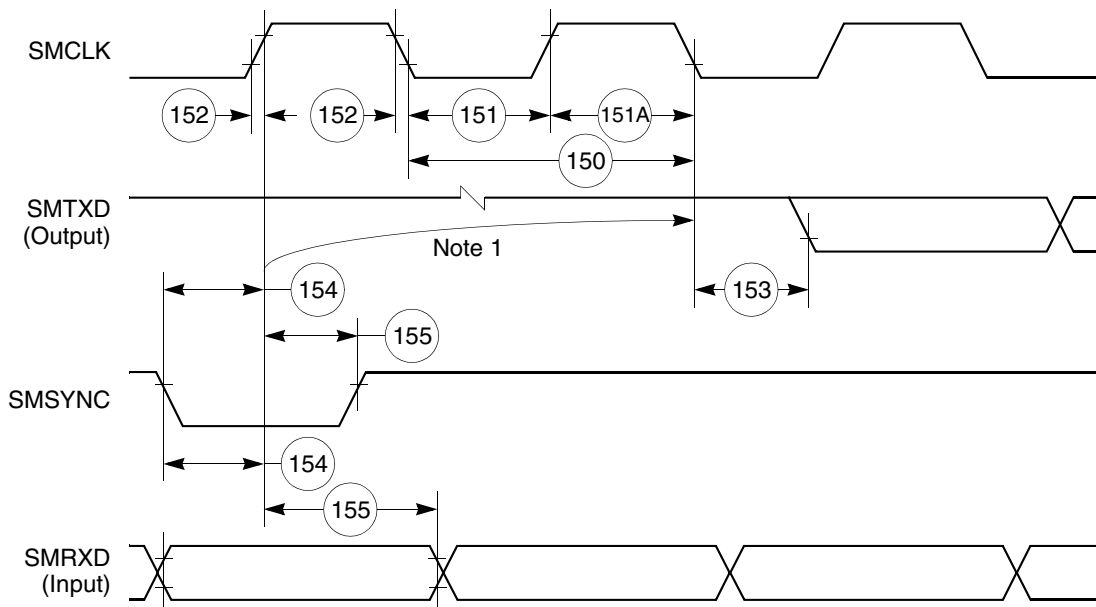
11.9 SMC Transparent AC Electrical Specifications

Table 23 provides the SMC transparent timings as shown in Figure 64.

Table 23. SMC Transparent Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
150	SMCLK clock period ¹	100	—	ns
151	SMCLK width low	50	—	ns
151A	SMCLK width high	50	—	ns
152	SMCLK rise/fall time	—	15	ns
153	SMTXD active delay (from SMCLK falling edge)	10	50	ns
154	SMRXD/SMSYNC setup time	20	—	ns
155	RXD1/SMSYNC hold time	5	—	ns

¹ SYNCCLK must be at least twice as fast as SMCLK.



Note:

1. This delay is equal to an integer number of character-length clocks.

Figure 64. SMC Transparent Timing Diagram

Figure 75 shows the MII serial management channel timing diagram.

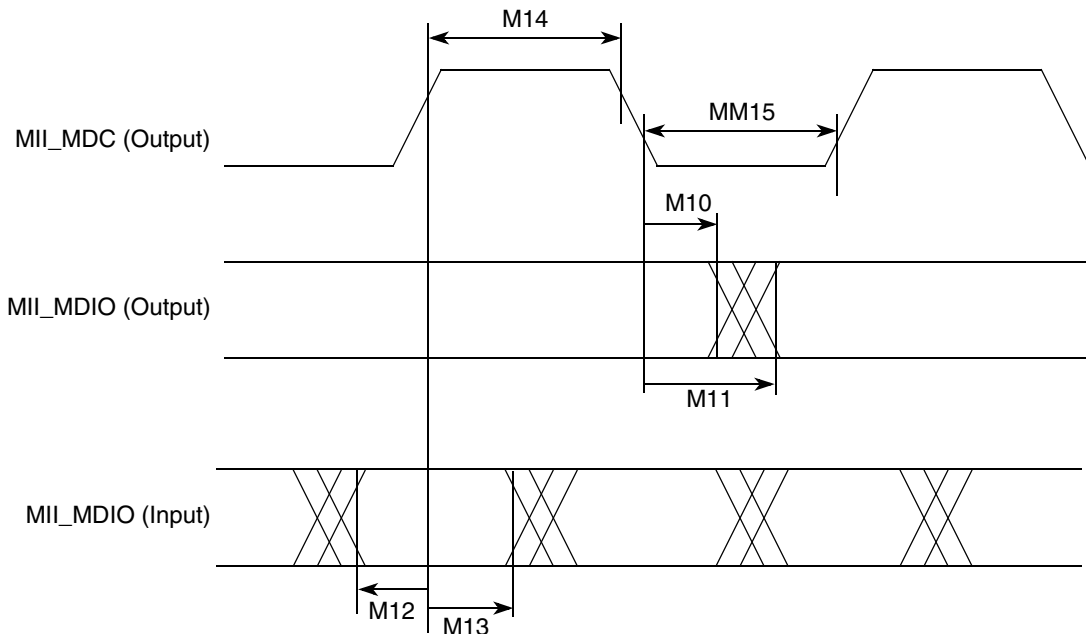


Figure 75. MII Serial Management Channel Timing Diagram

14 Mechanical Data and Ordering Information

14.1 Ordering Information

Table 33 provides information on the MPC860 Revision D.4 derivative devices.

Table 33. MPC860 Family Revision D.4 Derivatives

Device	Number of SCCs ¹	Ethernet Support ² (Mbps)	Multichannel HDLC Support	ATM Support
MPC855T	1	10/100	Yes	Yes
MPC860DE	2	10	N/A	N/A
MPC860DT		10/100	Yes	Yes
MPC860DP		10/100	Yes	Yes
MPC860EN	4	10	N/A	N/A
MPC860SR		10	Yes	Yes
MPC860T		10/100	Yes	Yes
MPC860P		10/100	Yes	Yes

¹ Serial communications controller (SCC)

² Up to 4 channels at 40 MHz or 2 channels at 25 MHz

Table 34. MPC860 Family Package/Frequency Availability (continued)

Package Type	Freq. (MHz) / Temp. (Tj)	Package	Order Number
Ball grid array (<i>continued</i>) ZP suffix—leaded ZQ suffix—leaded VR suffix—lead-free	80 0° to 95°C	ZP/ZQ ¹	MPC855TZQ80D4 MPC860DEZQ80D4 MPC860DTZQ80D4 MPC860ENZQ80D4 MPC860SRZQ80D4 MPC860TZQ80D4 MPC860DPZQ80D4 MPC860PZQ80D4
		Tape and Reel	MPC860PZQ80D4R2 MPC860PVR80D4R2
		VR	MPC855TVR80D4 MPC860DEV80D4 MPC860DPVR80D4 MPC860ENVR80D4 MPC860PVR80D4 MPC860SRVR80D4 MPC860TVR80D4
Ball grid array (CZP suffix) CZP suffix—leaded CZQ suffix—leaded CVR suffix—lead-free	50 –40° to 95°C	ZP/ZQ ¹	MPC855TCZQ50D4 MPC855TCVR50D4 MPC860DECZQ50D4 MPC860DTCZQ50D4 MPC860ENCZQ50D4 MPC860SRCZQ50D4 MPC860TCZQ50D4 MPC860DPCZQ50D4 MPC860PCZQ50D4
		Tape and Reel	MPC855TCZQ50D4R2 MC860ENCVR50D4R2
		CVR	MPC860DECVR50D4 MPC860DTCVR50D4 MPC860ENCVR50D4 MPC860PCVR50D4 MPC860SRCVR50D4 MPC860TCVR50D4
	66 –40° to 95°C	ZP/ZQ ¹	MPC855TCZQ66D4 MPC855TCVR66D4 MPC860ENCZQ66D4 MPC860SRCZQ66D4 MPC860TCZQ66D4 MPC860DPCZQ66D4 MPC860PCZQ66D4
		CVR	MPC860DTCVR66D4 MPC860ENCVR66D4 MPC860PCVR66D4 MPC860SRCVR66D4 MPC860TCVR66D4

¹ The ZP package is no longer recommended for use. The ZQ package replaces the ZP package.

14.2 Pin Assignments

Figure 76 shows the top view pinout of the PBGA package. For additional information, see the *MPC860 PowerQUICC User's Manual*, or the *MPC855T User's Manual*.

NOTE: This is the top view of the device.

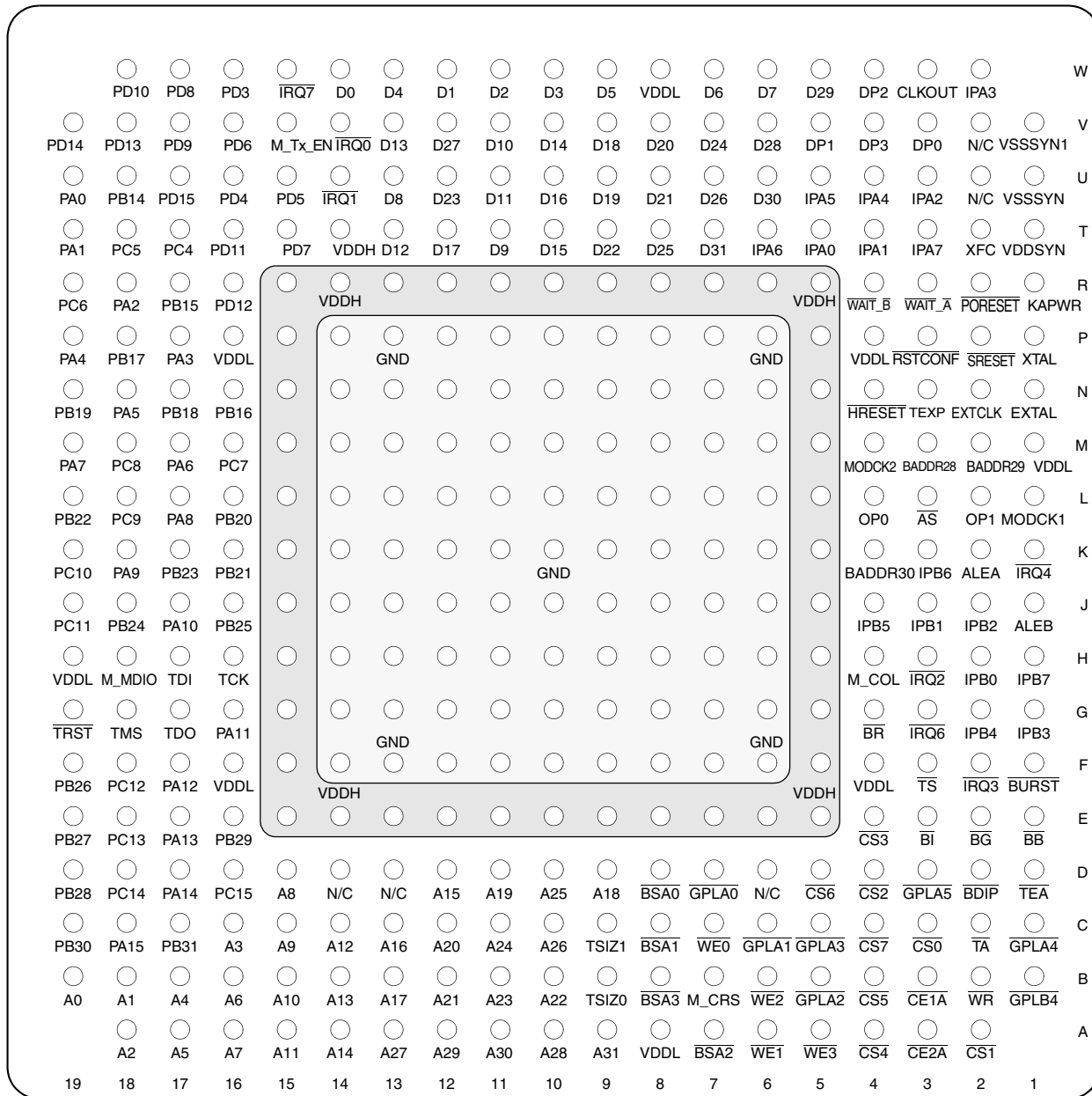


Figure 76. Pinout of the PBGA Package