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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	66MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (2), 10/100Mbps (1)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 95°C (TA)
Security Features	-
Package / Case	357-BBGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc860dtcvr66d4

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Overview

1 Overview

The MPC860 power quad integrated communications controller (PowerQUICCTM) is a versatile one-chip integrated microprocessor and peripheral combination designed for a variety of controller applications. It particularly excels in communications and networking systems. The PowerQUICC unit is referred to as the MPC860 in this hardware specification.

The MPC860 implements Power ArchitectureTM technology and contains a superset of Freescale's MC68360 quad integrated communications controller (QUICC), referred to here as the QUICC, RISC communications proceessor module (CPM). The CPU on the MPC860 is a 32-bit core built on Power Architecture technology that incorporates memory management units (MMUs) and instruction and data caches.. The CPM from the MC68360 QUICC has been enhanced by the addition of the inter-integrated controller (I²C) channel. The memory controller has been enhanced, enabling the MPC860 to support any type of memory, including high-performance memories and new types of DRAMs. A PCMCIA socket controller supports up to two sockets. A real-time clock has also been integrated.

Table 1 shows the functionality supported by the MPC860 family.

	Cache (Kbytes)	Ethe	ernet				
Part	Instruction Cache	Data Cache	10T	10/100	ΑΤΜ	SCC	Reference ¹	
MPC860DE	4	4	Up to 2	_	_	2	1	
MPC860DT	4	4	Up to 2	1	Yes	2	1	
MPC860DP	16	8	Up to 2	1	Yes	2	1	
MPC860EN	4	4	Up to 4	—	—	4	1	
MPC860SR	4	4	Up to 4	—	Yes	4	1	
MPC860T	4	4	Up to 4	1	Yes	4	1	
MPC860P	16	8	Up to 4	1	Yes	4	1	
MPC855T	4	4	1	1	Yes	1	2	

Table 1. MPC860 Family Functionality

Supporting documentation for these devices refers to the following:

1. MPC860 PowerQUICC Family User's Manual (MPC860UM, Rev. 3)

2. MPC855T User's Manual (MPC855TUM, Rev. 1)



Power Dissipation

5 **Power Dissipation**

Table 5 provides power dissipation information. The modes are 1:1, where CPU and bus speeds are equal, and 2:1, where CPU frequency is twice the bus speed.

Die Revision	Frequency (MHz)	Typical ¹	Maximum ²	Unit
D.4	50	656	735	mW
(1:1 mode)	66	TBD	TBD	mW
D.4	66	722	762	mW
(2:1 mode)	80	851	909	mW

Table 5. Power Dissipation (PD)

¹ Typical power dissipation is measured at 3.3 V.

² Maximum power dissipation is measured at 3.5 V.

NOTE

Values in Table 5 represent V_{DDL} -based power dissipation and do not include I/O power dissipation over V_{DDH} . I/O power dissipation varies widely by application due to buffer current, depending on external circuitry.

6 DC Characteristics

Table 6 provides the DC electrical characteristics for the MPC860.

 Table 6. DC Electrical Specifications

Characteristic	Symbol	Min	Мах	Unit
Operating voltage at 40 MHz or less	V _{DDH} , V _{DDL} , V _{DDSYN}	3.0	3.6	V
	KAPWR (power-down mode)	2.0	3.6	V
	KAPWR (all other operating modes)	V _{DDH} – 0.4	V _{DDH}	V
Operating voltage greater than 40 MHz	V _{DDH} , V _{DDL} , KAPWR, V _{DDSYN}	3.135	3.465	V
	KAPWR (power-down mode)	2.0	3.6	V
	KAPWR (all other operating modes)	V _{DDH} – 0.4	V _{DDH}	V
Input high voltage (all inputs except EXTAL and EXTCLK)	V _{IH}	2.0	5.5	V
Input low voltage ¹	V _{IL}	GND	0.8	V
EXTAL, EXTCLK input high voltage	V _{IHC}	$0.7 imes (V_{DDH})$	V _{DDH} + 0.3	V
Input leakage current, $V_{in} = 5.5 \text{ V}$ (except TMS, TRST, DSCK, and DSDI pins)	l _{in}	—	100	μA



		33	MHz	40 1	MHz	50 I	MHz	66 MHz		
Num	Characteristic	Min	Мах	Min	Мах	Min	Мах	Min	Max	Unit
B29d	$\overline{WE}(0:3)$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 0	43.45		35.5	_	28.00		20.73	_	ns
B29e	$\overline{\text{CS}}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 0	43.45		35.5		28.00		29.73	_	ns
B29f	\overline{WE} (0:3) negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 1	8.86	_	6.88	_	5.00	_	3.18		ns
B29g	$\overline{\text{CS}}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 1	8.86	_	6.88	—	5.00	—	3.18	_	ns
B29h	$\overline{WE}(0:3)$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 1	38.67	—	31.38	—	24.50	—	17.83	_	ns
B29i	$\overline{\text{CS}}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 1	38.67		31.38		24.50		17.83	_	ns
B30	\overline{CS} , \overline{WE} (0:3) negated to A(0:31), BADDR(28:30) invalid GPCM write access ⁸	5.58	—	4.25	—	3.00	—	1.79		ns
B30a	$\overline{\text{WE}}(0:3)$ negated to A(0:31), BADDR(28:30) invalid GPCM, write access, TRLX = 0, CSNT = 1, $\overline{\text{CS}}$ negated to A(0:31) invalid GPCM write access, TRLX = 0, CSNT = 1 ACS = 10, or ACS = 11, EBDF = 0	13.15	_	10.50	_	8.00	_	5.58		ns
B30b	$\label{eq:weighted} \hline WE(0:3) \ negated to \ A(0:31), \ invalid \ GPCM \\ BADDR(28:30) \ invalid \ GPCM \ write \ access, \\ TRLX = 1, \ CSNT = 1. \ \overline{CS} \ negated to \\ A(0:31), \ Invalid \ GPCM, \ write \ access, \\ TRLX = 1, \ CSNT = 1, \ ACS = 10, \ or \\ ACS = 11, \ EBDF = 0 \\ \hline \hline \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \$	43.45	_	35.50	_	28.00	_	20.73	_	ns
B30c	$\label{eq:weighted} \begin{array}{ c c c c } \hline WE(0:3) \mbox{ negated to } A(0:31), \mbox{ BADDR}(28:30) \\ \hline \mbox{ invalid GPCM write access, TRLX = 0, } \\ \hline CSNT = 1. \end{cmathcelline CS} \mbox{ negated to } A(0:31) \mbox{ invalid GPCM write access, TRLX = 0, } \\ \hline GPCM \mbox{ write access, TRLX = 0, } \\ \hline ACS = 10, \mbox{ ACS = 11, EBDF = 1} \end{array}$	8.36	_	6.38	_	4.50	_	2.68		ns
B30d	$\overline{WE}(0:3)$ negated to A(0:31), BADDR(28:30) invalid GPCM write access, TRLX = 1, CSNT =1. \overline{CS} negated to A(0:31) invalid GPCM write access TRLX = 1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 1	38.67	_	31.38	_	24.50	_	17.83		ns
B31	CLKOUT falling edge to CS valid—as requested by control bit CST4 in the corresponding word in UPM	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns

Table 7. Bus Operation Timings (continued)



Figure 9 provides the timing for the input data controlled by the UPM for data beats where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)



Figure 9. Input Data Timing when Controlled by UPM in the Memory Controller and DLT3 = 1

Figure 10 through Figure 13 provide the timing for the external bus read controlled by various GPCM factors.







Figure 20 provides the timing for the synchronous external master access controlled by the GPCM.

Figure 20. Synchronous External Master Access Timing (GPCM Handled ACS = 00)

Figure 21 provides the timing for the asynchronous external master memory access controlled by the GPCM.





Figure 22 provides the timing for the asynchronous external master control signals negation.



Figure 22. Asynchronous External Master—Control Signals Negation Timing



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Table 8 provides interrupt timing for the MPC860.

Table 8. Interrupt Timing

Num	Characteristic1	All Freq	Unit	
Num	Characteristic	Min	Мах	Unit
139	IRQx valid to CLKOUT rising edge (setup time)	6.00	_	ns
140	IRQx hold time after CLKOUT	2.00	_	ns
141	IRQx pulse width low	3.00	—	ns
142	IRQx pulse width high	3.00	_	ns
143	IRQx edge-to-edge time	$4 \times T_{CLOCKOUT}$	—	—

The timings I39 and I40 describe the testing conditions under which the IRQ lines are tested when being defined as level-sensitive. The IRQ lines are synchronized internally and do not have to be asserted or negated with reference to the CLKOUT.

The timings I41, I42, and I43 are specified to allow the correct function of the IRQ lines detection circuitry and have no direct relation with the total system interrupt latency that the MPC860 is able to support.

Figure 23 provides the interrupt detection timing for the external level-sensitive lines.



Figure 23. Interrupt Detection Timing for External Level Sensitive Lines

Figure 24 provides the interrupt detection timing for the external edge-sensitive lines.



Figure 24. Interrupt Detection Timing for External Edge Sensitive Lines



Table 9 shows the PCMCIA timing for the MPC860.

Table 9. PCMCIA Timing

Num	Obevectovictic	33	MHz	40 MHz		50 MHz		66 MHz		Unit
Num	Characteristic	Min	Max	Min	Max	Min	Max	Min	Max	Unit
P44	A(0:31), REG valid to PCMCIA Strobe asserted ¹	20.73	—	16.75	—	13.00	—	9.36	—	ns
P45	A(0:31), $\overline{\text{REG}}$ valid to ALE negation ¹	28.30	—	23.00	—	18.00	—	13.15	_	ns
P46	CLKOUT to REG valid	7.58	15.58	6.25	14.25	5.00	13.00	3.79	11.84	ns
P47	CLKOUT to REG invalid	8.58	—	7.25	—	6.00	—	4.84	_	ns
P48	CLKOUT to $\overline{CE1}$, $\overline{CE2}$ asserted	7.58	15.58	6.25	14.25	5.00	13.00	3.79	11.84	ns
P49	CLKOUT to $\overline{CE1}$, $\overline{CE2}$ negated	7.58	15.58	6.25	14.25	5.00	13.00	3.79	11.84	ns
P50	CLKOUT to PCOE, IORD, PCWE, IOWR assert time	—	11.00		11.00	—	11.00	—	11.00	ns
P51	CLKOUT to PCOE, IORD, PCWE, IOWR negate time	2.00	11.00	2.00	11.00	2.00	11.00	2.00	11.00	ns
P52	CLKOUT to ALE assert time	7.58	15.58	6.25	14.25	5.00	13.00	3.79	10.04	ns
P53	CLKOUT to ALE negate time	—	15.58		14.25	_	13.00	—	11.84	ns
P54	PCWE, IOWR negated to D(0:31) invalid ¹	5.58	—	4.25	—	3.00	—	1.79	_	ns
P55	WAITA and WAITB valid to CLKOUT rising edge ¹	8.00	—	8.00	—	8.00	—	8.00	—	ns
P56	CLKOUT rising edge to WAITA and WAITB invalid ¹	2.00	—	2.00	—	2.00	—	2.00	—	ns

¹ PSST = 1. Otherwise add PSST times cycle time.

PSHT = 0. Otherwise add PSHT times cycle time.

These synchronous timings define when the WAITx signals are detected in order to freeze (or relieve) the PCMCIA current cycle. The WAITx assertion will be effective only if it is detected 2 cycles before the PSL timer expiration. See Chapter 16, "PCMCIA Interface," in the *MPC860 PowerQUICCTM Family User's Manual*.







Figure 26. PCMCIA Access Cycle Timing External Bus Write

Figure 27 provides the PCMCIA \overline{WAIT} signal detection timing.



Figure 27. PCMCIA WAIT Signal Detection Timing



Table 10 shows the PCMCIA port timing for the MPC860.

Table 10. PCMCIA Port Timing

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
Num	Characteristic	Min	Max	Min	Max	Min	Max	Min	Max	Unit
P57	CLKOUT to OPx valid	—	19.00	_	19.00	_	19.00	_	19.00	ns
P58	HRESET negated to OPx drive ¹	25.73		21.75		18.00		14.36	_	ns
P59	IP_Xx valid to CLKOUT rising edge	5.00		5.00		5.00		5.00	_	ns
P60	CLKOUT rising edge to IP_Xx invalid	1.00		1.00		1.00		1.00	-	ns

¹ OP2 and OP3 only.

Figure 28 provides the PCMCIA output port timing for the MPC860.



Figure 28. PCMCIA Output Port Timing

Figure 29 provides the PCMCIA output port timing for the MPC860.



Figure 29. PCMCIA Input Port Timing



11 CPM Electrical Characteristics

This section provides the AC and DC electrical specifications for the communications processor module (CPM) of the MPC860.

11.1 PIP/PIO AC Electrical Specifications

Table 14 provides the PIP/PIO AC timings as shown in Figure 39 through Figure 43.

Table 14. PIP/PIO Timing

Num	Characteristic	All Freq	uencies	Unit
Num	Onardetensite	Min	Max	Onit
21	Data-in setup time to STBI low	0	_	ns
22	Data-in hold time to STBI high	2.5 – t3 ¹	_	CLK
23	STBI pulse width	1.5	_	CLK
24	STBO pulse width	1 CLK – 5 ns	_	ns
25	Data-out setup time to STBO low	2	_	CLK
26	Data-out hold time from STBO high	5	_	CLK
27	STBI low to STBO low (Rx interlock)	_	2	CLK
28	STBI low to STBO high (Tx interlock)	2	_	CLK
29	Data-in setup time to clock high	15	_	ns
30	Data-in hold time from clock high	7.5	_	ns
31	Clock low to data-out valid (CPU writes data, control, or direction)		25	ns

¹ t3 = Specification 23.



Figure 39. PIP Rx (Interlock Mode) Timing Diagram



Num	Charactariatia	All Freq	Unit	
Num	Characteristic	Min	Мах	Unit
42	SDACK assertion delay from clock high	—	12	ns
43	SDACK negation delay from clock low	—	12	ns
44	SDACK negation delay from TA low	—	20	ns
45	SDACK negation delay from clock high	_	15	ns
46	\overline{TA} assertion to rising edge of the clock setup time (applies to external \overline{TA})	7		ns

Table 16. IDMA Controller Timing (continued)



Figure 45. IDMA External Requests Timing Diagram



Figure 46. SDACK Timing Diagram—Peripheral Write, Externally-Generated TA





Figure 47. SDACK Timing Diagram—Peripheral Write, Internally-Generated TA



Figure 48. SDACK Timing Diagram—Peripheral Read, Internally-Generated TA



11.4 Baud Rate Generator AC Electrical Specifications

Table 17 provides the baud rate generator timings as shown in Figure 49.

Table 17. Baud Rate Generator Timing

Num	Charactariatia	All Freq	Unit	
Nulli	Characteristic	Min	Мах	Unit
50	BRGO rise and fall time	—	10	ns
51	BRGO duty cycle	40	60	%
52	BRGO cycle	40	—	ns



Figure 49. Baud Rate Generator Timing Diagram

11.5 Timer AC Electrical Specifications

Table 18 provides the general-purpose timer timings as shown in Figure 50.

Table 18. Timer Timing

Num	Characteristic	All Freq	Unit		
Num	Characteristic	Min Max			
61	TIN/TGATE rise and fall time	10	—	ns	
62	TIN/TGATE low time	1	—	CLK	
63	TIN/TGATE high time	2	—	CLK	
64	TIN/TGATE cycle time	3	—	CLK	
65	CLKO low to TOUT valid	3	25	ns	



CPM Electrical Characteristics













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Figure 56 through Figure 58 show the NMSI timings.









Figure 58. HDLC Bus Timing Diagram

11.8 Ethernet Electrical Specifications

Table 22 provides the Ethernet timings as shown in Figure 59 through Figure 63.

Num	Characteristic	All Frequencies		
		Min	Мах	Unit
120	CLSN width high	40		ns
121	RCLK1 rise/fall time	—	15	ns
122	RCLK1 width low	40	—	ns
123	RCLK1 clock period ¹	80	120	ns
124	RXD1 setup time	20	—	ns
125	RXD1 hold time	5	—	ns
126	RENA active delay (from RCLK1 rising edge of the last data bit)	10	—	ns
127	RENA width low	100	—	ns
128	TCLK1 rise/fall time	—	15	ns
129	TCLK1 width low	40	—	ns
130	TCLK1 clock period ¹	99	101	ns
131	TXD1 active delay (from TCLK1 rising edge)	10	50	ns
132	TXD1 inactive delay (from TCLK1 rising edge)	10	50	ns
133	TENA active delay (from TCLK1 rising edge)	10	50	ns
134	TENA inactive delay (from TCLK1 rising edge)	10	50	ns



Num	Characteristic	All Frequencies		Unit
		Min	Мах	Unit
135	RSTRT active delay (from TCLK1 falling edge)	10	50	ns
136	RSTRT inactive delay (from TCLK1 falling edge)	10	50	ns
137	REJECT width low	1	—	CLK
138	CLKO1 low to SDACK asserted ²	_	20	ns
139	CLKO1 low to SDACK negated ²	—	20	ns

Table 22. Ethernet Timing (continued)

¹ The ratios SYNCCLK/RCLK1 and SYNCCLK/TCLK1 must be greater than or equal to 2/1.

² SDACK is asserted whenever the SDMA writes the incoming frame DA into memory.



Figure 59. Ethernet Collision Timing Diagram



Figure 60. Ethernet Receive Timing Diagram



SMC Transparent AC Electrical Specifications 11.9

Table 23 provides the SMC transparent timings as shown in Figure 64.

Table 23. SMC Transparent Timing

Num	Characteristic	All Frequencies		11
		Min	Мах	Unit
150	SMCLK clock period ¹	100	—	ns
151	SMCLK width low	50	—	ns
151A	SMCLK width high	50	—	ns
152	SMCLK rise/fall time	—	15	ns
153	SMTXD active delay (from SMCLK falling edge)	10	50	ns
154	SMRXD/SMSYNC setup time	20	—	ns
155	RXD1/SMSYNC hold time	5	_	ns

¹ SYNCCLK must be at least twice as fast as SMCLK.



Note: 1. This delay is equal to an integer number of character-length clocks.

