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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	80MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (2), 10/100Mbps (1)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 95°C (TA)
Security Features	-
Package / Case	357-BBGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc860dtvr80d4

1 Overview

The MPC860 power quad integrated communications controller (PowerQUICC™) is a versatile one-chip integrated microprocessor and peripheral combination designed for a variety of controller applications. It particularly excels in communications and networking systems. The PowerQUICC unit is referred to as the MPC860 in this hardware specification.

The MPC860 implements Power Architecture™ technology and contains a superset of Freescale's MC68360 quad integrated communications controller (QUICC), referred to here as the QUICC, RISC communications proccessor module (CPM). The CPU on the MPC860 is a 32-bit core built on Power Architecture technology that incorporates memory management units (MMUs) and instruction and data caches.. The CPM from the MC68360 QUICC has been enhanced by the addition of the inter-integrated controller (I^2C) channel. The memory controller has been enhanced, enabling the MPC860 to support any type of memory, including high-performance memories and new types of DRAMs. A PCMCIA socket controller supports up to two sockets. A real-time clock has also been integrated.

Table 1 shows the functionality supported by the MPC860 family.

Table 1. MPC860 Family Functionality

Part	Cache (Kbytes)		Ethernet		ATM	SCC	Reference[1]
	Instruction Cache	Data Cache	10T	10/100			
MPC860DE	4	4	Up to 2	—	—	2	1
MPC860DT	4	4	Up to 2	1	Yes	2	1
MPC860DP	16	8	Up to 2	1	Yes	2	1
MPC860EN	4	4	Up to 4	—	—	4	1
MPC860SR	4	4	Up to 4	—	Yes	4	1
MPC860T	4	4	Up to 4	1	Yes	4	1
MPC860P	16	8	Up to 4	1	Yes	4	1
MPC855T	4	4	1	1	Yes	1	2

[1] Supporting documentation for these devices refers to the following:
1. MPC860 PowerQUICC Family User's Manual (MPC860UM, Rev. 3)
2. MPC855T User's Manual (MPC855TUM, Rev. 1)

- System integration unit (SIU)
  - Bus monitor
  - Software watchdog
  - Periodic interrupt timer (PIT)
  - Low-power stop mode
  - Clock synthesizer
  - Decrementer, time base, and real-time clock (RTC)
  - Reset controller
  - IEEE 1149.1™ Std. test access port (JTAG)
- Interrupts
  - Seven external interrupt request (IRQ) lines
  - 12 port pins with interrupt capability
  - 23 internal interrupt sources
  - Programmable priority between SCCs
  - Programmable highest priority request
- 10/100 Mbps Ethernet support, fully compliant with the IEEE 802.3u® Standard (not available when using ATM over UTOPIA interface)
- ATM support compliant with ATM forum UNI 4.0 specification
  - Cell processing up to 50–70 Mbps at 50-MHz system clock
  - Cell multiplexing/demultiplexing
  - Support of AAL5 and AAL0 protocols on a per-VC basis. AAL0 support enables OAM and software implementation of other protocols.
  - ATM pace control (APC) scheduler, providing direct support for constant bit rate (CBR) and unspecified bit rate (UBR) and providing control mechanisms enabling software support of available bit rate (ABR)
  - Physical interface support for UTOPIA (10/100-Mbps is not supported with this interface) and byte-aligned serial (for example, T1/E1/ADSL)
  - UTOPIA-mode ATM supports level-1 master with cell-level handshake, multi-PHY (up to four physical layer devices), connection to 25-, 51-, or 155-Mbps framers, and UTOPIA/system clock ratios of 1/2 or 1/3.
  - Serial-mode ATM connection supports transmission convergence (TC) function for T1/E1/ADSL lines, cell delineation, cell payload scrambling/descrambling, automatic idle/unassigned cell insertion/stripping, header error control (HEC) generation, checking, and statistics.
- Communications processor module (CPM)
  - RISC communications processor (CP)
  - Communication-specific commands (for example, GRACEFUL STOP TRANSMIT, ENTER HUNT MODE, and RESTART TRANSMIT)
  - Supports continuous mode transmission and reception on all serial channels

Table 4 shows the thermal characteristics for the MPC860.

Table 4. MPC860 Thermal Resistance Data

Rating	Environment		Symbol	ZP MPC860P	ZQ / VR MPC860P	Unit
Mold Compound Thickness				0.85	1.15	mm
Junction-to-ambient [1]	Natural convection	Single-layer board (1s)	$R_{\theta JA}$ [2]	34	34	°C/W
		Four-layer board (2s2p)	$R_{\theta JMA}$ [3]	22	22	
	Airflow (200 ft/min)	Single-layer board (1s)	$R_{\theta JMA}$ [3]	27	27	
		Four-layer board (2s2p)	$R_{\theta JMA}$ [3]	18	18	
Junction-to-board [4]			$R_{\theta JB}$	14	13	
Junction-to-case [5]			$R_{\theta JC}$	6	8	
Junction-to-package top [6]	Natural convection		Ψ_{JT}	2	2	

1 Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.
2 Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.
3 Per JEDEC JESD51-6 with the board horizontal.
4 Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5 Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature. For exposed pad packages where the pad would be expected to be soldered, junction-to-case thermal resistance is a simulated value from the junction to the exposed pad without contact resistance.
6 Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2.

Table 7. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B23	CLKOUT rising edge to $\overline{CS}$ negated GPCM read access, GPCM write access ACS = 00, TRLX = 0, and CSNT = 0	2.00	8.00	2.00	8.00	2.00	8.00	2.00	8.00	ns
B24	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 0	5.58	—	4.25	—	3.00	—	1.79	—	ns
B24a	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 0	13.15	—	10.50	—	8.00	—	5.58	—	ns
B25	CLKOUT rising edge to $\overline{OE}$, $\overline{WE}$(0:3) asserted	—	9.00	—	9.00	—	9.00	—	9.00	ns
B26	CLKOUT rising edge to $\overline{OE}$ negated	2.00	9.00	2.00	9.00	2.00	9.00	2.00	9.00	ns
B27	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 1	35.88	—	29.25	—	23.00	—	16.94	—	ns
B27a	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 1	43.45	—	35.50	—	28.00	—	20.73	—	ns
B28	CLKOUT rising edge to $\overline{WE}$(0:3) negated GPCM write access CSNT = 0	—	9.00	—	9.00	—	9.00	—	9.00	ns
B28a	CLKOUT falling edge to $\overline{WE}$(0:3) negated GPCM write access TRLX = 0, 1, CSNT = 1, EBDF = 0	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.54	ns
B28b	CLKOUT falling edge to $\overline{CS}$ negated GPCM write access TRLX = 0, 1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 0	—	14.33	—	13.00	—	11.75	—	10.54	ns
B28c	CLKOUT falling edge to $\overline{WE}$(0:3) negated GPCM write access TRLX = 0, 1, CSNT = 1 write access TRLX = 0, CSNT = 1, EBDF = 1	10.86	17.99	8.88	16.00	7.00	14.13	5.18	12.31	ns
B28d	CLKOUT falling edge to $\overline{CS}$ negated GPCM write access TRLX = 0, 1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 1	—	17.99	—	16.00	—	14.13	—	12.31	ns
B29	$\overline{WE}$(0:3) negated to D(0:31), DP(0:3) High-Z GPCM write access CSNT = 0, EBDF = 0	5.58	—	4.25	—	3.00	—	1.79	—	ns
B29a	$\overline{WE}$(0:3) negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 0	13.15	—	10.5	—	8.00	—	5.58	—	ns
B29b	$\overline{CS}$ negated to D(0:31), DP(0:3), High-Z GPCM write access, ACS = 00, TRLX = 0, 1, and CSNT = 0	5.58	—	4.25	—	3.00	—	1.79	—	ns
B29c	$\overline{CS}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 0	13.15	—	10.5	—	8.00	—	5.58	—	ns

Table 7. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B35	A(0:31), BADDR(28:30) to $\overline{CS}$ valid—as requested by control bit BST4 in the corresponding word in UPM	5.58	—	4.25	—	3.00	—	1.79	—	ns
B35a	A(0:31), BADDR(28:30), and D(0:31) to $\overline{BS}$ valid—as requested by control bit BST1 in the corresponding word in UPM	13.15	—	10.50	—	8.00	—	5.58	—	ns
B35b	A(0:31), BADDR(28:30), and D(0:31) to $\overline{BS}$ valid—as requested by control bit BST2 in the corresponding word in UPM	20.73	—	16.75	—	13.00	—	9.36	—	ns
B36	A(0:31), BADDR(28:30), and D(0:31) to $\overline{GPL}$ valid—as requested by control bit GxT4 in the corresponding word in UPM	5.58	—	4.25	—	3.00	—	1.79	—	ns
B37	UPWAIT valid to CLKOUT falling edge[9]	6.00	—	6.00	—	6.00	—	6.00	—	ns
B38	CLKOUT falling edge to UPWAIT valid[9]	1.00	—	1.00	—	1.00	—	1.00	—	ns
B39	$\overline{AS}$ valid to CLKOUT rising edge[10]	7.00	—	7.00	—	7.00	—	7.00	—	ns
B40	A(0:31), TSIZ(0:1), RD/$\overline{WR}$, $\overline{BURST}$, valid to CLKOUT rising edge	7.00	—	7.00	—	7.00	—	7.00	—	ns
B41	$\overline{TS}$ valid to CLKOUT rising edge (setup time)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B42	CLKOUT rising edge to $\overline{TS}$ valid (hold time)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B43	$\overline{AS}$ negation to memory controller signals negation	—	TBD	—	TBD	—	TBD	—	TBD	ns

1 Phase and frequency jitter performance results are only valid if the input jitter is less than the prescribed value.

2 If the rate of change of the frequency of EXTAL is slow (that is, it does not jump between the minimum and maximum values in one cycle) or the frequency of the jitter is fast (that is, it does not stay at an extreme value for a long time) then the maximum allowed jitter on EXTAL can be up to 2%.

3 The timings specified in B4 and B5 are based on full strength clock.

4 The timing for $\overline{BR}$ output is relevant when the MPC860 is selected to work with external bus arbiter. The timing for $\overline{BG}$ output is relevant when the MPC860 is selected to work with internal bus arbiter.

5 The timing required for $\overline{BR}$ input is relevant when the MPC860 is selected to work with internal bus arbiter. The timing for $\overline{BG}$ input is relevant when the MPC860 is selected to work with external bus arbiter.

6 The D(0:31) and DP(0:3) input timings B18 and B19 refer to the rising edge of the CLKOUT in which the $\overline{TA}$ input signal is asserted.

7 The D(0:31) and DP(0:3) input timings B20 and B21 refer to the falling edge of the CLKOUT. This timing is valid only for read accesses controlled by chip-selects under control of the UPM in the memory controller, for data beats where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

8 The timing B30 refers to $\overline{CS}$ when ACS = 00 and to $\overline{WE}$(0:3) when CSNT = 0.

9 The signal UPWAIT is considered asynchronous to the CLKOUT and synchronized internally. The timings specified in B37 and B38 are specified to enable the freeze of the UPM output signals as described in Figure 18.

10 The $\overline{AS}$ signal is considered asynchronous to the CLKOUT. The timing B39 is specified in order to allow the behavior specified in Figure 21.

Figure 3 is the control timing diagram.

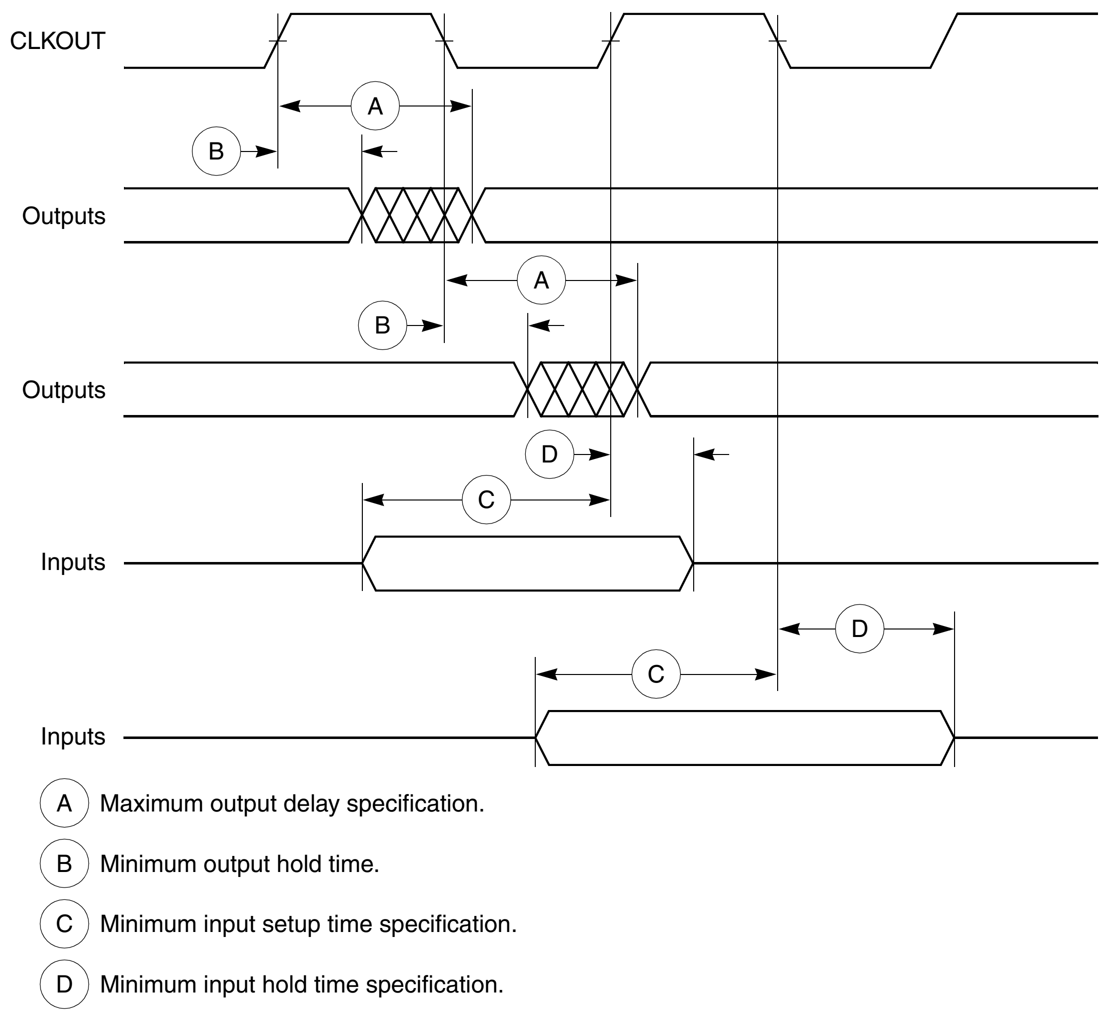


Figure 3. Control Timing

Figure 4 provides the timing for the external clock.

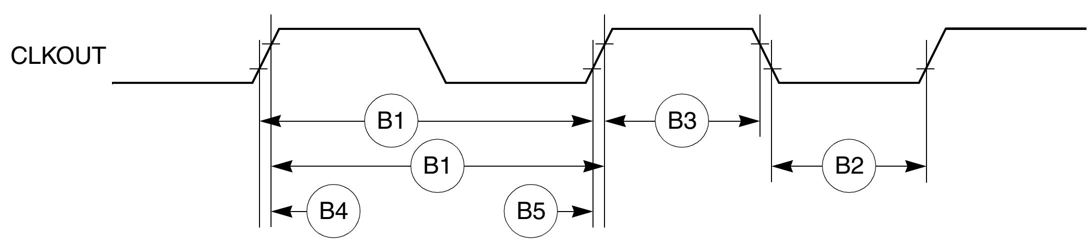


Figure 4. External Clock Timing

Figure 14 through Figure 16 provide the timing for the external bus write controlled by various GPCM factors.

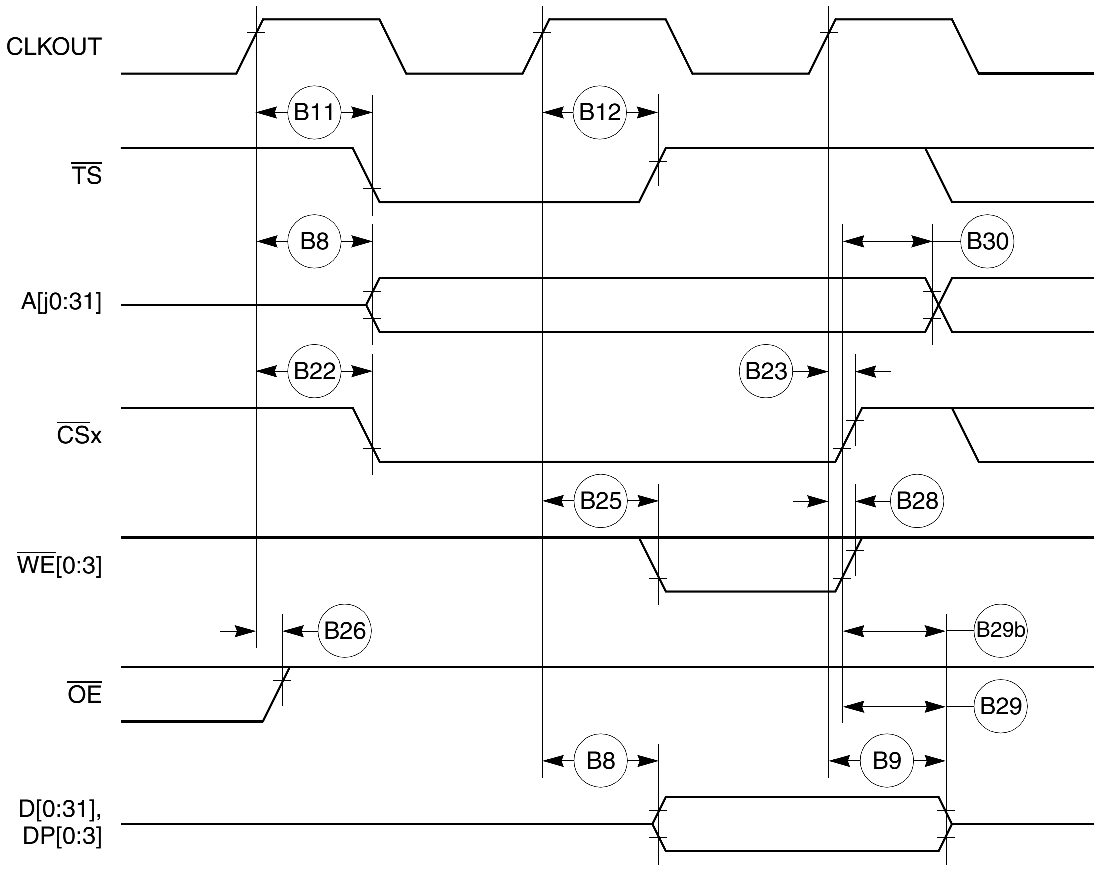


Figure 14. External Bus Write Timing (GPCM Controlled—TRLX = 0 or 1, CSNT = 0)

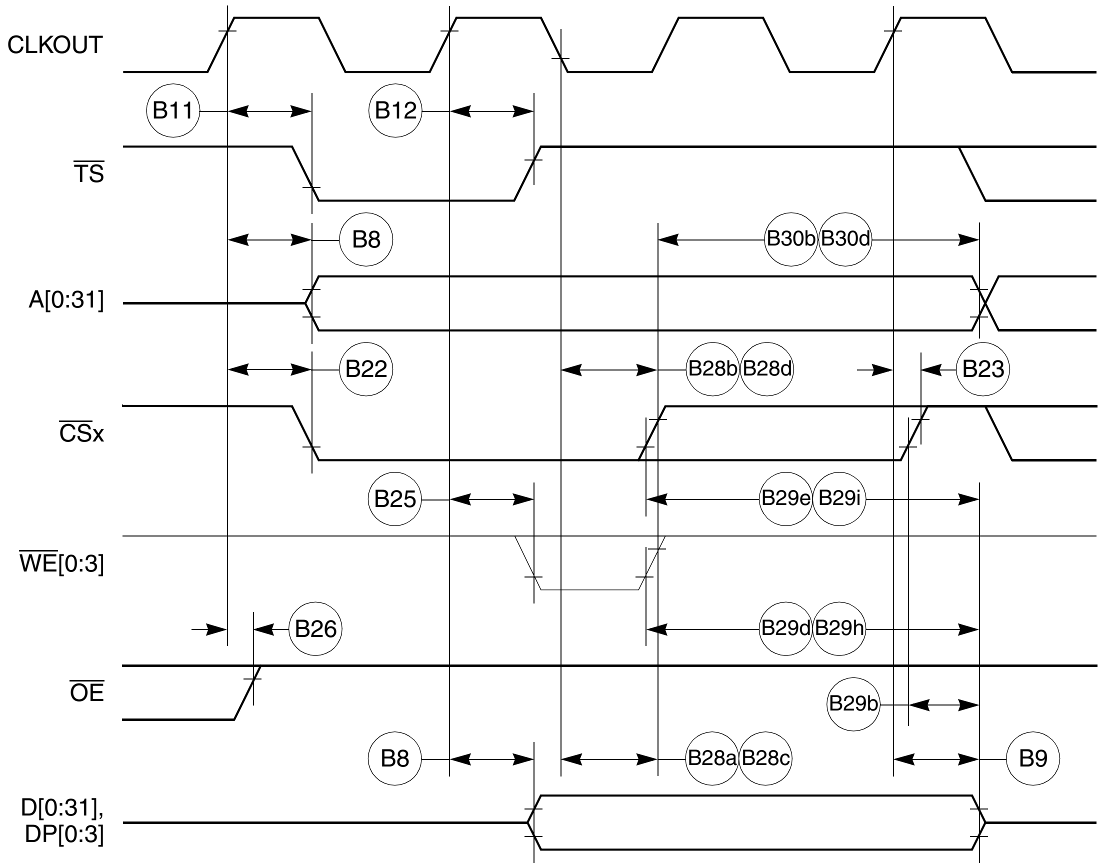


Figure 16. External Bus Write Timing (GPCM Controlled—TRLX = 0 or 1, CSNT = 1)

Figure 17 provides the timing for the external bus controlled by the UPM.

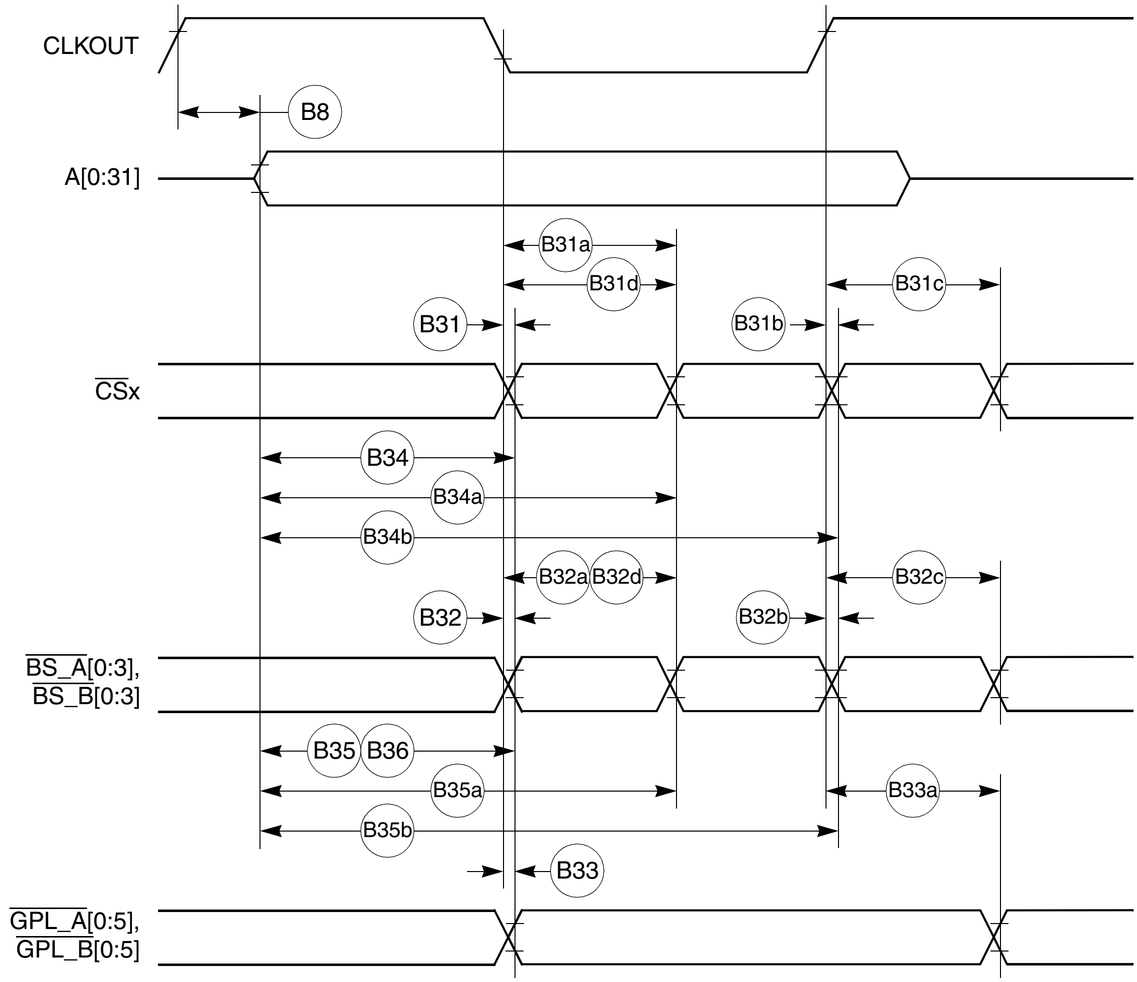


Figure 17. External Bus Timing (UPM Controlled Signals)

Figure 20 provides the timing for the synchronous external master access controlled by the GPCM.

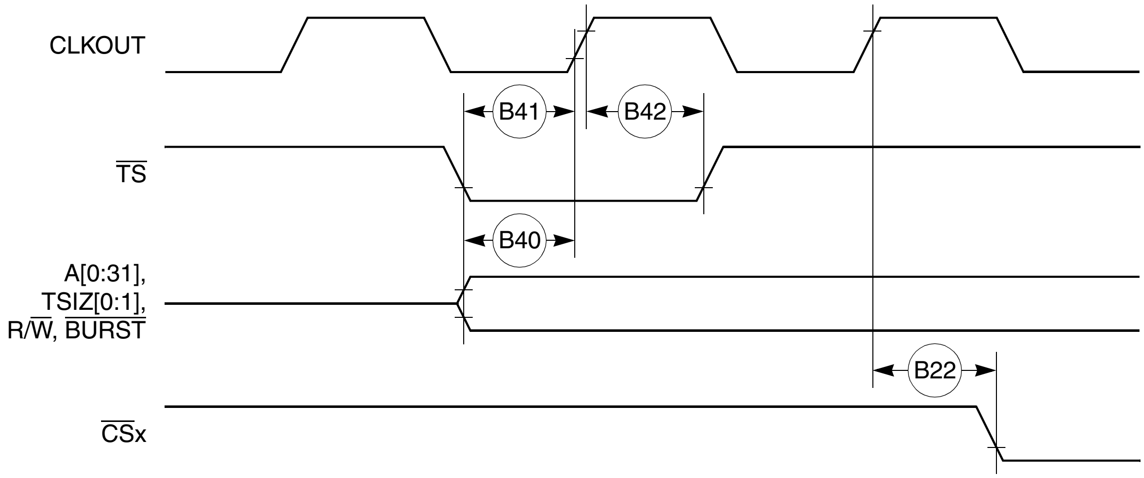


Figure 20. Synchronous External Master Access Timing (GPCM Handled ACS = 00)

Figure 21 provides the timing for the asynchronous external master memory access controlled by the GPCM.

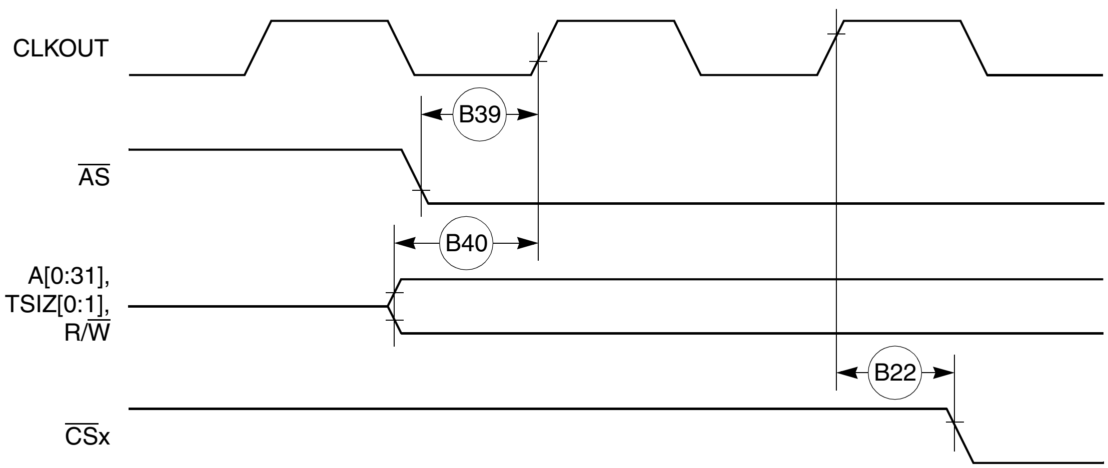


Figure 21. Asynchronous External Master Memory Access Timing (GPCM Controlled—ACS = 00)

Figure 22 provides the timing for the asynchronous external master control signals negation.

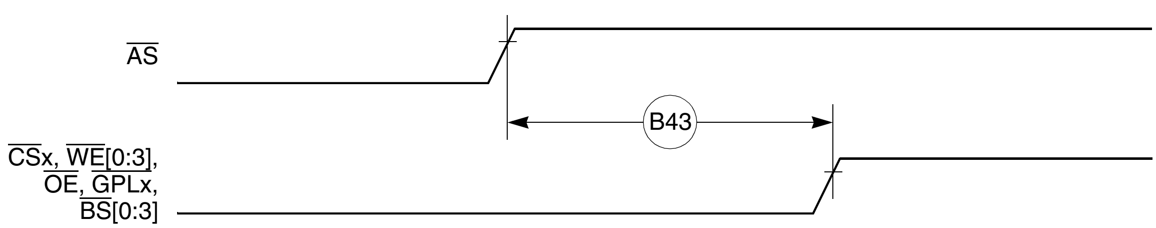


Figure 22. Asynchronous External Master—Control Signals Negation Timing

Table 8 provides interrupt timing for the MPC860.

Table 8. Interrupt Timing

Num	Characteristic[1]	All Frequencies		Unit
		Min	Max	
I39	$\overline{\text{IRQ}}$x valid to CLKOUT rising edge (setup time)	6.00	—	ns
I40	$\overline{\text{IRQ}}$x hold time after CLKOUT	2.00	—	ns
I41	$\overline{\text{IRQ}}$x pulse width low	3.00	—	ns
I42	$\overline{\text{IRQ}}$x pulse width high	3.00	—	ns
I43	$\overline{\text{IRQ}}$x edge-to-edge time	$4 \times T_{CLOCKOUT}$	—	—

[1] The timings I39 and I40 describe the testing conditions under which the $\overline{\text{IRQ}}$ lines are tested when being defined as level-sensitive. The $\overline{\text{IRQ}}$ lines are synchronized internally and do not have to be asserted or negated with reference to the CLKOUT.
The timings I41, I42, and I43 are specified to allow the correct function of the $\overline{\text{IRQ}}$ lines detection circuitry and have no direct relation with the total system interrupt latency that the MPC860 is able to support.

Figure 23 provides the interrupt detection timing for the external level-sensitive lines.

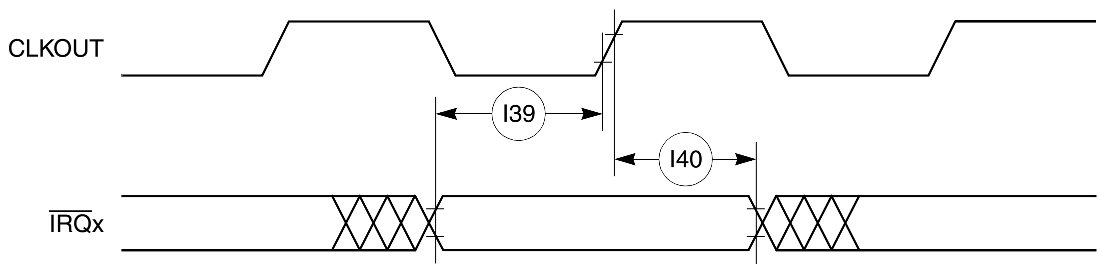


Figure 23. Interrupt Detection Timing for External Level Sensitive Lines

Figure 24 provides the interrupt detection timing for the external edge-sensitive lines.

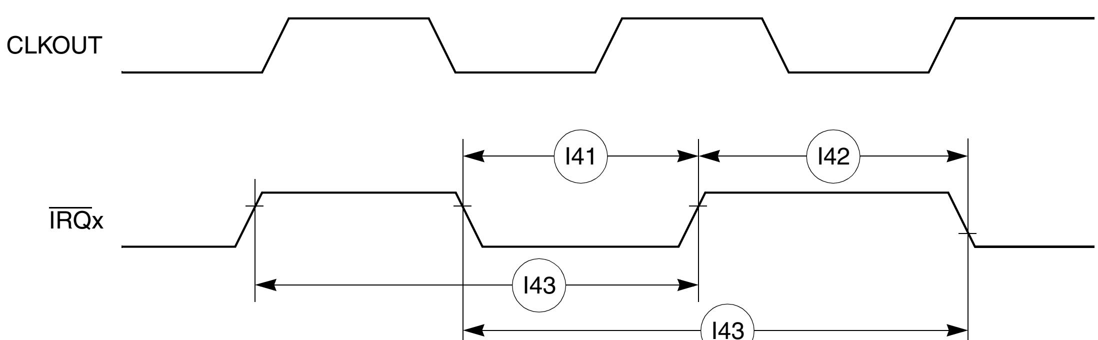


Figure 24. Interrupt Detection Timing for External Edge Sensitive Lines

Table 10 shows the PCMCIA port timing for the MPC860.

Table 10. PCMCIA Port Timing

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
P57	CLKOUT to OPx valid	—	19.00	—	19.00	—	19.00	—	19.00	ns
P58	$\overline{\text{HRESET}}$ negated to OPx drive[1]	25.73	—	21.75	—	18.00	—	14.36	—	ns
P59	IP_Xx valid to CLKOUT rising edge	5.00	—	5.00	—	5.00	—	5.00	—	ns
P60	CLKOUT rising edge to IP_Xx invalid	1.00	—	1.00	—	1.00	—	1.00	—	ns

[1] OP2 and OP3 only.

Figure 28 provides the PCMCIA output port timing for the MPC860.

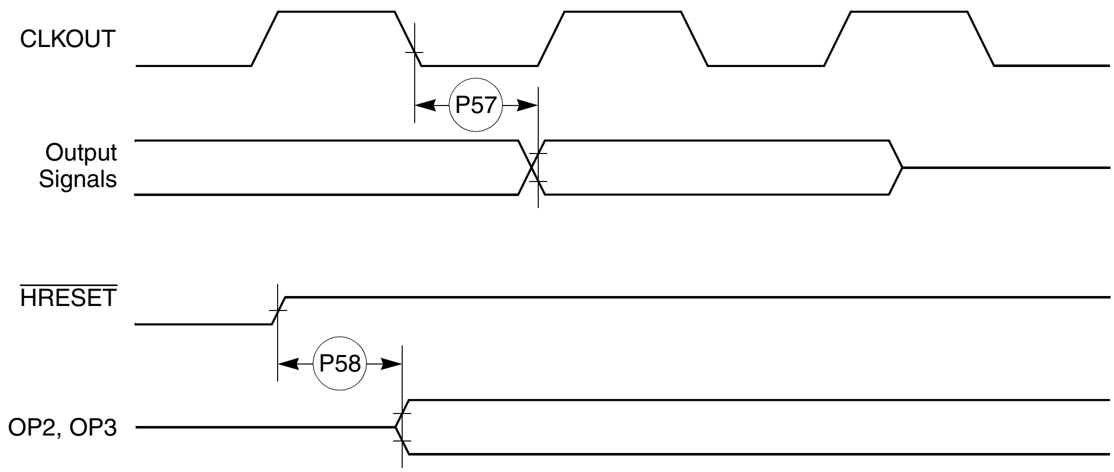


Figure 28. PCMCIA Output Port Timing

Figure 29 provides the PCMCIA output port timing for the MPC860.

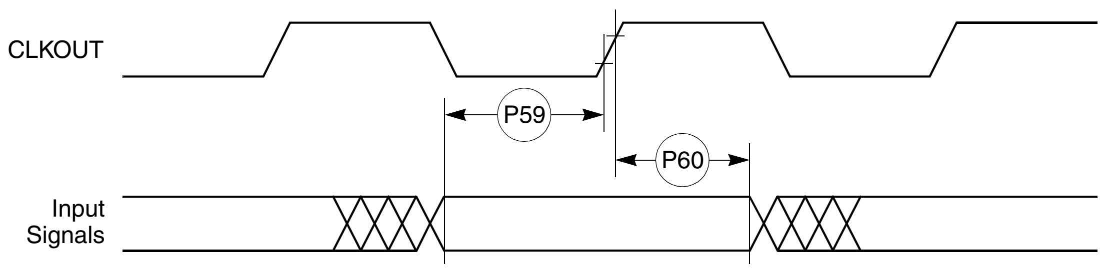


Figure 29. PCMCIA Input Port Timing

11 CPM Electrical Characteristics

This section provides the AC and DC electrical specifications for the communications processor module (CPM) of the MPC860.

11.1 PIP/PIO AC Electrical Specifications

Table 14 provides the PIP/PIO AC timings as shown in Figure 39 through Figure 43.

Table 14. PIP/PIO Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
21	Data-in setup time to STBI low	0	—	ns
22	Data-in hold time to STBI high	2.5 – t3[1]	—	CLK
23	STBI pulse width	1.5	—	CLK
24	STBO pulse width	1 CLK – 5 ns	—	ns
25	Data-out setup time to STBO low	2	—	CLK
26	Data-out hold time from STBO high	5	—	CLK
27	STBI low to STBO low (Rx interlock)	—	2	CLK
28	STBI low to STBO high (Tx interlock)	2	—	CLK
29	Data-in setup time to clock high	15	—	ns
30	Data-in hold time from clock high	7.5	—	ns
31	Clock low to data-out valid (CPU writes data, control, or direction)	—	25	ns

[1] t3 = Specification 23.

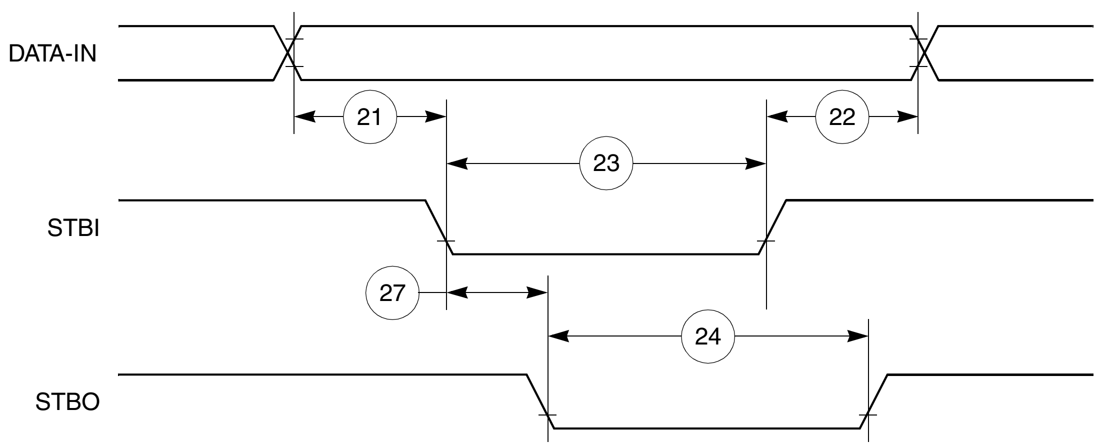


Figure 39. PIP Rx (Interlock Mode) Timing Diagram

Table 16. IDMA Controller Timing (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
42	$\overline{\text{SDACK}}$ assertion delay from clock high	—	12	ns
43	$\overline{\text{SDACK}}$ negation delay from clock low	—	12	ns
44	$\overline{\text{SDACK}}$ negation delay from $\overline{\text{TA}}$ low	—	20	ns
45	$\overline{\text{SDACK}}$ negation delay from clock high	—	15	ns
46	$\overline{\text{TA}}$ assertion to rising edge of the clock setup time (applies to external $\overline{\text{TA}}$)	7	—	ns

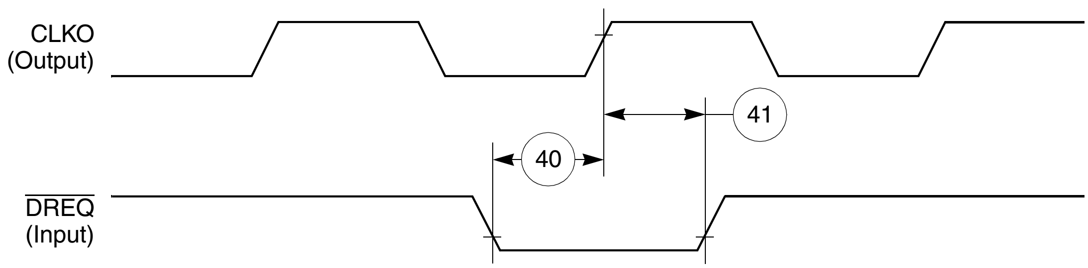


Figure 45. IDMA External Requests Timing Diagram

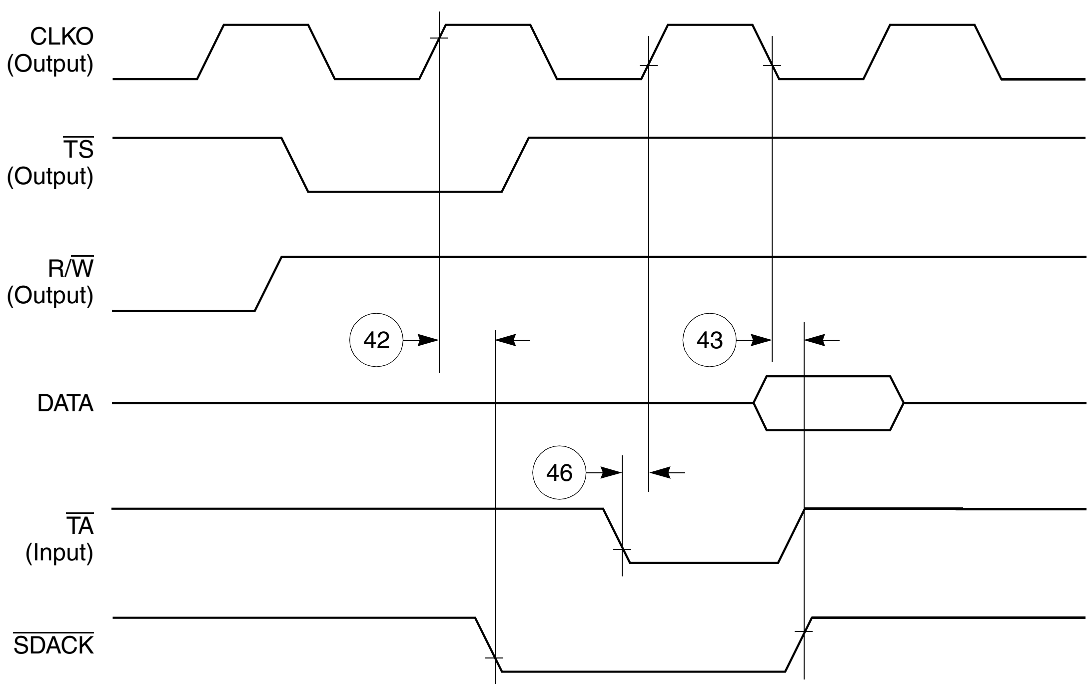


Figure 46. $\overline{\text{SDACK}}$ Timing Diagram—Peripheral Write, Externally-Generated $\overline{\text{TA}}$

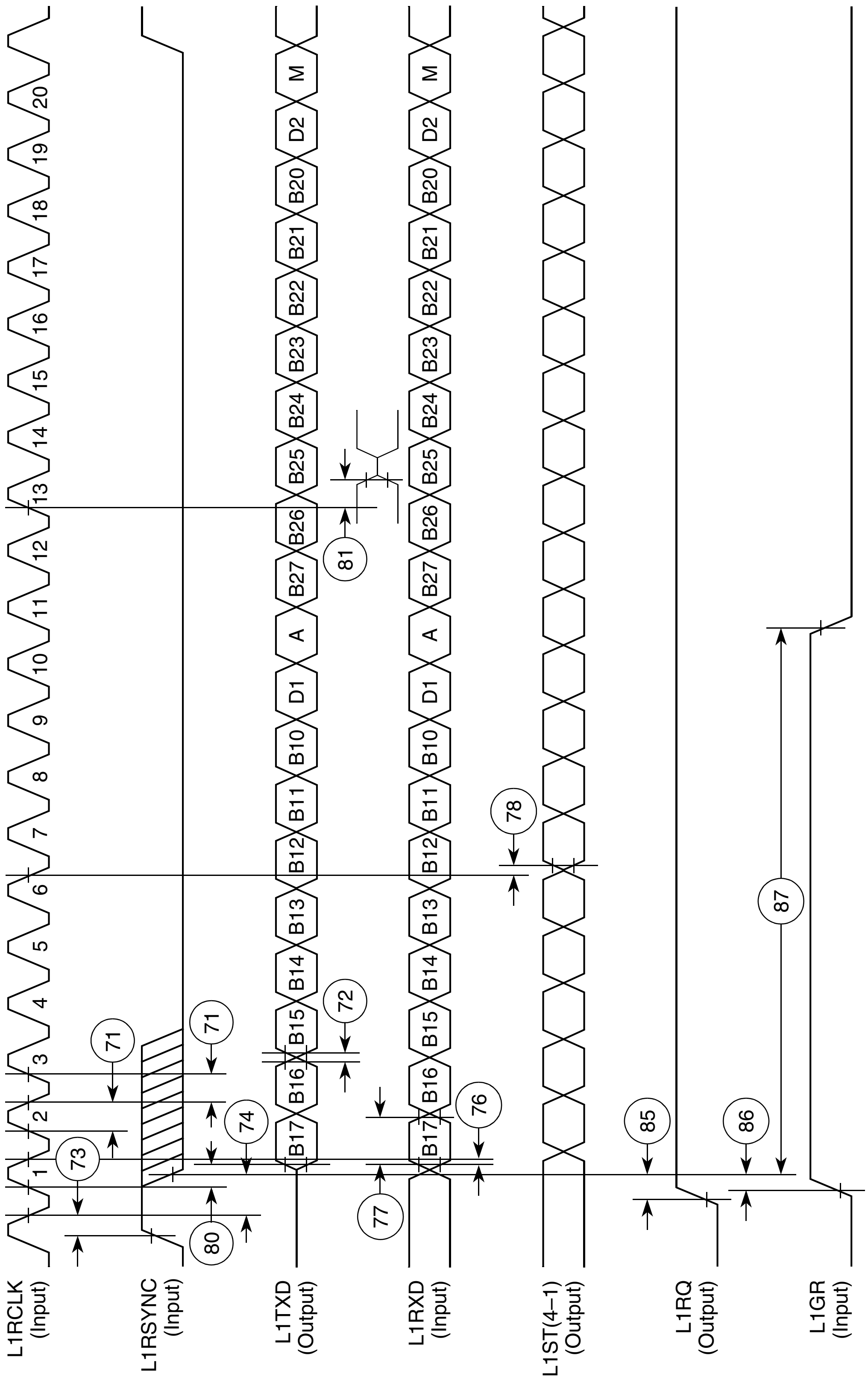


Figure 55. IDL Timing

Figure 56 through Figure 58 show the NMSI timings.

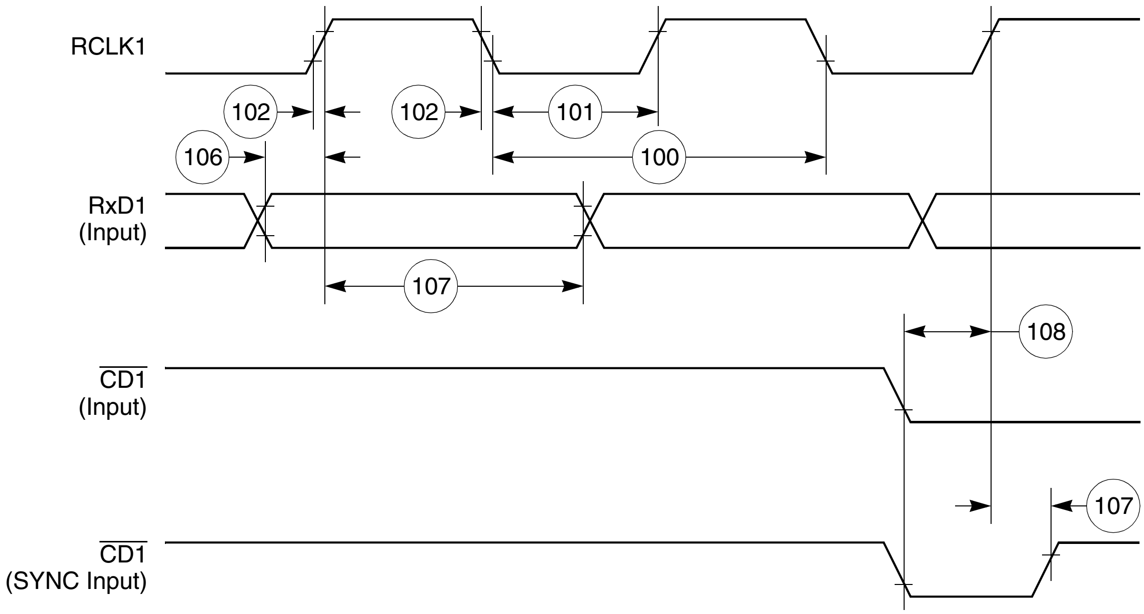


Figure 56. SCC NMSI Receive Timing Diagram

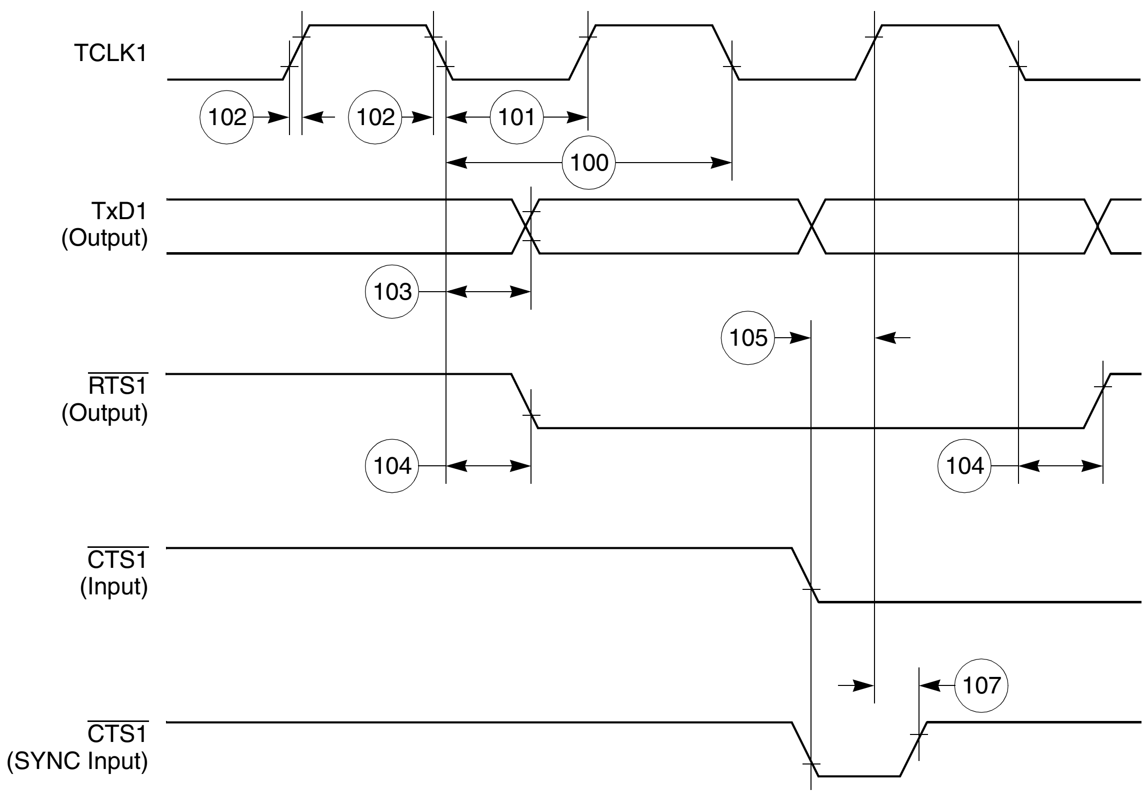


Figure 57. SCC NMSI Transmit Timing Diagram

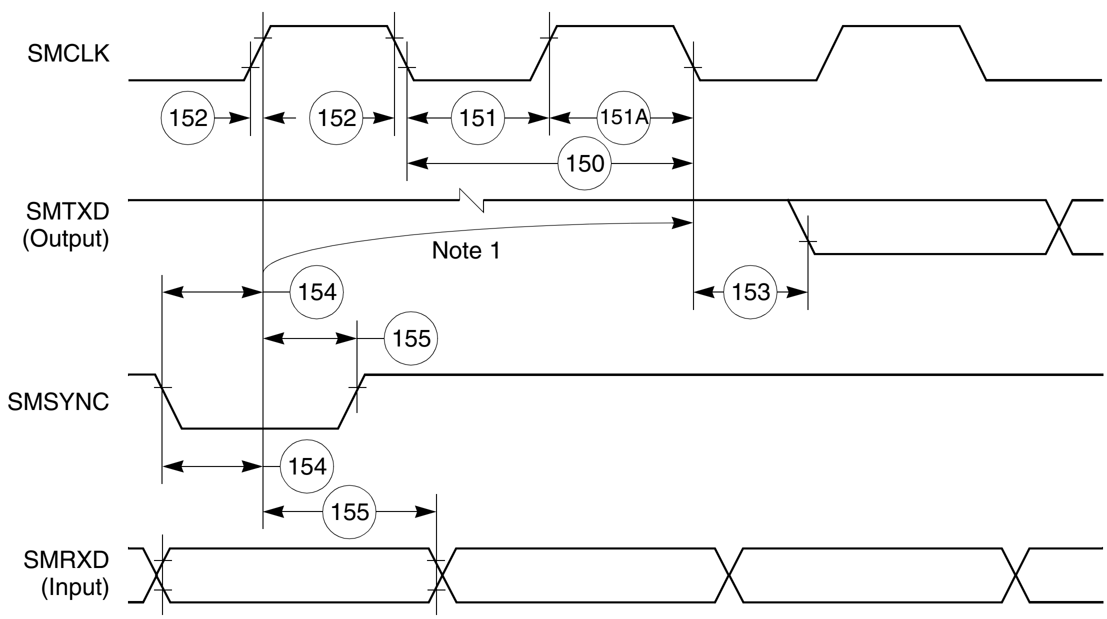
11.9 SMC Transparent AC Electrical Specifications

Table 23 provides the SMC transparent timings as shown in Figure 64.

Table 23. SMC Transparent Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
150	SMCLK clock period[1]	100	—	ns
151	SMCLK width low	50	—	ns
151A	SMCLK width high	50	—	ns
152	SMCLK rise/fall time	—	15	ns
153	SMTXD active delay (from SMCLK falling edge)	10	50	ns
154	SMRXD/SMSYNC setup time	20	—	ns
155	RXD1/SMSYNC hold time	5	—	ns

[1] SYNCCLK must be at least twice as fast as SMCLK.



Note:
1. This delay is equal to an integer number of character-length clocks.

Figure 64. SMC Transparent Timing Diagram

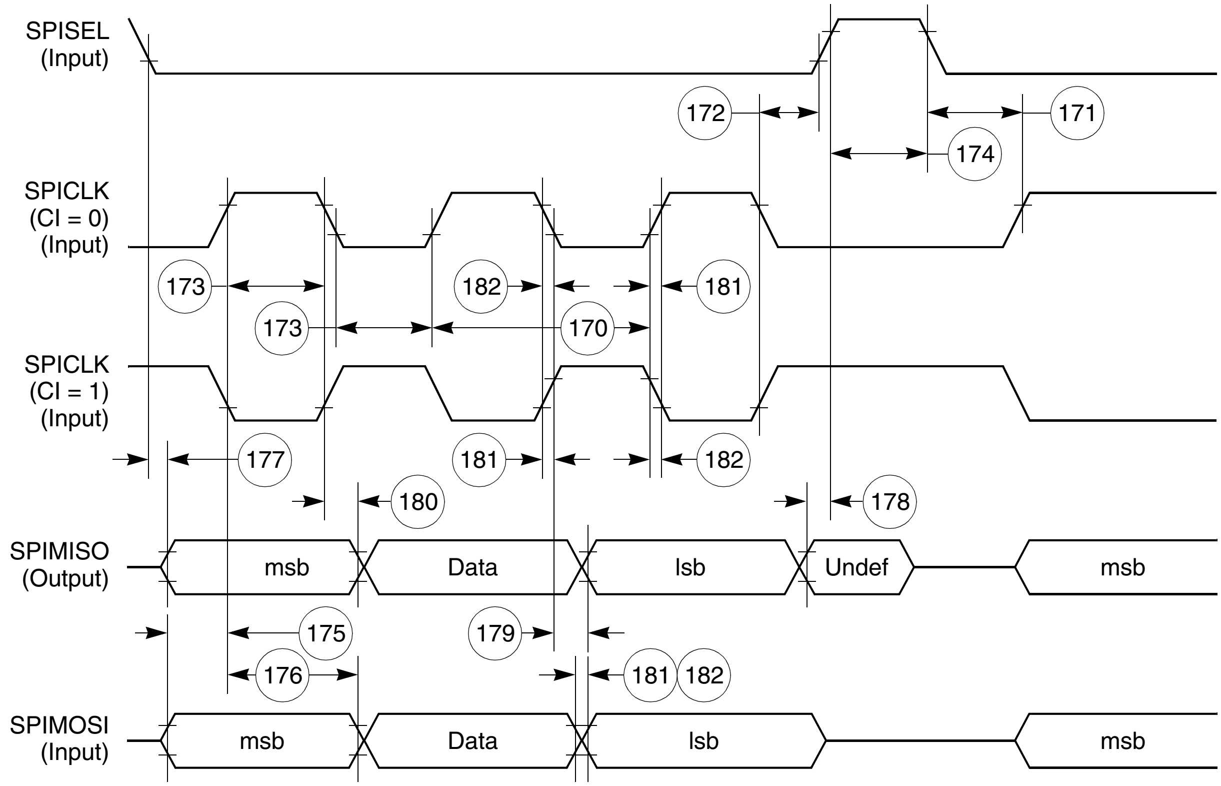


Figure 67. SPI Slave (CP = 0) Timing Diagram

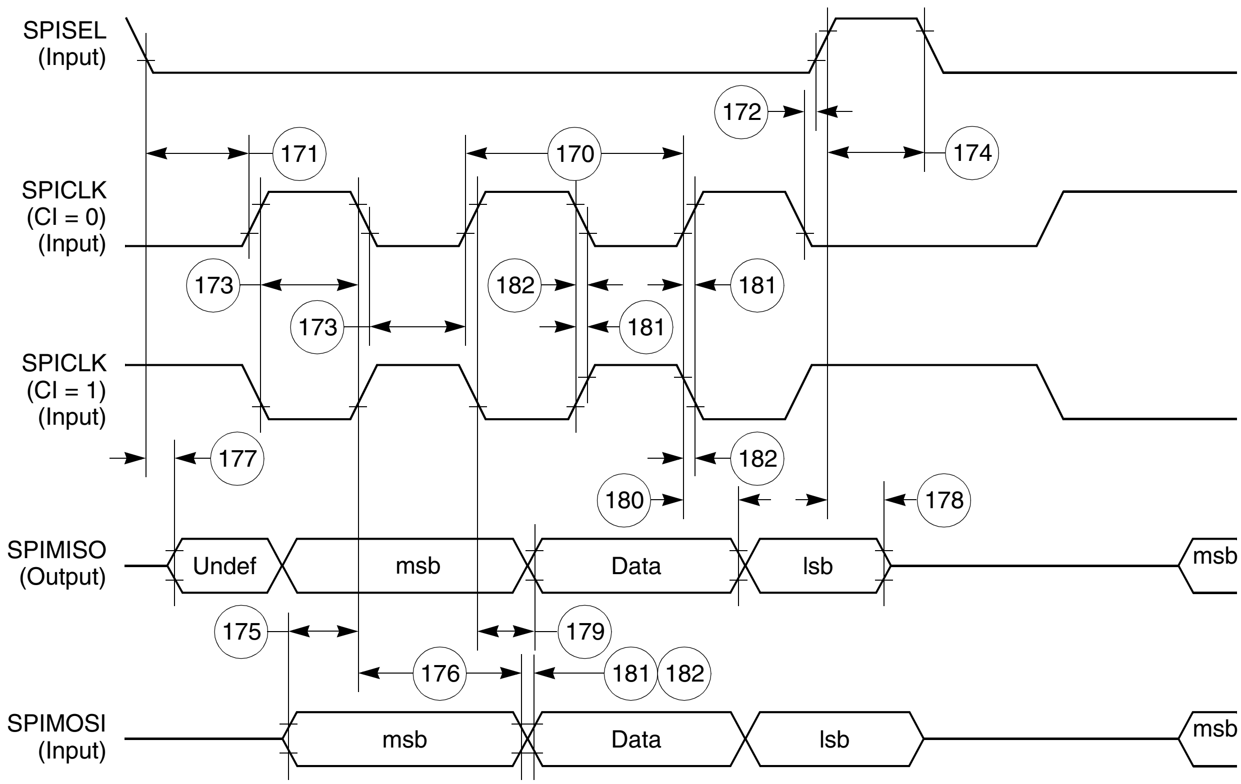


Figure 68. SPI Slave (CP = 1) Timing Diagram

Figure 70 shows signal timings during UTOPIA receive operations.

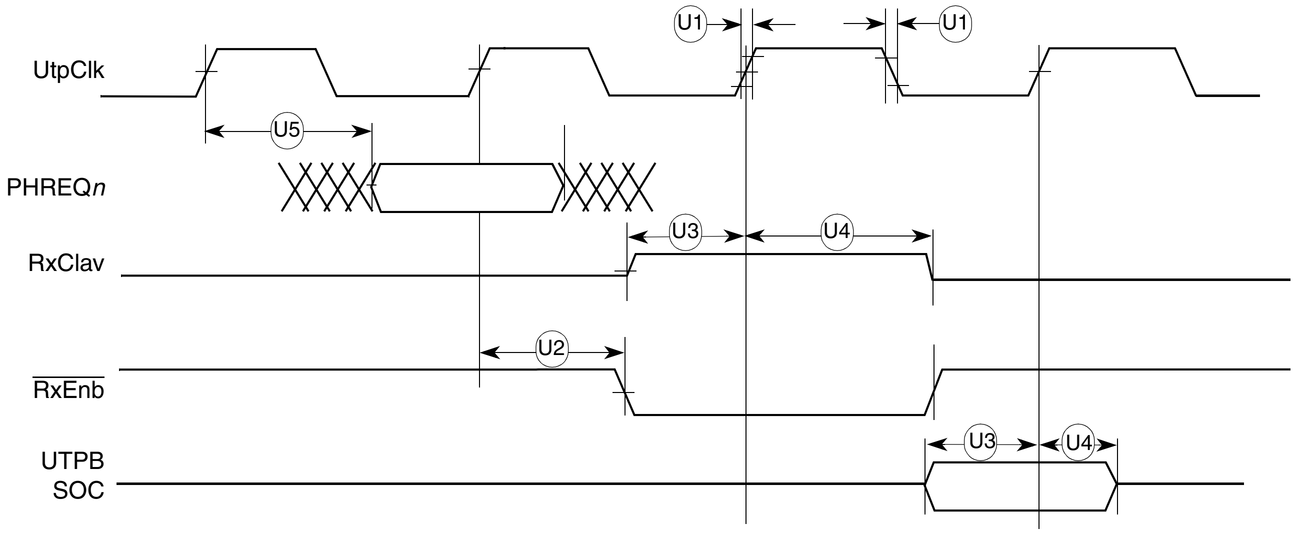


Figure 70. UTOPIA Receive Timing

Figure 71 shows signal timings during UTOPIA transmit operations.

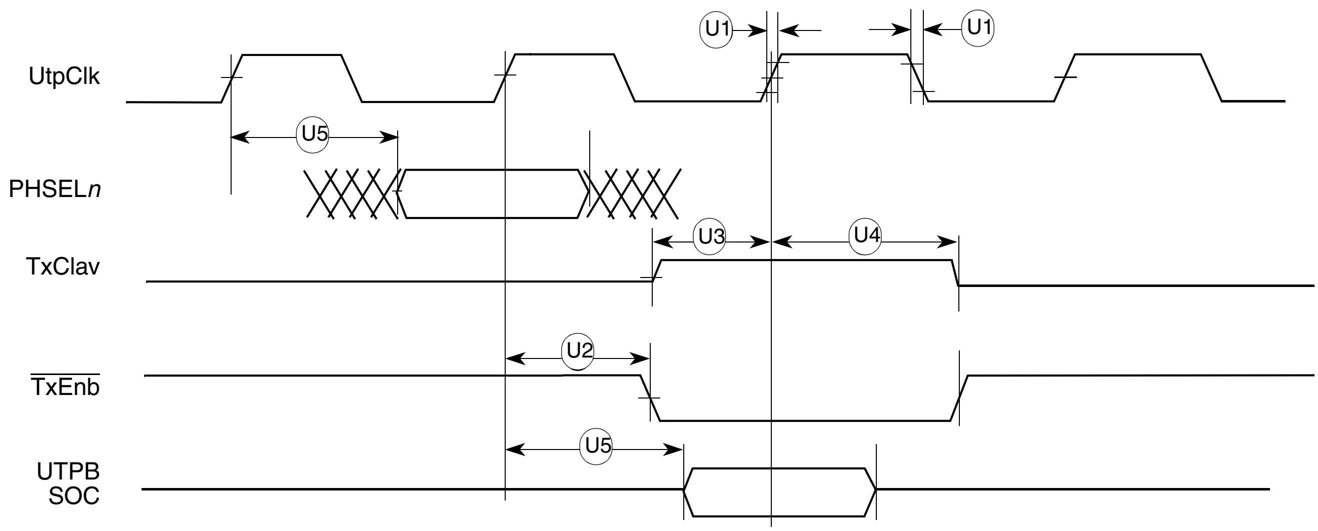


Figure 71. UTOPIA Transmit Timing

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