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Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	66MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (4)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 95°C (TA)
Security Features	-
Package / Case	357-BBGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc860envr66d4

- Up to 8 Kbytes of dual-port RAM
- 16 serial DMA (SDMA) channels
- Three parallel I/O registers with open-drain capability
- Four baud-rate generators (BRGs)
 - Independent (can be tied to any SCC or SMC)
 - Allows changes during operation
 - Autobaud support option
- Four serial communications controllers (SCCs)
 - Ethernet/IEEE 802.3® standard optional on SCC1–4, supporting full 10-Mbps operation (available only on specially programmed devices)
 - HDLC/SDLC (all channels supported at 2 Mbps)
 - HDLC bus (implements an HDLC-based local area network (LAN))
 - Asynchronous HDLC to support point-to-point protocol (PPP)
 - AppleTalk
 - Universal asynchronous receiver transmitter (UART)
 - Synchronous UART
 - Serial infrared (IrDA)
 - Binary synchronous communication (BISYNC)
 - Totally transparent (bit streams)
 - Totally transparent (frame-based with optional cyclic redundancy check (CRC))
- Two SMCs (serial management channels)
 - UART
 - Transparent
 - General circuit interface (GCI) controller
 - Can be connected to the time-division multiplexed (TDM) channels
- One SPI (serial peripheral interface)
 - Supports master and slave modes
 - Supports multimaster operation on the same bus
- One I²C (inter-integrated circuit) port
 - Supports master and slave modes
 - Multiple-master environment support
- Time-slot assigner (TSA)
 - Allows SCCs and SMCs to run in multiplexed and/or non-multiplexed operation
 - Supports T1, CEPT, PCM highway, ISDN basic rate, ISDN primary rate, user defined
 - 1- or 8-bit resolution
 - Allows independent transmit and receive routing, frame synchronization, and clocking

Table 6. DC Electrical Specifications (continued)

Characteristic	Symbol	Min	Max	Unit
Input leakage current, $V_{in} = 3.6$ V (except TMS, $\overline{TRST}$, DSCK, and DSDI pins)	I_{In}	—	10	μA
Input leakage current, $V_{in} = 0$ V (except TMS, $\overline{TRST}$, DSCK, and DSDI pins)	I_{In}	—	10	μA
Input capacitance ²	C_{in}	—	20	pF
Output high voltage, $I_{OH} = -2.0$ mA, $V_{DDH} = 3.0$ V (except XTAL, XFC, and open-drain pins)	V_{OH}	2.4	—	V
Output low voltage $I_{OL} = 2.0$ mA, CLKOUT $I_{OL} = 3.2$ mA ³ $I_{OL} = 5.3$ mA ⁴ $I_{OL} = 7.0$ mA, TXD1/PA14, TXD2/PA12 $I_{OL} = 8.9$ mA, $\overline{TS}$, $\overline{TA}$, $\overline{TEA}$, $\overline{BI}$, $\overline{BB}$, $\overline{HRESET}$, $\overline{SRESET}$	V_{OL}	—	0.5	V

¹ $V_{IL}(\max)$ for the I²C interface is 0.8 V rather than the 1.5 V as specified in the I²C standard.

² Input capacitance is periodically sampled.

³ A(0:31), TSIZ0/ $\overline{REG}$, TSIZ1, D(0:31), DP(0:3)/ $\overline{IRQ}$ (3:6), RD/ $\overline{WR}$, $\overline{BURST}$, $\overline{RSV}/\overline{IRQ2}$, IP_B(0:1)/IWP(0:1)/VFLS(0:1), IP_B2/IOIS16_B/AT2, IP_B3/IWP2/VF2, IP_B4/LWP0/VF0, IP_B5/LWP1/VF1, IP_B6/DSDI/AT0, IP_B7/PTR/AT3, RXD1/PA15, RXD2/PA13, L1TXDB/PA11, L1RXDB/PA10, L1TXDA/PA9, L1RXDA/PA8, TIN1/L1RCLKA/BRGO1/CLK1/PA7, BRGCLK1/ $\overline{TOUT1}/\overline{CLK2}/PA6$, TIN2/L1TCLKA/BRGO2/CLK3/PA5, $\overline{TOUT2}/\overline{CLK4}/PA4$, TIN3/BRGO3/CLK5/PA3, BRGCLK2/L1RCLKB/ $\overline{TOUT3}/\overline{CLK6}/PA2$, TIN4/BRGO4/CLK7/PA1, L1TCLKB/ $\overline{TOUT4}/\overline{CLK8}/PA0$, $\overline{REJECT1}/\overline{SPISEL}/PB31$, SPICLK/PB30, SPIMOSI/PB29, BRGO4/SPIMISO/PB28, BRGO1/I2CSDA/PB27, BRGO2/I2CSCL/PB26, SMTXD1/PB25, SMRXD1/PB24, $\overline{SMSYN1}/\overline{SDACK1}/PB23$, $\overline{SMSYN2}/\overline{SDACK2}/PB22$, SMTXD2/L1CLKOB/PB21, SMRXD2/L1CLKOA/PB20, L1ST1/ $\overline{RTS1}/PB19$, L1ST2/ $\overline{RTS2}/PB18$, L1ST3/L1RQB/PB17, L1ST4/L1RQA/PB16, BRGO3/PB15, $\overline{RSTRT1}/PB14$, L1ST1/ $\overline{RTS1}/\overline{DREQ0}/PC15$, L1ST2/ $\overline{RTS2}/\overline{DREQ1}/PC14$, L1ST3/L1RQB/PC13, L1ST4/L1RQA/PC12, $\overline{CTS1}/PC11$, $\overline{TGATE1}/\overline{CD1}/PC10$, $\overline{CTS2}/PC9$, $\overline{TGATE2}/\overline{CD2}/PC8$, $\overline{SDACK2}/L1TSYNCA/PC7$, L1RSYNCA/PC6, $\overline{SDACK1}/L1TSYNCA/PC5$, L1RSYNCA/PC4, PD15, PD14, PD13, PD12, PD11, PD10, PD9, PD8, PD5, PD6, PD7, PD4, PD3, MII_MDC, MII_TX_ER, MII_EN, MII_MDIO, and MII_TXD[0:3]

⁴ $\overline{BDIP}/\overline{GPL}_B(5)$, $\overline{BR}$, $\overline{BG}$, $\overline{FRZ}/\overline{IRQ6}$, $\overline{CS}(0:5)$, $\overline{CS}(6)/\overline{CE}(1)_B$, $\overline{CS}(7)/\overline{CE}(2)_B$, $\overline{WE0}/\overline{BS}_B0/\overline{IORD}$, $\overline{WE1}/\overline{BS}_B1/\overline{IOWR}$, $\overline{WE2}/\overline{BS}_B2/\overline{PCOE}$, $\overline{WE3}/\overline{BS}_B3/\overline{PCWE}$, $\overline{BS}_A(0:3)$, $\overline{GPL}_A0/\overline{GPL}_B0$, $\overline{OE}/\overline{GPL}_A1/\overline{GPL}_B1$, $\overline{GPL}_A(2:3)/\overline{GPL}_B(2:3)/\overline{CS}(2:3)$, UPWAITA/ $\overline{GPL}_A4$, UPWAITB/ $\overline{GPL}_B4$, $\overline{GPL}_A5$, ALE_A, $\overline{CE1}_A$, $\overline{CE2}_A$, ALE_B/DSCK/AT1, OP(0:1), OP2/MODCK1/ $\overline{STS}$, OP3/MODCK2/DSDO, and BADDR(28:30)

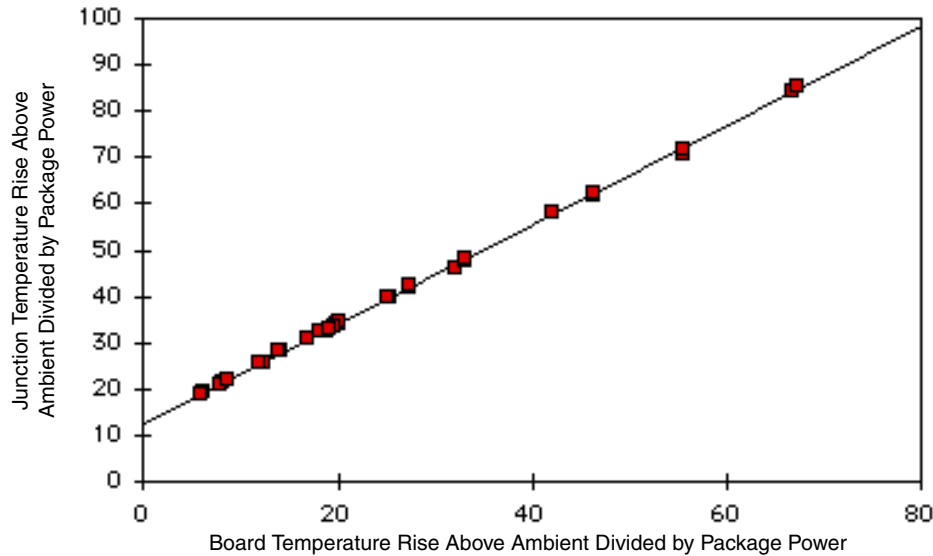


Figure 2. Effect of Board Temperature Rise on Thermal Behavior

If the board temperature is known, an estimate of the junction temperature in the environment can be made using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

$R_{\theta JB}$ = junction-to-board thermal resistance ($^{\circ}\text{C}/\text{W}$)

T_B = board temperature ($^{\circ}\text{C}$)

P_D = power dissipation in package

If the board temperature is known and the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. For this method to work, the board and board mounting must be similar to the test board used to determine the junction-to-board thermal resistance, namely a 2s2p (board with a power and a ground plane) and by attaching the thermal balls to the ground plane.

7.4 Estimation Using Simulation

When the board temperature is not known, a thermal simulation of the application is needed. The simple two-resistor model can be used with the thermal simulation of the application [2], or a more accurate and complex model of the package can be used in the thermal simulation.

7.5 Experimental Determination

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

Table 7. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B9	CLKOUT to A(0:31), BADDR(28:30), RD/WR, BURST, D(0:31), DP(0:3), TSIZ(0:1), REG, RSV, AT(0:3), PTR High-Z	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.04	ns
B11	CLKOUT to $\overline{TS}$, $\overline{BB}$ assertion	7.58	13.58	6.25	12.25	5.00	11.00	3.80	11.29	ns
B11a	CLKOUT to $\overline{TA}$, $\overline{BI}$ assertion (when driven by the memory controller or PCMCIA interface)	2.50	9.25	2.50	9.25	2.50	9.25	2.50	9.75	ns
B12	CLKOUT to $\overline{TS}$, $\overline{BB}$ negation	7.58	14.33	6.25	13.00	5.00	11.75	3.80	8.54	ns
B12a	CLKOUT to $\overline{TA}$, $\overline{BI}$ negation (when driven by the memory controller or PCMCIA interface)	2.50	11.00	2.50	11.00	2.50	11.00	2.50	9.00	ns
B13	CLKOUT to $\overline{TS}$, $\overline{BB}$ High-Z	7.58	21.58	6.25	20.25	5.00	19.00	3.80	14.04	ns
B13a	CLKOUT to $\overline{TA}$, $\overline{BI}$ High-Z (when driven by the memory controller or PCMCIA interface)	2.50	15.00	2.50	15.00	2.50	15.00	2.50	15.00	ns
B14	CLKOUT to $\overline{TEA}$ assertion	2.50	10.00	2.50	10.00	2.50	10.00	2.50	9.00	ns
B15	CLKOUT to $\overline{TEA}$ High-Z	2.50	15.00	2.50	15.00	2.50	15.00	2.50	15.00	ns
B16	$\overline{TA}$, $\overline{BI}$ valid to CLKOUT (setup time)	9.75	—	9.75	—	9.75	—	6.00	—	ns
B16a	$\overline{TEA}$, $\overline{KR}$, $\overline{RETRY}$, $\overline{CR}$ valid to CLKOUT (setup time)	10.00	—	10.00	—	10.00	—	4.50	—	ns
B16b	$\overline{BB}$, $\overline{BG}$, $\overline{BR}$, valid to CLKOUT (setup time) ⁵	8.50	—	8.50	—	8.50	—	4.00	—	ns
B17	CLKOUT to $\overline{TA}$, $\overline{TEA}$, $\overline{BI}$, $\overline{BB}$, $\overline{BG}$, $\overline{BR}$ valid (hold time)	1.00	—	1.00	—	1.00	—	2.00	—	ns
B17a	CLKOUT to $\overline{KR}$, $\overline{RETRY}$, $\overline{CR}$ valid (hold time)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B18	D(0:31), DP(0:3) valid to CLKOUT rising edge (setup time) ⁶	6.00	—	6.00	—	6.00	—	6.00	—	ns
B19	CLKOUT rising edge to D(0:31), DP(0:3) valid (hold time) ⁶	1.00	—	1.00	—	1.00	—	2.00	—	ns
B20	D(0:31), DP(0:3) valid to CLKOUT falling edge (setup time) ⁷	4.00	—	4.00	—	4.00	—	4.00	—	ns
B21	CLKOUT falling edge to D(0:31), DP(0:3) valid (hold time) ⁷	2.00	—	2.00	—	2.00	—	2.00	—	ns
B22	CLKOUT rising edge to $\overline{CS}$ asserted GPCM ACS = 00	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.04	ns
B22a	CLKOUT falling edge to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 0	—	8.00	—	8.00	—	8.00	—	8.00	ns
B22b	CLKOUT falling edge to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 0, EBDF = 0	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.54	ns
B22c	CLKOUT falling edge to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 0, EBDF = 1	10.86	17.99	8.88	16.00	7.00	14.13	5.18	12.31	ns

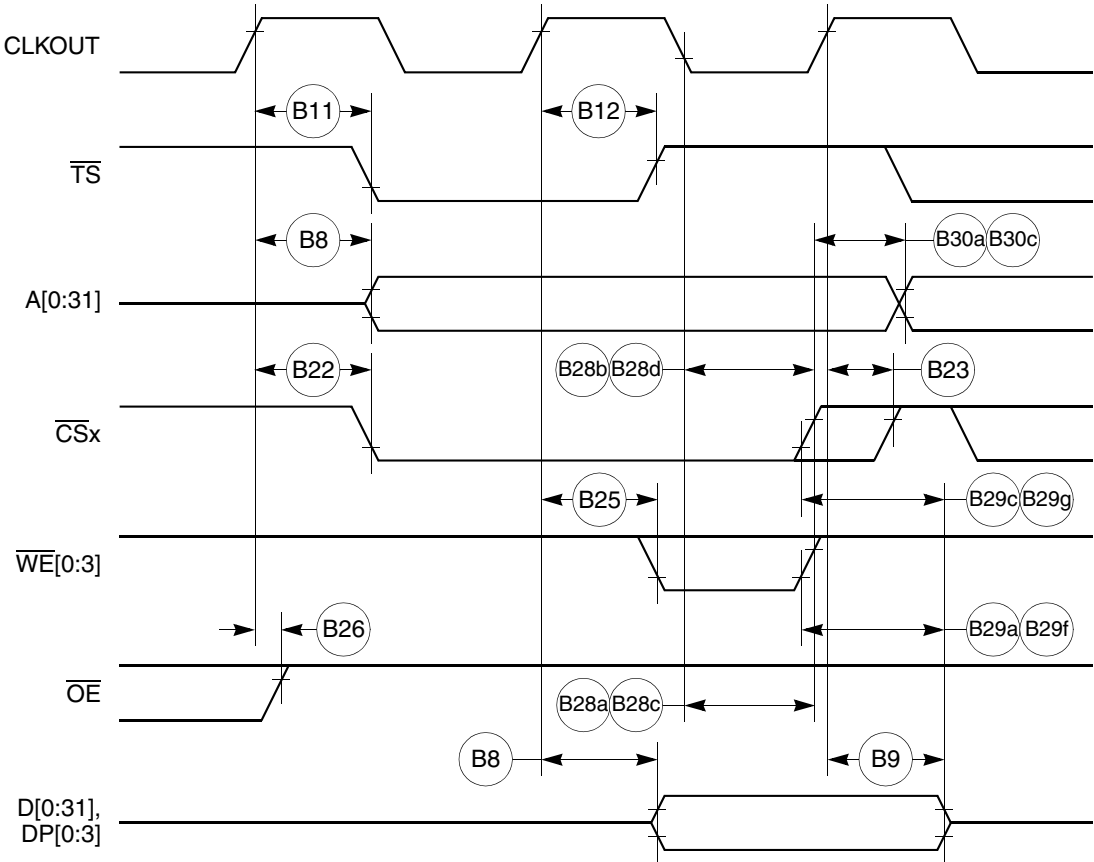


Figure 15. External Bus Write Timing (GPCM Controlled—TRLX = 0 or 1, CSNT = 1)

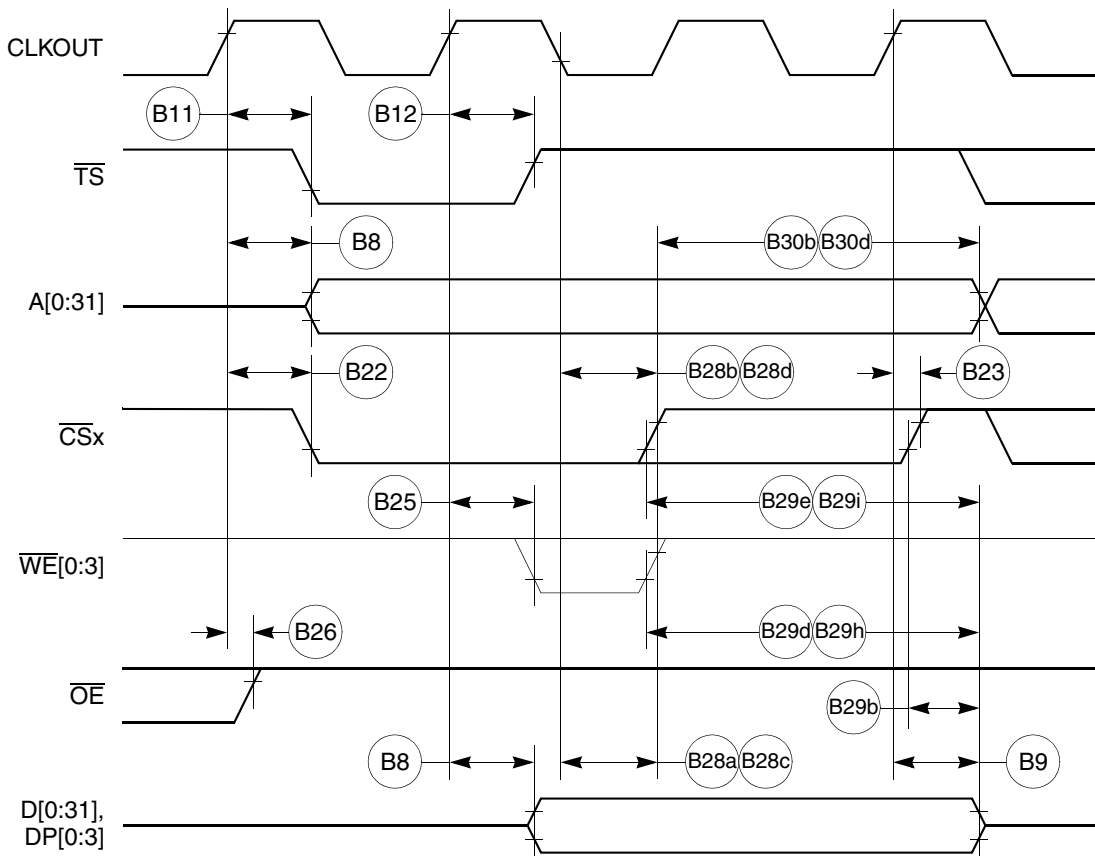


Figure 16. External Bus Write Timing (GPCM Controlled—TRLX = 0 or 1, CSNT = 1)

Figure 20 provides the timing for the synchronous external master access controlled by the GPCM.

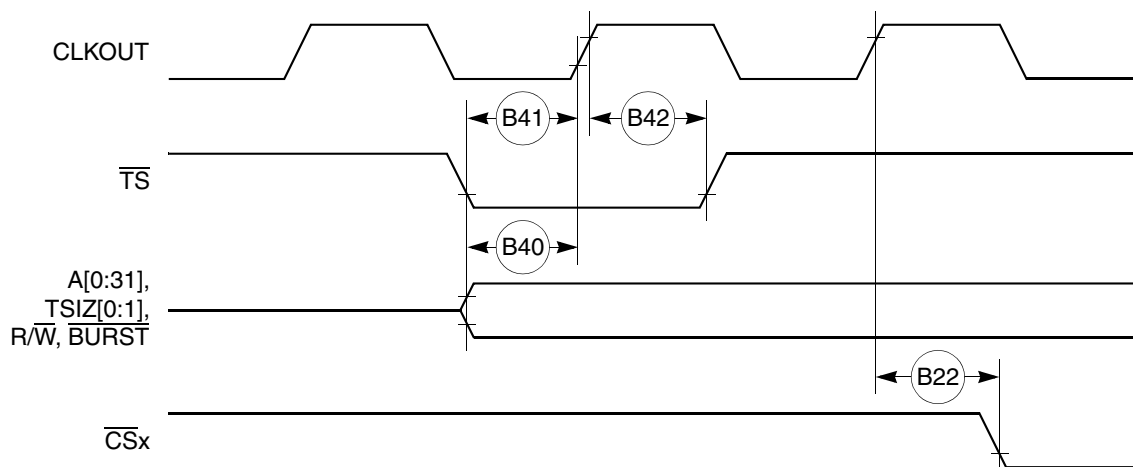


Figure 20. Synchronous External Master Access Timing (GPCM Handled ACS = 00)

Figure 21 provides the timing for the asynchronous external master memory access controlled by the GPCM.

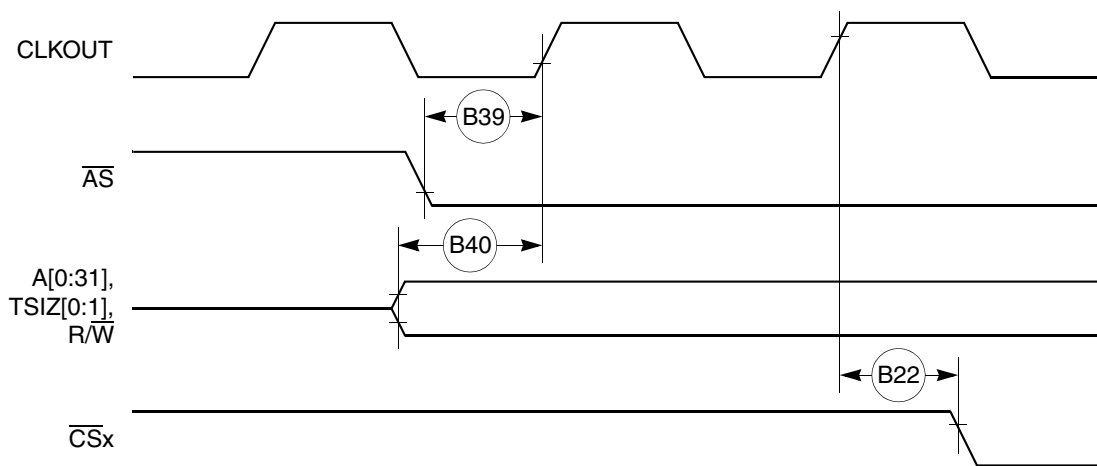


Figure 21. Asynchronous External Master Memory Access Timing (GPCM Controlled—ACS = 00)

Figure 22 provides the timing for the asynchronous external master control signals negation.

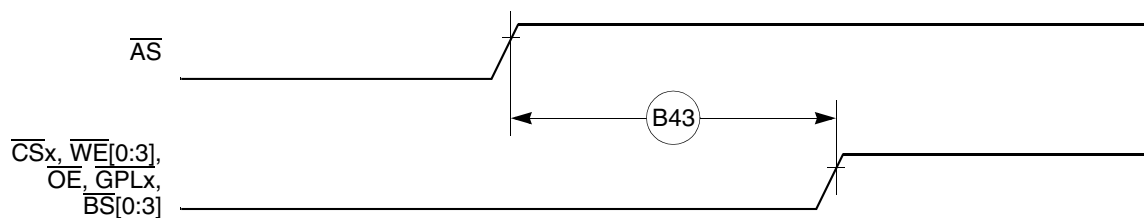


Figure 22. Asynchronous External Master—Control Signals Negation Timing

Table 8 provides interrupt timing for the MPC860.

Table 8. Interrupt Timing

Num	Characteristic ¹	All Frequencies		Unit
		Min	Max	
I39	$\overline{\text{IRQ}}_x$ valid to CLKOUT rising edge (setup time)	6.00	—	ns
I40	$\overline{\text{IRQ}}_x$ hold time after CLKOUT	2.00	—	ns
I41	$\overline{\text{IRQ}}_x$ pulse width low	3.00	—	ns
I42	$\overline{\text{IRQ}}_x$ pulse width high	3.00	—	ns
I43	$\overline{\text{IRQ}}_x$ edge-to-edge time	$4 \times T_{\text{CLOCKOUT}}$	—	—

¹ The timings I39 and I40 describe the testing conditions under which the $\overline{\text{IRQ}}$ lines are tested when being defined as level-sensitive. The $\overline{\text{IRQ}}$ lines are synchronized internally and do not have to be asserted or negated with reference to the CLKOUT.
The timings I41, I42, and I43 are specified to allow the correct function of the $\overline{\text{IRQ}}$ lines detection circuitry and have no direct relation with the total system interrupt latency that the MPC860 is able to support.

Figure 23 provides the interrupt detection timing for the external level-sensitive lines.

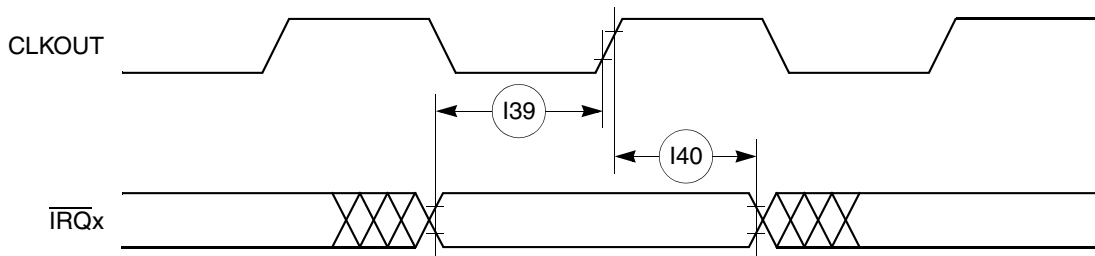


Figure 23. Interrupt Detection Timing for External Level Sensitive Lines

Figure 24 provides the interrupt detection timing for the external edge-sensitive lines.

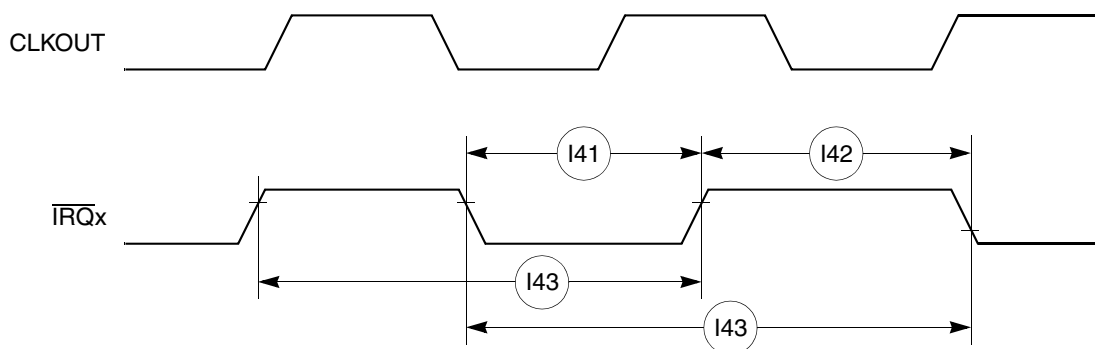


Figure 24. Interrupt Detection Timing for External Edge Sensitive Lines

Figure 26 provides the PCMCIA access cycle timing for the external bus write.

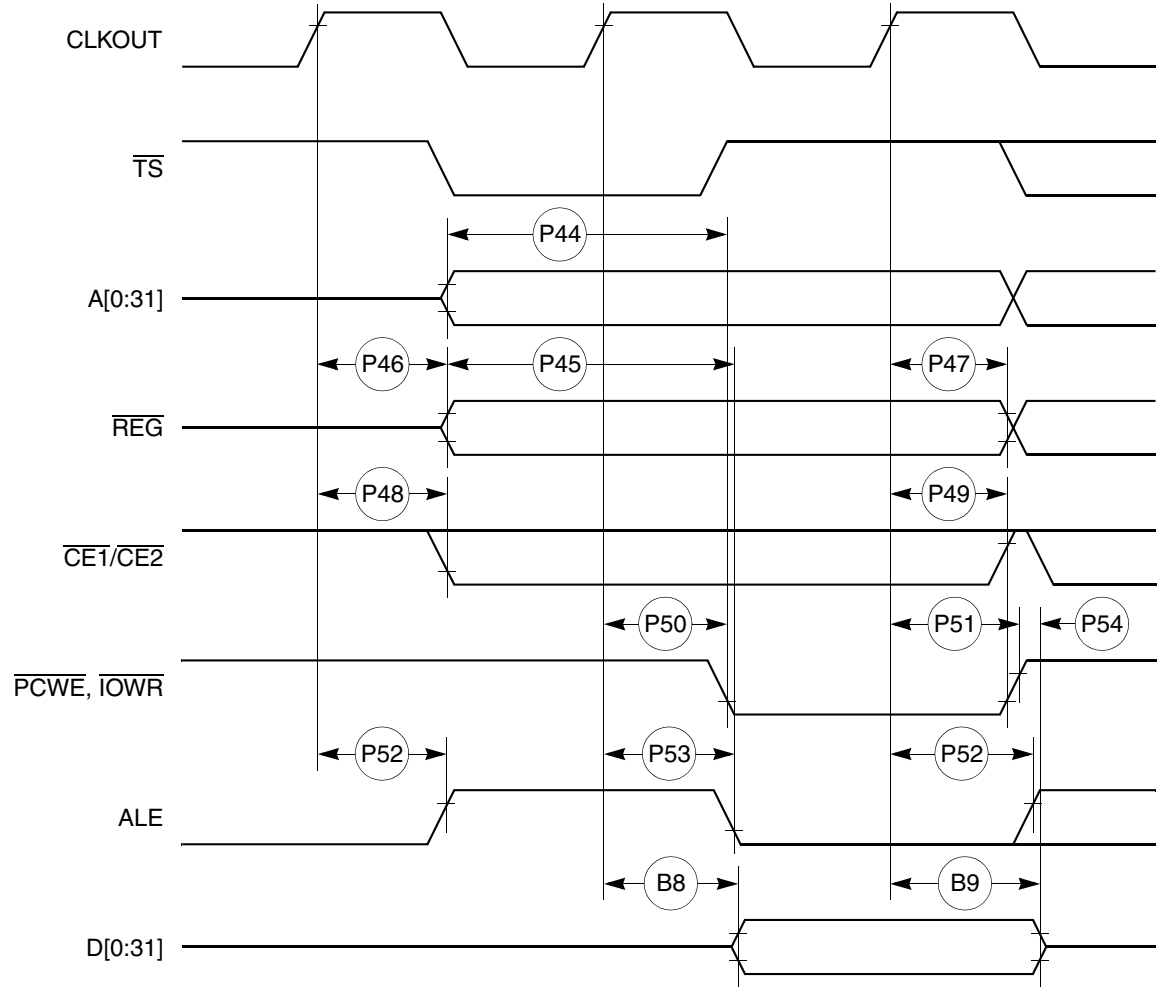


Figure 26. PCMCIA Access Cycle Timing External Bus Write

Figure 27 provides the PCMCIA $\overline{\text{WAIT}}$ signal detection timing.

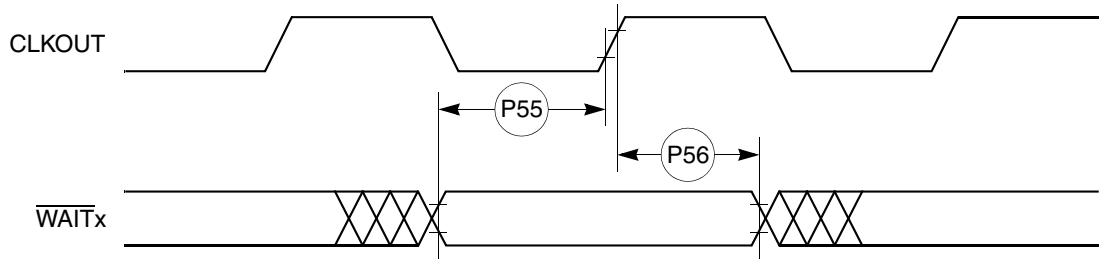


Figure 27. PCMCIA $\overline{\text{WAIT}}$ Signal Detection Timing

Table 10 shows the PCMCIA port timing for the MPC860.

Table 10. PCMCIA Port Timing

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
P57	CLKOUT to OPx valid	—	19.00	—	19.00	—	19.00	—	19.00	ns
P58	$\overline{\text{HRESET}}$ negated to OPx drive ¹	25.73	—	21.75	—	18.00	—	14.36	—	ns
P59	IP_Xx valid to CLKOUT rising edge	5.00	—	5.00	—	5.00	—	5.00	—	ns
P60	CLKOUT rising edge to IP_Xx invalid	1.00	—	1.00	—	1.00	—	1.00	—	ns

¹ OP2 and OP3 only.

Figure 28 provides the PCMCIA output port timing for the MPC860.

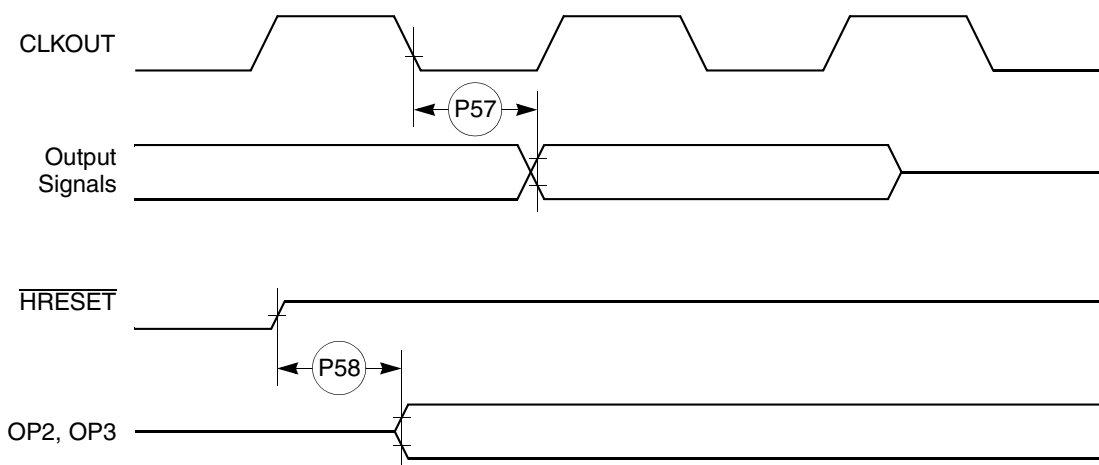


Figure 28. PCMCIA Output Port Timing

Figure 29 provides the PCMCIA output port timing for the MPC860.

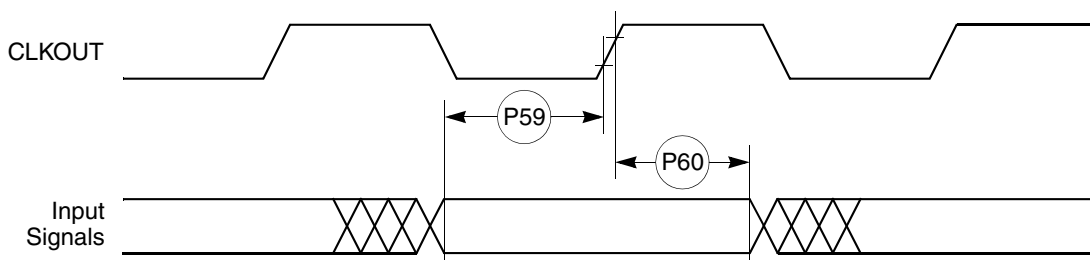


Figure 29. PCMCIA Input Port Timing

11 CPM Electrical Characteristics

This section provides the AC and DC electrical specifications for the communications processor module (CPM) of the MPC860.

11.1 PIP/PIO AC Electrical Specifications

Table 14 provides the PIP/PIO AC timings as shown in Figure 39 through Figure 43.

Table 14. PIP/PIO Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
21	Data-in setup time to STBI low	0	—	ns
22	Data-in hold time to STBI high	$2.5 - t_3^1$	—	CLK
23	STBI pulse width	1.5	—	CLK
24	STBO pulse width	1 CLK – 5 ns	—	ns
25	Data-out setup time to STBO low	2	—	CLK
26	Data-out hold time from STBO high	5	—	CLK
27	STBI low to STBO low (Rx interlock)	—	2	CLK
28	STBI low to STBO high (Tx interlock)	2	—	CLK
29	Data-in setup time to clock high	15	—	ns
30	Data-in hold time from clock high	7.5	—	ns
31	Clock low to data-out valid (CPU writes data, control, or direction)	—	25	ns

¹ t_3 = Specification 23.

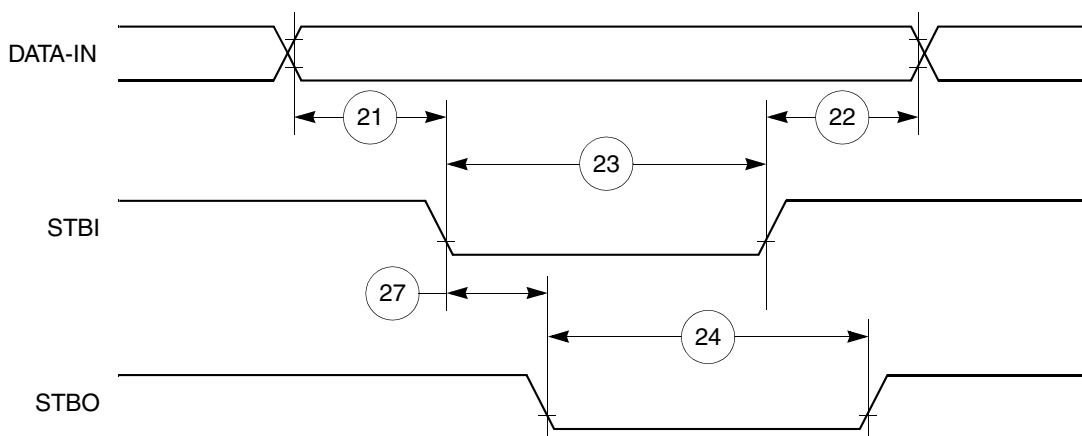


Figure 39. PIP Rx (Interlock Mode) Timing Diagram

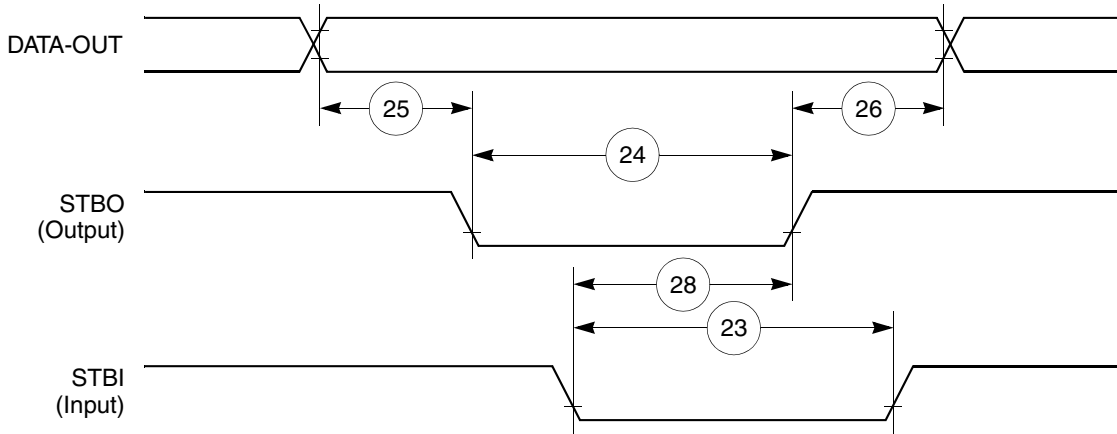


Figure 40. PIP Tx (Interlock Mode) Timing Diagram

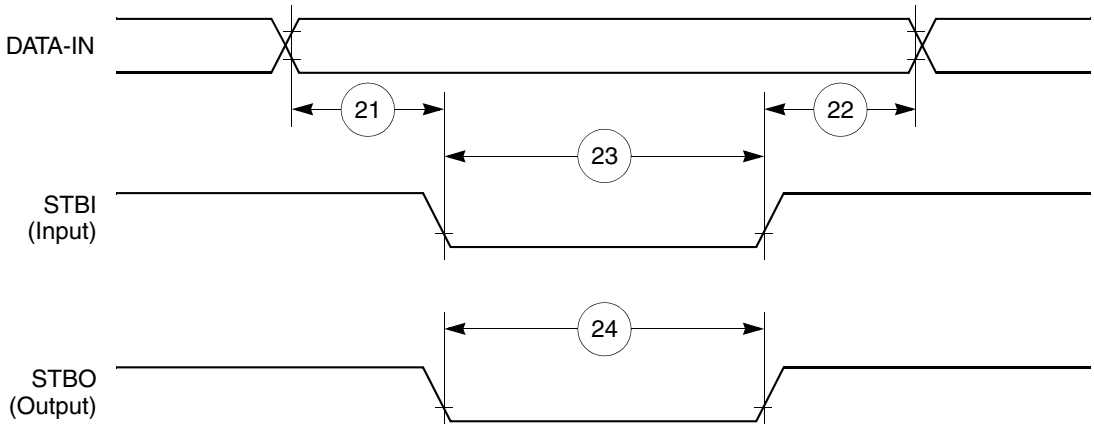


Figure 41. PIP Rx (Pulse Mode) Timing Diagram

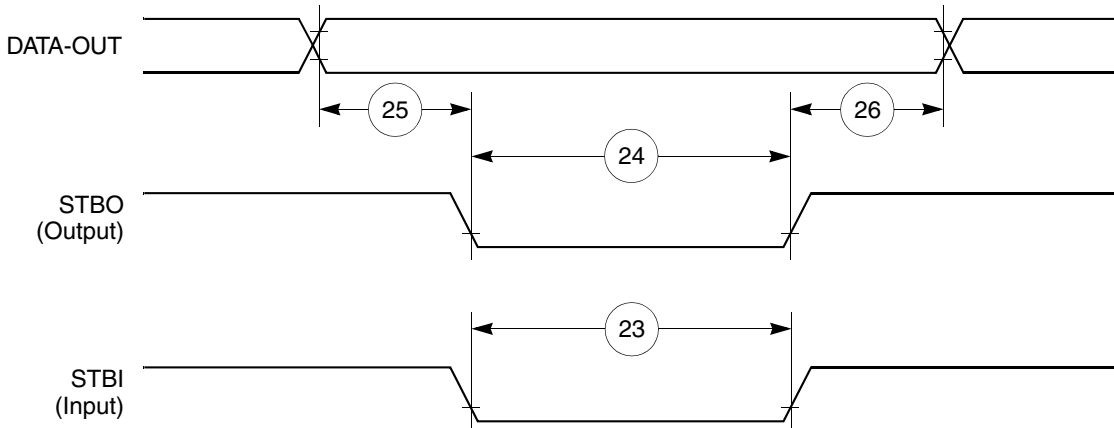


Figure 42. PIP TX (Pulse Mode) Timing Diagram

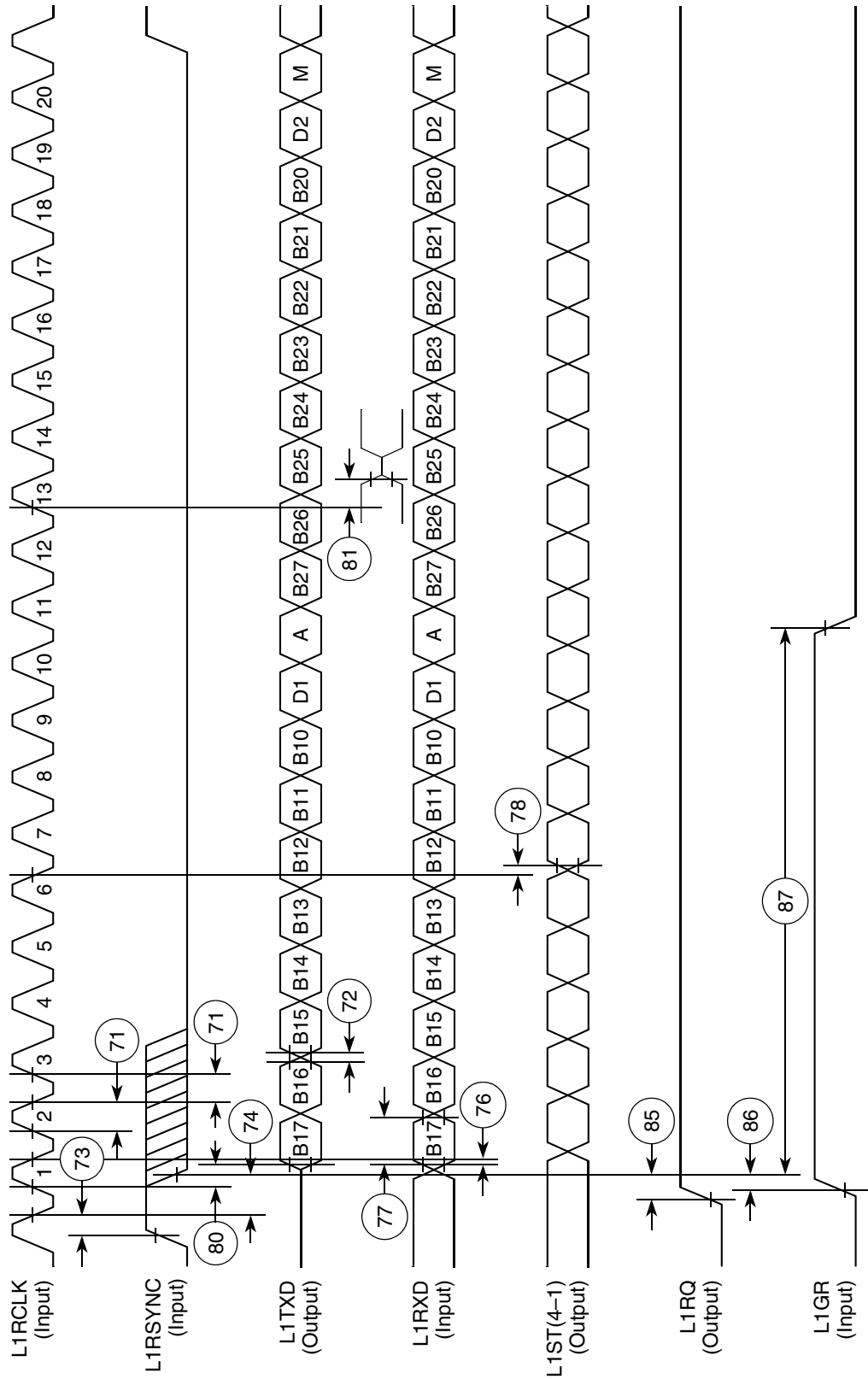


Figure 55. IDL Timing

Table 22. Ethernet Timing (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
135	$\overline{\text{RSTRT}}$ active delay (from TCLK1 falling edge)	10	50	ns
136	$\overline{\text{RSTRT}}$ inactive delay (from TCLK1 falling edge)	10	50	ns
137	$\overline{\text{REJECT}}$ width low	1	—	CLK
138	CLKO1 low to $\overline{\text{SDACK}}$ asserted ²	—	20	ns
139	CLKO1 low to $\overline{\text{SDACK}}$ negated ²	—	20	ns

¹ The ratios SYNCCLK/RCLK1 and SYNCCLK/TCLK1 must be greater than or equal to 2/1.

² $\overline{\text{SDACK}}$ is asserted whenever the SDMA writes the incoming frame DA into memory.

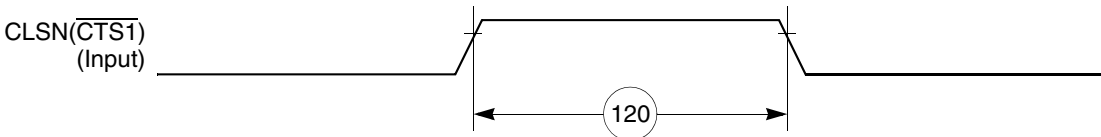


Figure 59. Ethernet Collision Timing Diagram

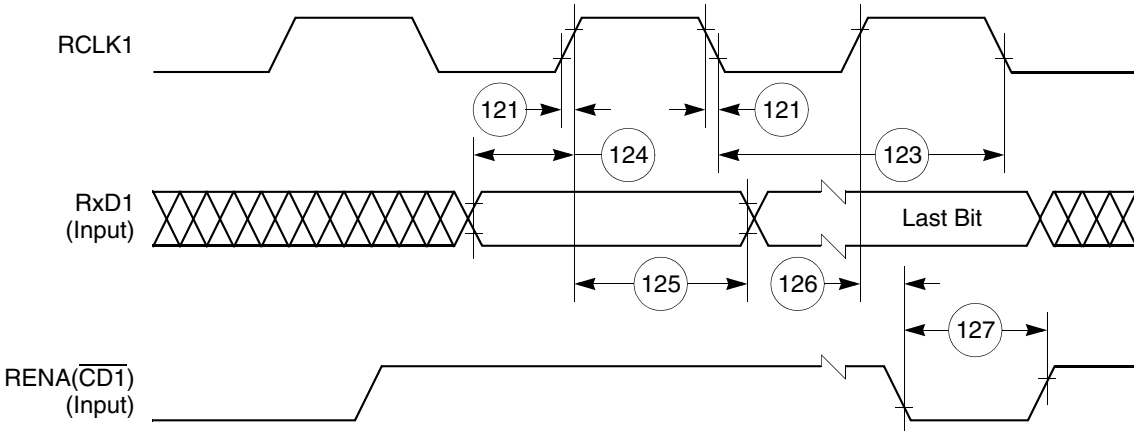


Figure 60. Ethernet Receive Timing Diagram

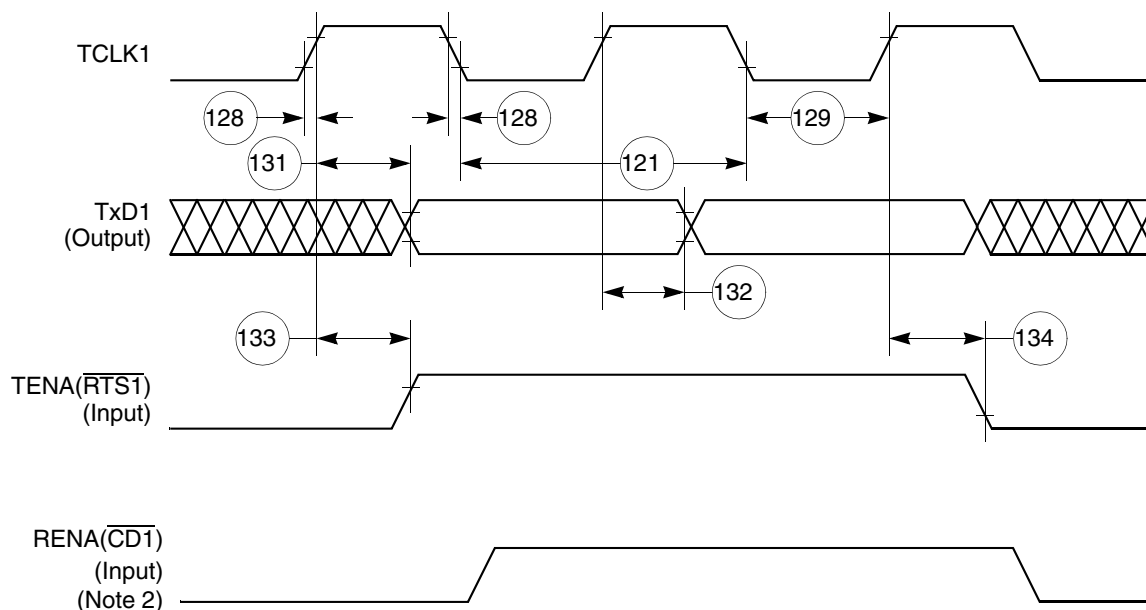


Figure 61. Ethernet Transmit Timing Diagram

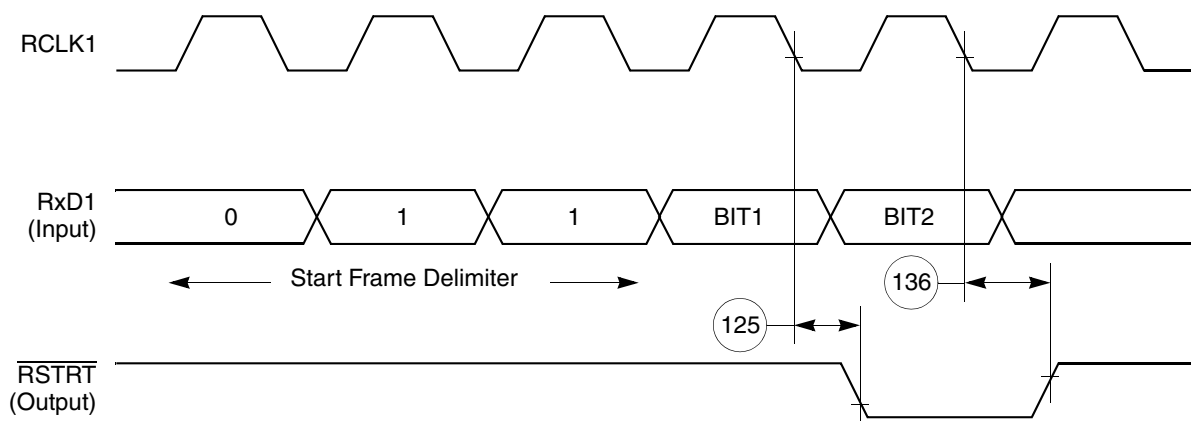


Figure 62. CAM Interface Receive Start Timing Diagram



Figure 63. CAM Interface $\overline{\text{REJECT}}$ Timing Diagram

11.10 SPI Master AC Electrical Specifications

Table 24 provides the SPI master timings as shown in Figure 65 and Figure 66.

Table 24. SPI Master Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
160	MASTER cycle time	4	1024	t_{cyc}
161	MASTER clock (SCK) high or low time	2	512	t_{cyc}
162	MASTER data setup time (inputs)	50	—	ns
163	Master data hold time (inputs)	0	—	ns
164	Master data valid (after SCK edge)	—	20	ns
165	Master data hold time (outputs)	0	—	ns
166	Rise time output	—	15	ns
167	Fall time output	—	15	ns

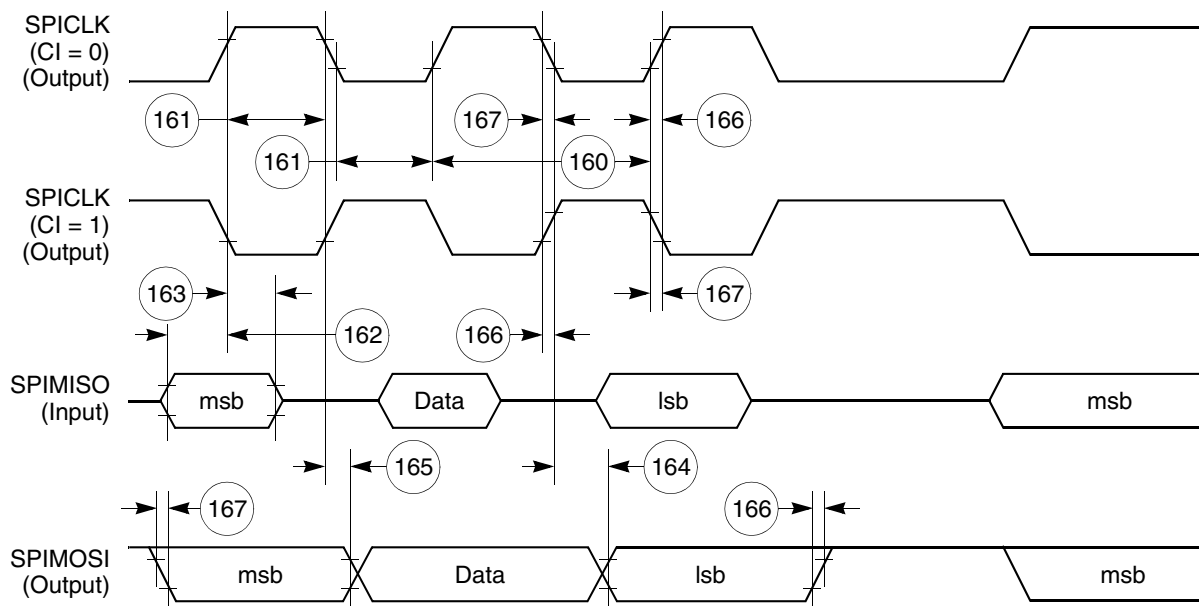


Figure 65. SPI Master (CP = 0) Timing Diagram

Figure 69 shows the I²C bus timing.

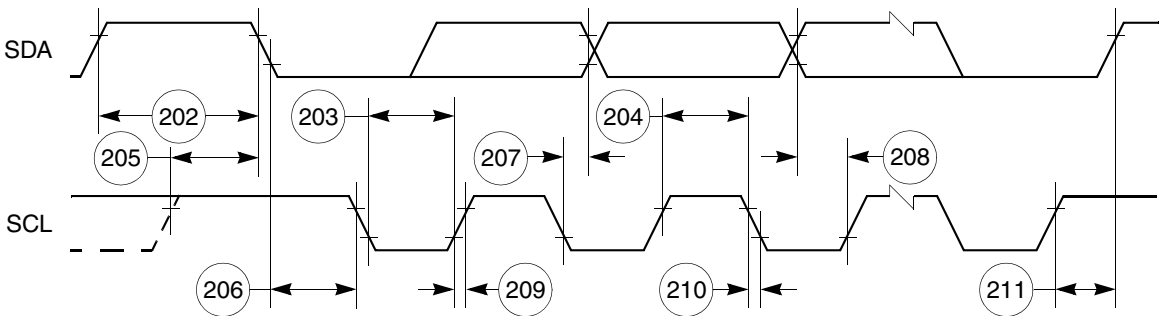


Figure 69. I²C Bus Timing Diagram

12 UTOPIA AC Electrical Specifications

Table 28 shows the AC electrical specifications for the UTOPIA interface.

Table 28. UTOPIA AC Electrical Specifications

Num	Signal Characteristic	Direction	Min	Max	Unit
U1	UtpClk rise/fall time (Internal clock option)	Output	—	3.5	ns
	Duty cycle		50	50	%
	Frequency		—	50	MHz
U1a	UtpClk rise/fall time (external clock option)	Input	—	3.5	ns
	Duty cycle		40	60	%
	Frequency		—	50	MHz
U2	$\overline{\text{RxEnb}}$ and $\overline{\text{TxEnb}}$ active delay	Output	2	16	ns
U3	UTPB, SOC, Rxclav and Txclav setup time	Input	8	—	ns
U4	UTPB, SOC, Rxclav and Txclav hold time	Input	1	—	ns
U5	UTPB, SOC active delay (and PHREQ and PHSEL active delay in MPHY mode)	Output	2	16	ns

13.3 MII Async Inputs Signal Timing (MII_CRCS, MII_COL)

Table 31 provides information on the MII async inputs signal timing.

Table 31. MII Async Inputs Signal Timing

Num	Characteristic	Min	Max	Unit
M9	MII_CRCS, MII_COL minimum pulse width	1.5	—	MII_TX_CLK period

Figure 74 shows the MII asynchronous inputs signal timing diagram.

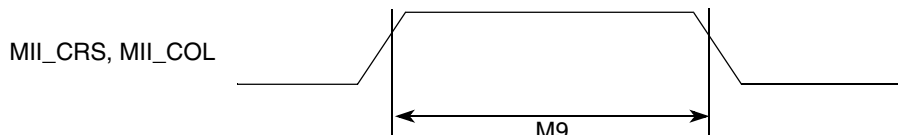


Figure 74. MII Async Inputs Timing Diagram

13.4 MII Serial Management Channel Timing (MII_MDIO, MII_MDC)

Table 32 provides information on the MII serial management channel signal timing. The FEC functions correctly with a maximum MDC frequency in excess of 2.5 MHz. The exact upper bound is under investigation.

Table 32. MII Serial Management Channel Timing

Num	Characteristic	Min	Max	Unit
M10	MII_MDC falling edge to MII_MDIO output invalid (minimum propagation delay)	0	—	ns
M11	MII_MDC falling edge to MII_MDIO output valid (max prop delay)	—	25	ns
M12	MII_MDIO (input) to MII_MDC rising edge setup	10	—	ns
M13	MII_MDIO (input) to MII_MDC rising edge hold	0	—	ns
M14	MII_MDC pulse width high	40%	60%	MII_MDC period
M15	MII_MDC pulse width low	40%	60%	MII_MDC period

Figure 75 shows the MII serial management channel timing diagram.

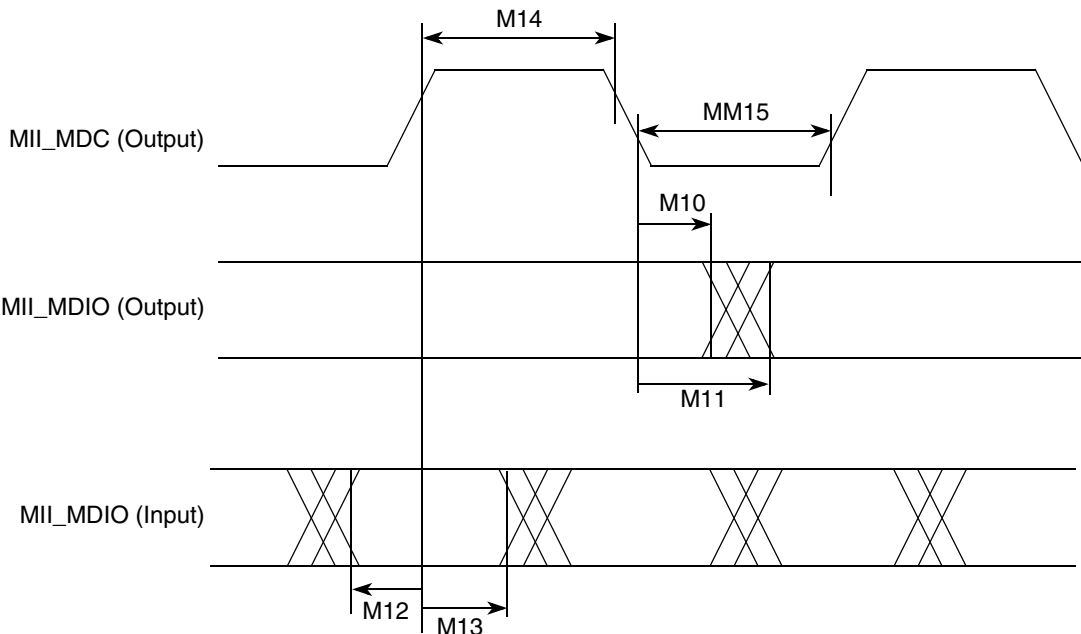


Figure 75. MII Serial Management Channel Timing Diagram

14 Mechanical Data and Ordering Information

14.1 Ordering Information

Table 33 provides information on the MPC860 Revision D.4 derivative devices.

Table 33. MPC860 Family Revision D.4 Derivatives

Device	Number of SCCs ¹	Ethernet Support ² (Mbps)	Multichannel HDLC Support	ATM Support
MPC855T	1	10/100	Yes	Yes
MPC860DE	2	10	N/A	N/A
MPC860DT		10/100	Yes	Yes
MPC860DP		10/100	Yes	Yes
MPC860EN	4	10	N/A	N/A
MPC860SR		10	Yes	Yes
MPC860T		10/100	Yes	Yes
MPC860P		10/100	Yes	Yes

¹ Serial communications controller (SCC)

² Up to 4 channels at 40 MHz or 2 channels at 25 MHz

14.3 Mechanical Dimensions of the PBGA Package

Figure 77 shows the mechanical dimensions of the ZP PBGA package.

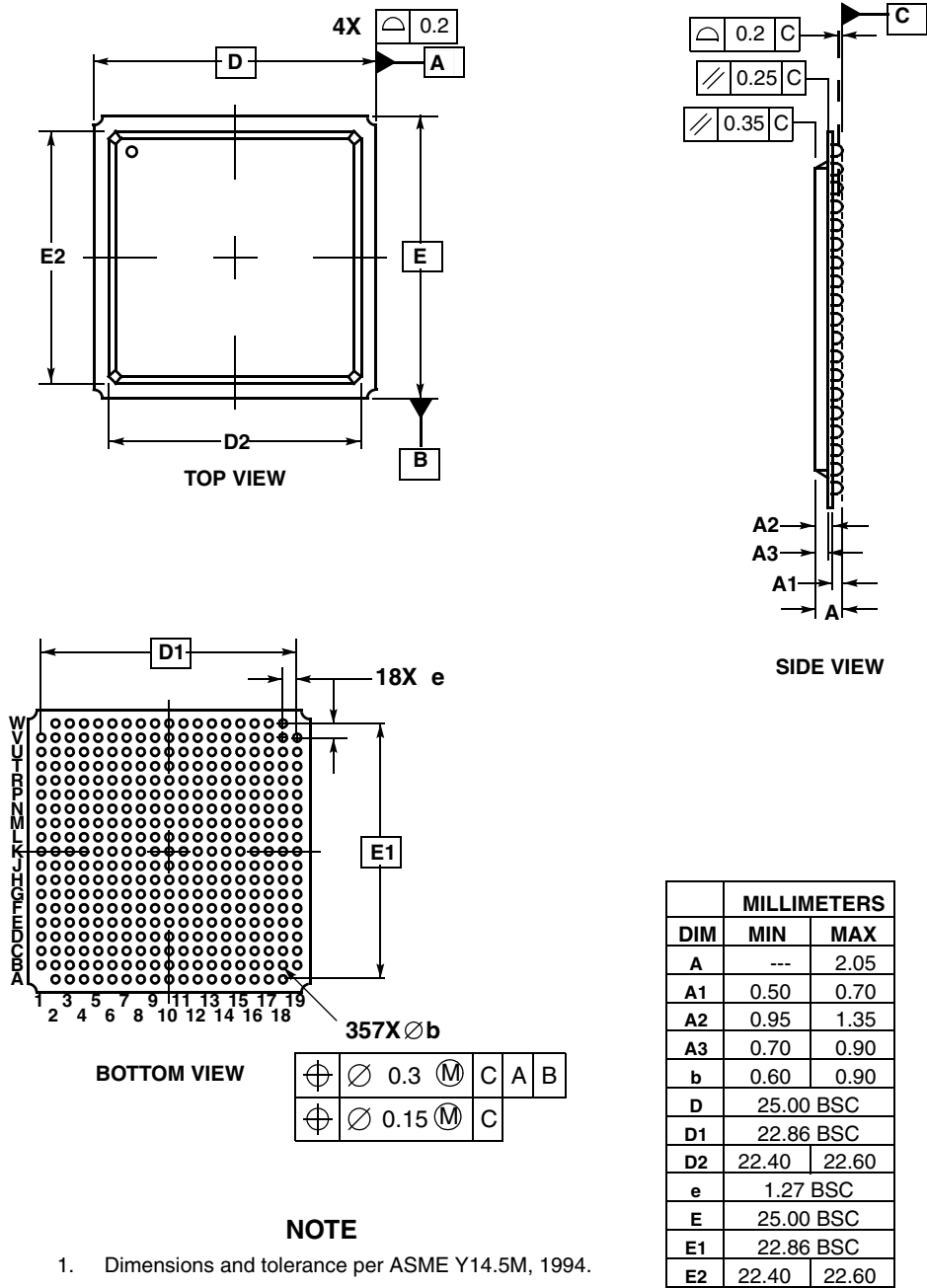


Figure 77. Mechanical Dimensions and Bottom Surface Nomenclature of the ZP PBGA Package