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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Obsolete
MPC8xx
1 Core, 32-Bit
80MHz
Communications; CPM
DRAM
No
-
10Mbps (4)
-
-
3.3V
0°C ~ 95°C (TA)
-
357-BBGA
357-PBGA (25x25)
https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc860envr80d4

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		33	MHz	40	MHz	50 I	MHz	66 I	MHz	
Num	Characteristic	Min	Max	Min	Max	Min	Max	Min	Max	Unit
B31a	CLKOUT falling edge to CS valid—as requested by control bit CST1 in the corresponding word in UPM	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.54	ns
B31b	CLKOUT rising edge to \overline{CS} valid—as requested by control bit CST2 in the corresponding word in UPM	1.50	8.00	1.50	8.00	1.50	8.00	1.50	8.00	ns
B31c	CLKOUT rising edge to $\overline{\text{CS}}$ valid—as requested by control bit CST3 in the corresponding word in UPM	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.04	ns
B31d	CLKOUT falling edge to \overline{CS} valid—as requested by control bit CST1 in the corresponding word in UPM, EBDF = 1	13.26	17.99	11.28	16.00	9.40	14.13	7.58	12.31	ns
B32	CLKOUT falling edge to BS valid—as requested by control bit BST4 in the corresponding word in UPM	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns
B32a	CLKOUT falling edge to \overline{BS} valid—as requested by control bit BST1 in the corresponding word in UPM, EBDF = 0	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.54	ns
B32b	CLKOUT rising edge to $\overline{\text{BS}}$ valid—as requested by control bit BST2 in the corresponding word in UPM	1.50	8.00	1.50	8.00	1.50	8.00	1.50	8.00	ns
B32c	CLKOUT rising edge to $\overline{\text{BS}}$ valid—as requested by control bit BST3 in the corresponding word in UPM	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.54	ns
B32d	CLKOUT falling edge to \overline{BS} valid—as requested by control bit BST1 in the corresponding word in UPM, EBDF = 1	13.26	17.99	11.28	16.00	9.40	14.13	7.58	12.31	ns
B33	CLKOUT falling edge to GPL valid—as requested by control bit GxT4 in the corresponding word in UPM	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns
B33a	CLKOUT rising edge to GPL valid—as requested by control bit GxT3 in the corresponding word in UPM	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.54	ns
B34	A(0:31), BADDR(28:30), and D(0:31) to \overline{CS} valid—as requested by control bit CST4 in the corresponding word in UPM	5.58	—	4.25	—	3.00	—	1.79	_	ns
B34a	A(0:31), BADDR(28:30), and D(0:31) to \overline{CS} valid—as requested by control bit CST1 in the corresponding word in UPM	13.15		10.50		8.00		5.58	_	ns
B34b	A(0:31), BADDR(28:30), and D(0:31) to \overline{CS} valid—as requested by control bit CST2 in the corresponding word in UPM	20.73	_	16.75		13.00		9.36	_	ns

Table 7. Bus Operation Timings (continued)



	Characteristic	33	MHz	40 MHz		50 MHz		66 MHz		11
NUM		Min	Max	Min	Max	Min	Max	Min	Max	Unit
B35	A(0:31), BADDR(28:30) to \overline{CS} valid—as requested by control bit BST4 in the corresponding word in UPM	5.58	_	4.25	_	3.00	_	1.79	_	ns
B35a	A(0:31), BADDR(28:30), and D(0:31) to $\overline{\text{BS}}$ valid—as requested by control bit BST1 in the corresponding word in UPM	13.15	—	10.50	—	8.00	—	5.58	_	ns
B35b	A(0:31), BADDR(28:30), and D(0:31) to $\overline{\text{BS}}$ valid—as requested by control bit BST2 in the corresponding word in UPM	20.73	—	16.75	—	13.00	—	9.36		ns
B36	A(0:31), BADDR(28:30), and D(0:31) to GPL valid—as requested by control bit GxT4 in the corresponding word in UPM	5.58	—	4.25	—	3.00	—	1.79	_	ns
B37	UPWAIT valid to CLKOUT falling edge ⁹	6.00	—	6.00	—	6.00	—	6.00		ns
B38	CLKOUT falling edge to UPWAIT valid ⁹	1.00	—	1.00	_	1.00	_	1.00	_	ns
B39	AS valid to CLKOUT rising edge ¹⁰	7.00	_	7.00	_	7.00	_	7.00	_	ns
B40	A(0:31), TSIZ(0:1), RD/WR, BURST, valid to CLKOUT rising edge	7.00	—	7.00	—	7.00	—	7.00	_	ns
B41	$\overline{\text{TS}}$ valid to CLKOUT rising edge (setup time)	7.00	—	7.00	_	7.00	_	7.00	_	ns
B42	CLKOUT rising edge to \overline{TS} valid (hold time)	2.00	—	2.00	—	2.00	—	2.00	_	ns
B43	AS negation to memory controller signals negation	_	TBD	_	TBD	_	TBD	_	TBD	ns

¹ Phase and frequency jitter performance results are only valid if the input jitter is less than the prescribed value.

² If the rate of change of the frequency of EXTAL is slow (that is, it does not jump between the minimum and maximum values in one cycle) or the frequency of the jitter is fast (that is, it does not stay at an extreme value for a long time) then the maximum allowed jitter on EXTAL can be up to 2%.

³ The timings specified in B4 and B5 are based on full strength clock.

⁴ The timing for BR output is relevant when the MPC860 is selected to work with external bus arbiter. The timing for BG output is relevant when the MPC860 is selected to work with internal bus arbiter.

⁵ The timing required for BR input is relevant when the MPC860 is selected to work with internal bus arbiter. The timing for BG input is relevant when the MPC860 is selected to work with external bus arbiter.

⁶ The D(0:31) and DP(0:3) input timings B18 and B19 refer to the rising edge of the CLKOUT in which the TA input signal is asserted.

⁷ The D(0:31) and DP(0:3) input timings B20 and B21 refer to the falling edge of the CLKOUT. This timing is valid only for read accesses controlled by chip-selects under control of the UPM in the memory controller, for data beats where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

⁸ The timing B30 refers to \overline{CS} when ACS = 00 and to $\overline{WE}(0:3)$ when CSNT = 0.

⁹ The signal UPWAIT is considered asynchronous to the CLKOUT and synchronized internally. The timings specified in B37 and B38 are specified to enable the freeze of the UPM output signals as described in Figure 18.

¹⁰ The AS signal is considered asynchronous to the CLKOUT. The timing B39 is specified in order to allow the behavior specified in Figure 21.



Figure 5 provides the timing for the synchronous output signals.



Figure 5. Synchronous Output Signals Timing

Figure 6 provides the timing for the synchronous active pull-up and open-drain output signals.



Figure 6. Synchronous Active Pull-Up Resistor and Open-Drain Outputs Signals Timing





Figure 15. External Bus Write Timing (GPCM Controlled—TRLX = 0 or 1, CSNT = 1)



Table 9 shows the PCMCIA timing for the MPC860.

Table 9. PCMCIA Timing

Num	Obevectovictic	33 MHz		40 MHz		50 MHz		66 MHz		11
Num	Characteristic	Min	Max	Min	Max	Min	Max	Min	Max	Unit
P44	A(0:31), REG valid to PCMCIA Strobe asserted ¹	20.73	—	16.75	—	13.00	—	9.36	—	ns
P45	A(0:31), $\overline{\text{REG}}$ valid to ALE negation ¹	28.30	—	23.00	—	18.00	—	13.15	—	ns
P46	CLKOUT to REG valid	7.58	15.58	6.25	14.25	5.00	13.00	3.79	11.84	ns
P47	CLKOUT to REG invalid	8.58	—	7.25	—	6.00	—	4.84	—	ns
P48	CLKOUT to $\overline{CE1}$, $\overline{CE2}$ asserted	7.58	15.58	6.25	14.25	5.00	13.00	3.79	11.84	ns
P49	CLKOUT to $\overline{CE1}$, $\overline{CE2}$ negated	7.58	15.58	6.25	14.25	5.00	13.00	3.79	11.84	ns
P50	CLKOUT to PCOE, IORD, PCWE, IOWR assert time	—	11.00		11.00	—	11.00	—	11.00	ns
P51	CLKOUT to PCOE, IORD, PCWE, IOWR negate time	2.00	11.00	2.00	11.00	2.00	11.00	2.00	11.00	ns
P52	CLKOUT to ALE assert time	7.58	15.58	6.25	14.25	5.00	13.00	3.79	10.04	ns
P53	CLKOUT to ALE negate time	—	15.58		14.25	_	13.00	—	11.84	ns
P54	PCWE, IOWR negated to D(0:31) invalid ¹	5.58	—	4.25	—	3.00	—	1.79	—	ns
P55	WAITA and WAITB valid to CLKOUT rising edge ¹	8.00	—	8.00	—	8.00	—	8.00	—	ns
P56	CLKOUT rising edge to WAITA and WAITB invalid ¹	2.00	—	2.00	—	2.00	—	2.00	—	ns

¹ PSST = 1. Otherwise add PSST times cycle time.

PSHT = 0. Otherwise add PSHT times cycle time.

These synchronous timings define when the WAITx signals are detected in order to freeze (or relieve) the PCMCIA current cycle. The WAITx assertion will be effective only if it is detected 2 cycles before the PSL timer expiration. See Chapter 16, "PCMCIA Interface," in the *MPC860 PowerQUICCTM Family User's Manual*.





Figure 25 provides the PCMCIA access cycle timing for the external bus read.

Figure 25. PCMCIA Access Cycle Timing External Bus Read



Table 12 shows the reset timing for the MPC860.

Table 12. Reset Timing

Num	Characteristic	33 N	/IHz	40 N	ЛНz	50 N	ЛНz	66 N	ΛHz	llmit
Num	Characteristic	Min	Max	Min	Max	Min	Max	Min	Max	Unit
R69	CLKOUT to HRESET high impedance	—	20.00	—	20.00	—	20.00	—	20.00	ns
R70	CLKOUT to SRESET high impedance	—	20.00	—	20.00	—	20.00	—	20.00	ns
R71	RSTCONF pulse width	515.15	_	425.00		340.00	_	257.58	_	ns
R72	_		_	_	_	_	_		_	
R73	Configuration data to HRESET rising edge setup time	504.55	_	425.00		350.00	_	277.27	_	ns
R74	Configuration data to RSTCONF rising edge setup time	350.00	—	350.00	—	350.00	—	350.00	—	ns
R75	Configuration data hold time after RSTCONF negation	0.00	—	0.00	—	0.00	—	0.00	—	ns
R76	Configuration data hold time after HRESET negation	0.00	—	0.00	—	0.00	—	0.00	—	ns
R77	HRESET and RSTCONF asserted to data out drive	-	25.00		25.00	—	25.00	—	25.00	ns
R78	RSTCONF negated to data out high impedance	—	25.00	_	25.00	_	25.00	_	25.00	ns
R79	CLKOUT of last rising edge before chip three-state HRESET to data out high impedance	_	25.00	—	25.00	_	25.00	_	25.00	ns
R80	DSDI, DSCK setup	90.91	—	75.00	—	60.00	—	45.45	—	ns
R81	DSDI, DSCK hold time	0.00	—	0.00	_	0.00	_	0.00	—	ns
R82	SRESET negated to CLKOUT rising edge for DSDI and DSCK sample	242.42	_	200.00		160.00		121.21	_	ns



Figure 32 shows the reset timing for the data bus configuration.



Figure 32. Reset Timing—Configuration from Data Bus

Figure 33 provides the reset timing for the data bus weak drive during configuration.



Figure 33. Reset Timing—Data Bus Weak Drive During Configuration





Figure 34 provides the reset timing for the debug port configuration.

Figure 34. Reset Timing—Debug Port Configuration

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Table 13 provides the JTAG timings for the MPC860 shown in Figure 35 through Figure 38.

Num	um Characteristic	All Freq	uencies	Unit
Nulli	Characteristic	Min	Мах	Onit
J82	TCK cycle time	100.00	—	ns
J83	TCK clock pulse width measured at 1.5 V	40.00	_	ns
J84	TCK rise and fall times	0.00	10.00	ns
J85	TMS, TDI data setup time	5.00	—	ns
J86	TMS, TDI data hold time	25.00	_	ns
J87	TCK low to TDO data valid	—	27.00	ns
J88	TCK low to TDO data invalid	0.00	—	ns
J89	TCK low to TDO high impedance	—	20.00	ns
J90	TRST assert time	100.00	_	ns
J91	TRST setup time to TCK low	40.00	—	ns
J92	TCK falling edge to output valid	—	50.00	ns
J93	TCK falling edge to output valid out of high impedance	—	50.00	ns
J94	TCK falling edge to output high impedance	—	50.00	ns
J95	Boundary scan input valid to TCK rising edge	50.00	—	ns
J96	TCK rising edge to boundary scan input invalid	50.00		ns

Table 13. JTAG Timing



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Figure 35. JTAG Test Clock Input Timing



Figure 36. JTAG Test Access Port Timing Diagram



Figure 37. JTAG TRST Timing Diagram





Num	Charactariatia	All Freq	Unit	
	Characteristic	Min	Мах	Unit
42	SDACK assertion delay from clock high	—	12	ns
43	SDACK negation delay from clock low	—	12	ns
44	SDACK negation delay from TA low	—	20	ns
45	SDACK negation delay from clock high	_	15	ns
46	\overline{TA} assertion to rising edge of the clock setup time (applies to external \overline{TA})	7		ns

Table 16. IDMA Controller Timing (continued)



Figure 45. IDMA External Requests Timing Diagram



Figure 46. SDACK Timing Diagram—Peripheral Write, Externally-Generated TA









Figure 56 through Figure 58 show the NMSI timings.





Num	Chavastavistia	All Freq	Unit	
	Characteristic	Min	Мах	Cint
135	RSTRT active delay (from TCLK1 falling edge)	10	50	ns
136	RSTRT inactive delay (from TCLK1 falling edge)	10	50	ns
137	REJECT width low	1	—	CLK
138	CLKO1 low to SDACK asserted ²		20	ns
139	CLKO1 low to SDACK negated ²	_	20	ns

Table 22. Ethernet Timing (continued)

¹ The ratios SYNCCLK/RCLK1 and SYNCCLK/TCLK1 must be greater than or equal to 2/1.

² SDACK is asserted whenever the SDMA writes the incoming frame DA into memory.



Figure 59. Ethernet Collision Timing Diagram



Figure 60. Ethernet Receive Timing Diagram



CPM Electrical Characteristics







11.11 SPI Slave AC Electrical Specifications

Table 25 provides the SPI slave timings as shown in Figure 67 and Figure 68.

Table 25. SPI Slave Timing

Num	Characteristic	All Freq	Unit	
Nulli		Min	Мах	Unit
170	Slave cycle time	2	_	t _{cyc}
171	Slave enable lead time	15	—	ns
172	Slave enable lag time	15	—	ns
173	Slave clock (SPICLK) high or low time	1	—	t _{cyc}
174	Slave sequential transfer delay (does not require deselect)	1	_	t _{cyc}
175	Slave data setup time (inputs)	20	—	ns
176	Slave data hold time (inputs)	20	—	ns
177	Slave access time	—	50	ns



11.12 I²C AC Electrical Specifications

Table 26 provides the I^2C (SCL < 100 kHz) timings.

Table 26. I²C Timing (SCL < 100 kHz)

Num	Characteristic	All Freq	uencies	Unit
Nulli		Min	Мах	Unit
200	SCL clock frequency (slave)	0	100	kHz
200	SCL clock frequency (master) ¹	1.5	100	kHz
202	Bus free time between transmissions	4.7	—	μS
203	Low period of SCL	4.7	—	μS
204	High period of SCL	4.0	—	μS
205	Start condition setup time	4.7	—	μS
206	Start condition hold time	4.0	—	μS
207	Data hold time	0	—	μS
208	Data setup time	250	—	ns
209	SDL/SCL rise time	—	1	μS
210	SDL/SCL fall time	—	300	ns
211	Stop condition setup time	4.7	—	μS

SCL frequency is given by SCL = BRGCLK_frequency / ((BRG register + 3 × pre_scaler × 2). The ratio SYNCCLK/(BRGCLK/pre_scaler) must be greater than or equal to 4/1.

Table 27 provides the I^2C (SCL > 100 kHz) timings.

Table 27. . I²C Timing (SCL > 100 kHz)

Num	Characteristic	Expression	All Freq	Unit	
Num	Characteristic	Expression	Min	Мах	Unit
200	SCL clock frequency (slave)	fSCL	0	BRGCLK/48	Hz
200	SCL clock frequency (master) ¹	fSCL	BRGCLK/16512	BRGCLK/48	Hz
202	Bus free time between transmissions		1/(2.2 * fSCL)	—	S
203	Low period of SCL		1/(2.2 * fSCL)	—	S
204	High period of SCL		1/(2.2 * fSCL)	_	S
205	Start condition setup time		1/(2.2 * fSCL)	—	S
206	Start condition hold time		1/(2.2 * fSCL)	—	S
207	Data hold time		0	_	S
208	Data setup time		1/(40 * fSCL)	—	S
209	SDL/SCL rise time		—	1/(10 * fSCL)	S
210	SDL/SCL fall time		—	1/(33 * fSCL)	S
211	Stop condition setup time		1/2(2.2 * fSCL)	—	s

SCL frequency is given by SCL = BRGCLK_frequency / ((BRG register + 3) × pre_scaler × 2). The ratio SYNCCLK/(BRGCLK / pre_scaler) must be greater than or equal to 4/1.



13.2 MII Transmit Signal Timing (MII_TXD[3:0], MII_TX_EN, MII_TX_ER, MII_TX_CLK)

The transmitter functions correctly up to a MII_TX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed the MII_TX_CLK frequency -1%.

Table 30 provides information on the MII transmit signal timing.

Table 30. MI	Transmit	Signal	Timing
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Num	Characteristic	Min	Max	Unit
M5	MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER invalid	5	_	ns
M6	MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER valid		25	
M7	MII_TX_CLK pulse width high	35	65%	MII_TX_CLK period
M8	MII_TX_CLK pulse width low	35%	65%	MII_TX_CLK period

Figure 73 shows the MII transmit signal timing diagram.



Figure 73. MII Transmit Signal Timing Diagram



13.3 MII Async Inputs Signal Timing (MII_CRS, MII_COL)

Table 31 provides information on the MII async inputs signal timing.

Table 31. MII Async Inputs Signal Timing

Num	Characteristic	Min	Мах	Unit
M9	MII_CRS, MII_COL minimum pulse width	1.5		MII_TX_CLK period

Figure 74 shows the MII asynchronous inputs signal timing diagram.



13.4 MII Serial Management Channel Timing (MII_MDIO, MII_MDC)

Table 32 provides information on the MII serial management channel signal timing. The FEC functions correctly with a maximum MDC frequency in excess of 2.5 MHz. The exact upper bound is under investigation.

Num	Characteristic	Min	Мах	Unit
M10	MII_MDC falling edge to MII_MDIO output invalid (minimum propagation delay)	0	_	ns
M11	MII_MDC falling edge to MII_MDIO output valid (max prop delay)	_	25	ns
M12	MII_MDIO (input) to MII_MDC rising edge setup	10	—	ns
M13	MII_MDIO (input) to MII_MDC rising edge hold	0	—	ns
M14	MII_MDC pulse width high	40%	60%	MII_MDC period
M15	MII_MDC pulse width low	40%	60%	MII_MDC period

Table 32. MII Serial Management Channel Timing



Mechanical Data and Ordering Information

Figure 75 shows the MII serial management channel timing diagram.



Figure 75. MII Serial Management Channel Timing Diagram

14 Mechanical Data and Ordering Information

14.1 Ordering Information

Table 33 provides information on the MPC860 Revision D.4 derivative devices.

Device	Number of SCCs ¹	Ethernet Support ² (Mbps)	Multichannel HDLC Support	ATM Support
MPC855T	1	10/100	Yes	Yes
MPC860DE	2	10	N/A	N/A
MPC860DT		10/100	Yes	Yes
MPC860DP		10/100	Yes	Yes
MPC860EN	4	10	N/A	N/A
MPC860SR		10	Yes	Yes
MPC860T		10/100	Yes	Yes
MPC860P		10/100	Yes	Yes

Table 33. MPC860 Family Revision D.4 Derivatives

¹ Serial communications controller (SCC)

² Up to 4 channels at 40 MHz or 2 channels at 25 MHz