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#### Understanding Embedded - Microprocessors

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#### Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

#### Details

Obsolete
MPC8xx
1 Core, 32-Bit
80MHz
Communications; CPM
DRAM
No
-
10Mbps (4)
-
·
3.3V
0°C ~ 95°C (TA)
-
357-BBGA
357-PBGA (25x25)
https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc860enzq80d4

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Overview

# 1 Overview

The MPC860 power quad integrated communications controller (PowerQUICC<sup>TM</sup>) is a versatile one-chip integrated microprocessor and peripheral combination designed for a variety of controller applications. It particularly excels in communications and networking systems. The PowerQUICC unit is referred to as the MPC860 in this hardware specification.

The MPC860 implements Power Architecture<sup>TM</sup> technology and contains a superset of Freescale's MC68360 quad integrated communications controller (QUICC), referred to here as the QUICC, RISC communications proceessor module (CPM). The CPU on the MPC860 is a 32-bit core built on Power Architecture technology that incorporates memory management units (MMUs) and instruction and data caches.. The CPM from the MC68360 QUICC has been enhanced by the addition of the inter-integrated controller (I<sup>2</sup>C) channel. The memory controller has been enhanced, enabling the MPC860 to support any type of memory, including high-performance memories and new types of DRAMs. A PCMCIA socket controller supports up to two sockets. A real-time clock has also been integrated.

Table 1 shows the functionality supported by the MPC860 family.

Part	Cache (Kbytes)		Ethe	ernet			
	Instruction Cache	Data Cache	10T	10/100	ΑΤΜ	SCC	Reference <sup>1</sup>
MPC860DE	4	4	Up to 2	_	_	2	1
MPC860DT	4	4	Up to 2	1	Yes	2	1
MPC860DP	16	8	Up to 2	1	Yes	2	1
MPC860EN	4	4	Up to 4	—	—	4	1
MPC860SR	4	4	Up to 4	—	Yes	4	1
MPC860T	4	4	Up to 4	1	Yes	4	1
MPC860P	16	8	Up to 4	1	Yes	4	1
MPC855T	4	4	1	1	Yes	1	2

Table 1. MPC860 Family Functionality

Supporting documentation for these devices refers to the following:

1. MPC860 PowerQUICC Family User's Manual (MPC860UM, Rev. 3)

2. MPC855T User's Manual (MPC855TUM, Rev. 1)



## 2 Features

The following list summarizes the key MPC860 features:

- Embedded single-issue, 32-bit core (implementing the Power Architecture technology) with thirty-two 32-bit general-purpose registers (GPRs)
  - The core performs branch prediction with conditional prefetch without conditional execution.
  - 4- or 8-Kbyte data cache and 4- or 16-Kbyte instruction cache (see Table 1)
    - 16-Kbyte instruction caches are four-way, set-associative with 256 sets; 4-Kbyte instruction caches are two-way, set-associative with 128 sets.
    - 8-Kbyte data caches are two-way, set-associative with 256 sets; 4-Kbyte data caches are two-way, set-associative with 128 sets.
    - Cache coherency for both instruction and data caches is maintained on 128-bit (4-word) cache blocks.
    - Caches are physically addressed, implement a least recently used (LRU) replacement algorithm, and are lockable on a cache block basis.
  - MMUs with 32-entry TLB, fully-associative instruction, and data TLBs
  - MMUs support multiple page sizes of 4-, 16-, and 512-Kbytes, and 8-Mbytes; 16 virtual address spaces and 16 protection groups
  - Advanced on-chip-emulation debug mode
- Up to 32-bit data bus (dynamic bus sizing for 8, 16, and 32 bits)
- 32 address lines
- Operates at up to 80 MHz
- Memory controller (eight banks)
  - Contains complete dynamic RAM (DRAM) controller
  - Each bank can be a chip select or  $\overline{RAS}$  to support a DRAM bank.
  - Up to 15 wait states programmable per memory bank
  - Glueless interface to DRAM, SIMMS, SRAM, EPROM, Flash EPROM, and other memory devices
  - DRAM controller programmable to support most size and speed memory interfaces
  - Four  $\overline{\text{CAS}}$  lines, four  $\overline{\text{WE}}$  lines, and one  $\overline{\text{OE}}$  line
  - Boot chip-select available at reset (options for 8-, 16-, or 32-bit memory)
  - Variable block sizes (32 Kbytes to 256 Mbytes)
  - Selectable write protection
  - On-chip bus arbitration logic
- General-purpose timers
  - Four 16-bit timers or two 32-bit timers
  - Gate mode can enable/disable counting
  - Interrupt can be masked on reference match and event capture.



#### Table 4 shows the thermal characteristics for the MPC860.

#### Table 4. MPC860 Thermal Resistance Data

Rating	Env	ironment	Symbol	ZP MPC860P	ZQ / VR MPC860P	Unit
Mold Compound Thicknes	s			0.85	1.15	mm
Junction-to-ambient <sup>1</sup>	Natural convection	Single-layer board (1s)	$R_{\theta JA}^2$	34	34	°C/W
		Four-layer board (2s2p)	$R_{\theta JMA}^{3}$	22	22	
	Airflow (200 ft/min)	Single-layer board (1s)	$R_{\theta JMA}^{3}$	27	27	
		Four-layer board (2s2p)	$R_{\theta JMA}^{3}$	18	18	
Junction-to-board <sup>4</sup>			$R_{\theta JB}$	14	13	
Junction-to-case <sup>5</sup>			$R_{\thetaJC}$	6	8	
Junction-to-package top <sup>6</sup>	Natural convection		$\Psi_{JT}$	2	2	

<sup>1</sup> Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.

<sup>2</sup> Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.

<sup>3</sup> Per JEDEC JESD51-6 with the board horizontal.

<sup>4</sup> Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

- <sup>5</sup> Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature. For exposed pad packages where the pad would be expected to be soldered, junction-to-case thermal resistance is a simulated value from the junction to the exposed pad without contact resistance.
- <sup>6</sup> Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2.



**Thermal Calculation and Measurement** 

# 7 Thermal Calculation and Measurement

For the following discussions,  $P_D = (V_{DD} \times I_{DD}) + PI/O$ , where PI/O is the power dissipation of the I/O drivers.

### 7.1 Estimation with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T<sub>J</sub>, in °C can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

 $T_A$  = ambient temperature (°C)

 $R_{\theta JA}$  = package junction-to-ambient thermal resistance (°C/W)

 $P_D$  = power dissipation in package

The junction-to-ambient thermal resistance is an industry standard value which provides a quick and easy estimation of thermal performance. However, the answer is only an estimate; test cases have demonstrated that errors of a factor of two (in the quantity  $T_J - T_A$ ) are possible.

### 7.2 Estimation with Junction-to-Case Thermal Resistance

Historically, the thermal resistance has frequently been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

 $R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$ 

where:

 $R_{\theta JA}$  = junction-to-ambient thermal resistance (°C/W)

 $R_{\theta IC}$  = junction-to-case thermal resistance (°C/W)

 $R_{\theta CA}$  = case-to-ambient thermal resistance (°C/W)

 $R_{\theta JC}$  is device related and cannot be influenced by the user. The user adjusts the thermal environment to affect the case-to-ambient thermal resistance,  $R_{\theta CA}$ . For instance, the user can change the airflow around the device, add a heat sink, change the mounting arrangement on the printed-circuit board, or change the thermal dissipation on the printed-circuit board surrounding the device. This thermal model is most useful for ceramic packages with heat sinks where some 90% of the heat flows through the case and the heat sink to the ambient environment. For most packages, a better model is required.

## 7.3 Estimation with Junction-to-Board Thermal Resistance

A simple package thermal model which has demonstrated reasonable accuracy (about 20%) is a two-resistor model consisting of a junction-to-board and a junction-to-case thermal resistance. The junction-to-case thermal resistance covers the situation where a heat sink is used or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed-circuit board. It has been observed that the thermal performance of most plastic packages, especially PBGA packages, is strongly dependent on the board temperature; see Figure 2.



Layout Practices

where:

 $\Psi_{JT}$  = thermal characterization parameter

 $T_T$  = thermocouple temperature on top of package

 $P_D$  = power dissipation in package

The thermal characterization parameter is measured per JEDEC JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

## 7.6 References

Semiconductor Equipment and Materials International	(415) 964-5111
805 East Middlefield Rd.	
Mountain View, CA 94043	
MIL-SPEC and EIA/JESD (JEDEC) Specifications	800-854-7179 or
(Available from Global Engineering Documents)	303-397-7956
JEDEC Specifications	http://www.jedec.org

- 1. C.E. Triplett and B. Joiner, "An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module," Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.
- B. Joiner and V. Adams, "Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling," Proceedings of SemiTherm, San Diego, 1999, pp. 212–220.

# 8 Layout Practices

Each  $V_{DD}$  pin on the MPC860 should be provided with a low-impedance path to the board's supply. Each GND pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on the chip. The  $V_{DD}$  power supply should be bypassed to ground using at least four 0.1 µF-bypass capacitors located as close as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to chip  $V_{DD}$  and GND should be kept to less than half an inch per capacitor lead. A four-layer board employing two inner layers as  $V_{CC}$  and GND planes is recommended.

All output pins on the MPC860 have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized in order to minimize undershoot and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data buses. Maximum PC trace lengths of 6 inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the  $V_{CC}$  and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.



	Chavastavistis	33	MHz	40 MHz		50 MHz		66 MHz		
Num	Characteristic	Min	Мах	Min	Мах	Min	Мах	Min	Max	Unit
B29d	$\overline{WE}(0:3)$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 0	43.45		35.5	_	28.00		20.73	_	ns
B29e	$\overline{\text{CS}}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 0	43.45		35.5		28.00		29.73	_	ns
B29f	$\overline{WE}$ (0:3) negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 1	8.86		6.88	_	5.00	_	3.18		ns
B29g	$\overline{\text{CS}}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 1	8.86	_	6.88	—	5.00	—	3.18	_	ns
B29h	$\overline{WE}(0:3)$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 1	38.67	—	31.38	—	24.50	—	17.83	_	ns
B29i	$\overline{\text{CS}}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 1	38.67		31.38		24.50		17.83	_	ns
B30	$\overline{CS}$ , $\overline{WE}$ (0:3) negated to A(0:31), BADDR(28:30) invalid GPCM write access <sup>8</sup>	5.58	—	4.25	—	3.00	—	1.79		ns
B30a	$\overline{\text{WE}}(0:3)$ negated to A(0:31), BADDR(28:30) invalid GPCM, write access, TRLX = 0, CSNT = 1, $\overline{\text{CS}}$ negated to A(0:31) invalid GPCM write access, TRLX = 0, CSNT = 1 ACS = 10, or ACS = 11, EBDF = 0	13.15	_	10.50	_	8.00	_	5.58		ns
B30b	$\label{eq:weighted} \hline WE(0:3) \ negated to \ A(0:31), \ invalid \ GPCM \\ BADDR(28:30) \ invalid \ GPCM \ write \ access, \\ TRLX = 1, \ CSNT = 1. \ \overline{CS} \ negated to \\ A(0:31), \ Invalid \ GPCM, \ write \ access, \\ TRLX = 1, \ CSNT = 1, \ ACS = 10, \ or \\ ACS = 11, \ EBDF = 0 \\ \hline \hline \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \$	43.45	_	35.50	_	28.00	_	20.73	_	ns
B30c	$\label{eq:weighted} \begin{array}{ c c c c } \hline WE(0:3) \mbox{ negated to } A(0:31), \mbox{ BADDR}(28:30) \\ \hline \mbox{ invalid GPCM write access, TRLX = 0, } \\ \hline CSNT = 1. \end{cmathcelline CS} \mbox{ negated to } A(0:31) \mbox{ invalid GPCM write access, TRLX = 0, } \\ \hline GPCM \mbox{ write access, TRLX = 0, } \\ \hline ACS = 10, \mbox{ ACS = 11, EBDF = 1} \end{array}$	8.36	_	6.38	_	4.50	_	2.68		ns
B30d	$\overline{WE}(0:3)$ negated to A(0:31), BADDR(28:30) invalid GPCM write access, TRLX = 1, CSNT =1. $\overline{CS}$ negated to A(0:31) invalid GPCM write access TRLX = 1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 1	38.67	_	31.38	_	24.50	_	17.83		ns
B31	CLKOUT falling edge to CS valid—as requested by control bit CST4 in the corresponding word in UPM	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns

#### Table 7. Bus Operation Timings (continued)



	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		11
NUM	Characteristic	Min	Max	Min	Max	Min	Max	Min	Max	Unit
B35	A(0:31), BADDR(28:30) to $\overline{CS}$ valid—as requested by control bit BST4 in the corresponding word in UPM	5.58	_	4.25	_	3.00	_	1.79	_	ns
B35a	A(0:31), BADDR(28:30), and D(0:31) to $\overline{\text{BS}}$ valid—as requested by control bit BST1 in the corresponding word in UPM	13.15	—	10.50	—	8.00	—	5.58	_	ns
B35b	A(0:31), BADDR(28:30), and D(0:31) to $\overline{\text{BS}}$ valid—as requested by control bit BST2 in the corresponding word in UPM	20.73	—	16.75	—	13.00	—	9.36		ns
B36	A(0:31), BADDR(28:30), and D(0:31) to GPL valid—as requested by control bit GxT4 in the corresponding word in UPM	5.58	—	4.25	—	3.00	—	1.79	_	ns
B37	UPWAIT valid to CLKOUT falling edge <sup>9</sup>	6.00	—	6.00	—	6.00	—	6.00		ns
B38	CLKOUT falling edge to UPWAIT valid <sup>9</sup>	1.00	—	1.00	_	1.00	_	1.00	_	ns
B39	AS valid to CLKOUT rising edge <sup>10</sup>	7.00	_	7.00	_	7.00	_	7.00	_	ns
B40	A(0:31), TSIZ(0:1), RD/WR, BURST, valid to CLKOUT rising edge	7.00	—	7.00	—	7.00	—	7.00	_	ns
B41	$\overline{\text{TS}}$ valid to CLKOUT rising edge (setup time)	7.00	—	7.00	_	7.00	_	7.00	_	ns
B42	CLKOUT rising edge to $\overline{TS}$ valid (hold time)	2.00	—	2.00	—	2.00	—	2.00	_	ns
B43	AS negation to memory controller signals negation	_	TBD	_	TBD	_	TBD	_	TBD	ns

<sup>1</sup> Phase and frequency jitter performance results are only valid if the input jitter is less than the prescribed value.

<sup>2</sup> If the rate of change of the frequency of EXTAL is slow (that is, it does not jump between the minimum and maximum values in one cycle) or the frequency of the jitter is fast (that is, it does not stay at an extreme value for a long time) then the maximum allowed jitter on EXTAL can be up to 2%.

<sup>3</sup> The timings specified in B4 and B5 are based on full strength clock.

<sup>4</sup> The timing for BR output is relevant when the MPC860 is selected to work with external bus arbiter. The timing for BG output is relevant when the MPC860 is selected to work with internal bus arbiter.

<sup>5</sup> The timing required for BR input is relevant when the MPC860 is selected to work with internal bus arbiter. The timing for BG input is relevant when the MPC860 is selected to work with external bus arbiter.

<sup>6</sup> The D(0:31) and DP(0:3) input timings B18 and B19 refer to the rising edge of the CLKOUT in which the TA input signal is asserted.

<sup>7</sup> The D(0:31) and DP(0:3) input timings B20 and B21 refer to the falling edge of the CLKOUT. This timing is valid only for read accesses controlled by chip-selects under control of the UPM in the memory controller, for data beats where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

<sup>8</sup> The timing B30 refers to  $\overline{CS}$  when ACS = 00 and to  $\overline{WE}(0:3)$  when CSNT = 0.

<sup>9</sup> The signal UPWAIT is considered asynchronous to the CLKOUT and synchronized internally. The timings specified in B37 and B38 are specified to enable the freeze of the UPM output signals as described in Figure 18.

<sup>10</sup> The AS signal is considered asynchronous to the CLKOUT. The timing B39 is specified in order to allow the behavior specified in Figure 21.





Figure 15. External Bus Write Timing (GPCM Controlled—TRLX = 0 or 1, CSNT = 1)







Figure 16. External Bus Write Timing (GPCM Controlled—TRLX = 0 or 1, CSNT = 1)



#### Table 9 shows the PCMCIA timing for the MPC860.

Table 9. PCMCIA Timing

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		11
Num		Min	Max	Min	Max	Min	Max	Min	Max	Unit
P44	A(0:31), REG valid to PCMCIA Strobe asserted <sup>1</sup>	20.73	—	16.75	—	13.00	—	9.36	—	ns
P45	A(0:31), $\overline{\text{REG}}$ valid to ALE negation <sup>1</sup>	28.30	—	23.00	—	18.00	—	13.15	_	ns
P46	CLKOUT to REG valid	7.58	15.58	6.25	14.25	5.00	13.00	3.79	11.84	ns
P47	CLKOUT to REG invalid	8.58	—	7.25	—	6.00	—	4.84	_	ns
P48	CLKOUT to $\overline{CE1}$ , $\overline{CE2}$ asserted	7.58	15.58	6.25	14.25	5.00	13.00	3.79	11.84	ns
P49	CLKOUT to $\overline{CE1}$ , $\overline{CE2}$ negated	7.58	15.58	6.25	14.25	5.00	13.00	3.79	11.84	ns
P50	CLKOUT to PCOE, IORD, PCWE, IOWR assert time	—	11.00		11.00	—	11.00	—	11.00	ns
P51	CLKOUT to PCOE, IORD, PCWE, IOWR negate time	2.00	11.00	2.00	11.00	2.00	11.00	2.00	11.00	ns
P52	CLKOUT to ALE assert time	7.58	15.58	6.25	14.25	5.00	13.00	3.79	10.04	ns
P53	CLKOUT to ALE negate time	—	15.58		14.25	_	13.00	—	11.84	ns
P54	PCWE, IOWR negated to D(0:31) invalid <sup>1</sup>	5.58	—	4.25	—	3.00	—	1.79	—	ns
P55	WAITA and WAITB valid to CLKOUT rising edge <sup>1</sup>	8.00	—	8.00	—	8.00	—	8.00	—	ns
P56	CLKOUT rising edge to WAITA and WAITB invalid <sup>1</sup>	2.00	—	2.00	—	2.00	—	2.00	—	ns

<sup>1</sup> PSST = 1. Otherwise add PSST times cycle time.

PSHT = 0. Otherwise add PSHT times cycle time.

These synchronous timings define when the WAITx signals are detected in order to freeze (or relieve) the PCMCIA current cycle. The WAITx assertion will be effective only if it is detected 2 cycles before the PSL timer expiration. See Chapter 16, "PCMCIA Interface," in the *MPC860 PowerQUICCTM Family User's Manual*.



Table 11 shows the debug port timing for the MPC860.

Table 11. Debug Port Timing

Num	Chavastaviatia	All Freq	Unit	
	Characteristic	Min	Мах	Unit
P61	DSCK cycle time	$3 \times T_{CLOCKOUT}$	_	
P62	DSCK clock pulse width	$1.25 \times T_{CLOCKOUT}$	—	—
P63	DSCK rise and fall times	0.00	3.00	ns
P64	DSDI input data setup time	8.00	—	ns
P65	DSDI data hold time	5.00	—	ns
P66	DSCK low to DSDO data valid	0.00	15.00	ns
P67	DSCK low to DSDO invalid	0.00	2.00	ns

Figure 30 provides the input timing for the debug port clock.



Figure 30. Debug Port Clock Input Timing

Figure 31 provides the timing for the debug port.



Figure 31. Debug Port Timings



**CPM Electrical Characteristics** 

Figure 56 through Figure 58 show the NMSI timings.





**CPM Electrical Characteristics** 





**CPM Electrical Characteristics** 





# **13 FEC Electrical Characteristics**

This section provides the AC electrical specifications for the Fast Ethernet controller (FEC). Note that the timing specifications for the MII signals are independent of system clock frequency (part speed designation). Also, MII signals use TTL signal levels compatible with devices operating at either 5.0 V or 3.3 V.

# 13.1 MII Receive Signal Timing (MII\_RXD[3:0], MII\_RX\_DV, MII\_RX\_ER, MII\_RX\_CLK)

The receiver functions correctly up to a MII\_RX\_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed the MII\_RX\_CLK frequency - 1%.

Table 29 provides information on the MII receive signal timing.

Num	Characteristic	Min	Max	Unit
M1	MII_RXD[3:0], MII_RX_DV, MII_RX_ER to MII_RX_CLK setup	5		ns
M2	MII_RX_CLK to MII_RXD[3:0], MII_RX_DV, MII_RX_ER hold	5		ns
M3	MII_RX_CLK pulse width high	35%	65%	MII_RX_CLK period
M4	MII_RX_CLK pulse width low	35%	65%	MII_RX_CLK period

#### Table 29. Mll Receive Signal Timing

Figure 72 shows MII receive signal timing.



Figure 72. MII Receive Signal Timing Diagram



FEC Electrical Characteristics

# 13.2 MII Transmit Signal Timing (MII\_TXD[3:0], MII\_TX\_EN, MII\_TX\_ER, MII\_TX\_CLK)

The transmitter functions correctly up to a MII\_TX\_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed the MII\_TX\_CLK frequency -1%.

Table 30 provides information on the MII transmit signal timing.

Table 30. MI	Transmit	Signal	Timing
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Num	Characteristic	Min	Max	Unit
M5	MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER invalid	5	_	ns
M6	MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER valid		25	
M7	MII_TX_CLK pulse width high	35	65%	MII_TX_CLK period
M8	MII_TX_CLK pulse width low	35%	65%	MII_TX_CLK period

Figure 73 shows the MII transmit signal timing diagram.



Figure 73. MII Transmit Signal Timing Diagram



#### Table 34 identifies the packages and operating frequencies available for the MPC860.

Package Type	Freq. (MHz) / Temp. (Tj)	Package	Order Number
Ball grid array ZP suffix—leaded ZQ suffix—leaded VR suffix—lead-free	50 0° to 95°C	ZP/ZQ <sup>1</sup>	MPC855TZQ50D4 MPC860DEZQ50D4 MPC860DTZQ50D4 MPC860ENZQ50D4 MPC860SRZQ50D4 MPC860TZQ50D4 MPC860DPZQ50D4 MPC860PZQ50D4
		Tape and Reel	MPC855TZQ50D4R2 MPC860DEZQ50D4R2 MPC860ENZQ50D4R2 MPC860SRZQ50D4R2 MPC860TZQ50D4R2 MPC860DPZQ50D4R2 MPC855TVR50D4R2 MPC860ENVR50D4R2 MPC860SRVR50D4R2 MPC860TVR50D4R2
		VR	MPC855TVR50D4 MPC860DEVR50D4 MPC860DPVR50D4 MPC860DTVR50D4 MPC860ENVR50D4 MPC860PVR50D4 MPC860SRVR50D4 MPC860SRVR50D4 MPC860TVR50D4
	66 0° to 95°C	ZP/ZQ <sup>1</sup>	MPC855TZQ66D4 MPC860DEZQ66D4 MPC860DTZQ66D4 MPC860ENZQ66D4 MPC860SRZQ66D4 MPC860TZQ66D4 MPC860DPZQ66D4 MPC860PZQ66D4
		Tape and Reel	MPC860SRZQ66D4R2 MPC860PZQ66D4R2
		VR	MPC855TVR66D4 MPC860DEVR66D4 MPC860DPVR66D4 MPC860DTVR66D4 MPC860ENVR66D4 MPC860PVR66D4 MPC860SRVR66D4 MPC860TVR66D4

#### Table 34. MPC860 Family Package/Frequency Availability



Mechanical Data and Ordering Information

## 14.3 Mechanical Dimensions of the PBGA Package

Figure 77 shows the mechanical dimensions of the ZP PBGA package.



- 1. Dimensions and tolerance per ASME Y14.5M, 1994.
- 2. Dimensions in millimeters.
- 3. Dimension b is the maximum solder ball diameter measured parallel to data C.



22.40

E2

22.60



Document Revision History

# **15 Document Revision History**

Table 35 lists significant changes between revisions of this hardware specification.

Revision	Date	Changes
10	09/2015	In Table 34, moved MPC855TCVR50D4 and MPC855TCVR66D4 under the extended temperature (–40° to 95°C) and removed MC860ENCVR50D4R2 from the normal temperature Tape and Reel.
9	10/2011	Updated orderable part numbers in Table 34, "MPC860 Family Package/Frequency Availability."
8	08/2007	<ul> <li>Updated template.</li> <li>On page 1, added a second paragraph.</li> <li>After Table 2, inserted a new figure showing the undershoot/overshoot voltage (Figure 1) and renumbered the rest of the figures.</li> <li>In Figure 3, changed all reference voltage measurement points from 0.2 and 0.8 V to 50% level.</li> <li>In Table 16, changed num 46 description to read, "TA assertion to rising edge"</li> <li>In Figure 46, changed TA to reflect the rising edge of the clock.</li> </ul>
7.0	9/2004	<ul> <li>Added a tablefootnote to Table 6 DC Electrical Specifications about meeting the VIL Max of the I2C Standard</li> <li>Replaced the thermal characteristics in Table 4 by the ZQ package</li> <li>Add the new parts to the Ordering and Availablity Chart in Table 34</li> <li>Added the mechanical spec of the ZQ package in Figure 78</li> <li>Removed all of the old revisions from Table 5</li> </ul>
6.3	9/2003	<ul> <li>Added Section 11.2 on the Port C interrupt pins</li> <li>Nontechnical reformatting</li> </ul>
6.2	8/2003	<ul> <li>Changed B28a through B28d and B29d to show that TRLX can be 0 or 1</li> <li>Changed reference documentation to reflect the Rev 2 MPC860 PowerQUICC Family Users Manual</li> <li>Nontechnical reformatting</li> </ul>
6.1	11/2002	<ul> <li>Corrected UTOPIA RXenb* and TXenb* timing values</li> <li>Changed incorrect usage of Vcc to Vdd</li> <li>Corrected dual port RAM to 8 Kbytes</li> </ul>
6	10/2002	Added the MPC855T. Corrected Figure 26 on page -36.
5.1	11/2001	Revised template format, removed references to MAC functionality, changed Table 7 B23 max value @ 66 MHz from 2ns to 8ns, added this revision history table

#### Table 35. Document Revision History



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