Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	66MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (4), 10/100Mbps (1)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 95°C (TA)
Security Features	-
Package / Case	357-BBGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc860pczq66d4

1 Overview

The MPC860 power quad integrated communications controller (PowerQUICC™) is a versatile one-chip integrated microprocessor and peripheral combination designed for a variety of controller applications. It particularly excels in communications and networking systems. The PowerQUICC unit is referred to as the MPC860 in this hardware specification.

The MPC860 implements Power Architecture™ technology and contains a superset of Freescale's MC68360 quad integrated communications controller (QUICC), referred to here as the QUICC, RISC communications proccessor module (CPM). The CPU on the MPC860 is a 32-bit core built on Power Architecture technology that incorporates memory management units (MMUs) and instruction and data caches.. The CPM from the MC68360 QUICC has been enhanced by the addition of the inter-integrated controller (I^2C) channel. The memory controller has been enhanced, enabling the MPC860 to support any type of memory, including high-performance memories and new types of DRAMs. A PCMCIA socket controller supports up to two sockets. A real-time clock has also been integrated.

Table 1 shows the functionality supported by the MPC860 family.

Table 1. MPC860 Family Functionality

Part	Cache (Kbytes)		Ethernet		ATM	SCC	Reference[1]
	Instruction Cache	Data Cache	10T	10/100			
MPC860DE	4	4	Up to 2	—	—	2	1
MPC860DT	4	4	Up to 2	1	Yes	2	1
MPC860DP	16	8	Up to 2	1	Yes	2	1
MPC860EN	4	4	Up to 4	—	—	4	1
MPC860SR	4	4	Up to 4	—	Yes	4	1
MPC860T	4	4	Up to 4	1	Yes	4	1
MPC860P	16	8	Up to 4	1	Yes	4	1
MPC855T	4	4	1	1	Yes	1	2

[1] Supporting documentation for these devices refers to the following:
    1. MPC860 PowerQUICC Family User's Manual (MPC860UM, Rev. 3)
    2. MPC855T User's Manual (MPC855TUM, Rev. 1)

2 Features

The following list summarizes the key MPC860 features:

- Embedded single-issue, 32-bit core (implementing the Power Architecture technology) with thirty-two 32-bit general-purpose registers (GPRs)
  - The core performs branch prediction with conditional prefetch without conditional execution.
  - 4- or 8-Kbyte data cache and 4- or 16-Kbyte instruction cache (see Table 1)
    - 16-Kbyte instruction caches are four-way, set-associative with 256 sets; 4-Kbyte instruction caches are two-way, set-associative with 128 sets.
    - 8-Kbyte data caches are two-way, set-associative with 256 sets; 4-Kbyte data caches are two-way, set-associative with 128 sets.
    - Cache coherency for both instruction and data caches is maintained on 128-bit (4-word) cache blocks.
    - Caches are physically addressed, implement a least recently used (LRU) replacement algorithm, and are lockable on a cache block basis.
  - MMUs with 32-entry TLB, fully-associative instruction, and data TLBs
  - MMUs support multiple page sizes of 4-, 16-, and 512-Kbytes, and 8-Mbytes; 16 virtual address spaces and 16 protection groups
  - Advanced on-chip-emulation debug mode
- Up to 32-bit data bus (dynamic bus sizing for 8, 16, and 32 bits)
- 32 address lines
- Operates at up to 80 MHz
- Memory controller (eight banks)
  - Contains complete dynamic RAM (DRAM) controller
  - Each bank can be a chip select or $\overline{\text{RAS}}$ to support a DRAM bank.
  - Up to 15 wait states programmable per memory bank
  - Glueless interface to DRAM, SIMMS, SRAM, EPROM, Flash EPROM, and other memory devices
  - DRAM controller programmable to support most size and speed memory interfaces
  - Four $\overline{\text{CAS}}$ lines, four $\overline{\text{WE}}$ lines, and one $\overline{\text{OE}}$ line
  - Boot chip-select available at reset (options for 8-, 16-, or 32-bit memory)
  - Variable block sizes (32 Kbytes to 256 Mbytes)
  - Selectable write protection
  - On-chip bus arbitration logic
- General-purpose timers
  - Four 16-bit timers or two 32-bit timers
  - Gate mode can enable/disable counting
  - Interrupt can be masked on reference match and event capture.

- System integration unit (SIU)
  - Bus monitor
  - Software watchdog
  - Periodic interrupt timer (PIT)
  - Low-power stop mode
  - Clock synthesizer
  - Decrementer, time base, and real-time clock (RTC)
  - Reset controller
  - IEEE 1149.1™ Std. test access port (JTAG)
- Interrupts
  - Seven external interrupt request (IRQ) lines
  - 12 port pins with interrupt capability
  - 23 internal interrupt sources
  - Programmable priority between SCCs
  - Programmable highest priority request
- 10/100 Mbps Ethernet support, fully compliant with the IEEE 802.3u® Standard (not available when using ATM over UTOPIA interface)
- ATM support compliant with ATM forum UNI 4.0 specification
  - Cell processing up to 50–70 Mbps at 50-MHz system clock
  - Cell multiplexing/demultiplexing
  - Support of AAL5 and AAL0 protocols on a per-VC basis. AAL0 support enables OAM and software implementation of other protocols.
  - ATM pace control (APC) scheduler, providing direct support for constant bit rate (CBR) and unspecified bit rate (UBR) and providing control mechanisms enabling software support of available bit rate (ABR)
  - Physical interface support for UTOPIA (10/100-Mbps is not supported with this interface) and byte-aligned serial (for example, T1/E1/ADSL)
  - UTOPIA-mode ATM supports level-1 master with cell-level handshake, multi-PHY (up to four physical layer devices), connection to 25-, 51-, or 155-Mbps framers, and UTOPIA/system clock ratios of 1/2 or 1/3.
  - Serial-mode ATM connection supports transmission convergence (TC) function for T1/E1/ADSL lines, cell delineation, cell payload scrambling/descrambling, automatic idle/unassigned cell insertion/stripping, header error control (HEC) generation, checking, and statistics.
- Communications processor module (CPM)
  - RISC communications processor (CP)
  - Communication-specific commands (for example, GRACEFUL STOP TRANSMIT, ENTER HUNT MODE, and RESTART TRANSMIT)
  - Supports continuous mode transmission and reception on all serial channels

Table 6. DC Electrical Specifications (continued)

Characteristic	Symbol	Min	Max	Unit
Input leakage current, V_{in} = 3.6 V (except TMS, $\overline{TRST}$, DSCK, and DSDI pins)	I_{In}	—	10	μA
Input leakage current, V_{in} = 0 V (except TMS, $\overline{TRST}$, DSCK, and DSDI pins)	I_{In}	—	10	μA
Input capacitance[2]	C_{in}	—	20	pF
Output high voltage, I_{OH} = –2.0 mA, V_{DDH} = 3.0 V (except XTAL, XFC, and open-drain pins)	V_{OH}	2.4	—	V
Output low voltage I_{OL} = 2.0 mA, CLKOUT I_{OL} = 3.2 mA [3] I_{OL} = 5.3 mA [4] I_{OL} = 7.0 mA, TXD1/PA14, TXD2/PA12 I_{OL} = 8.9 mA, $\overline{TS}$, $\overline{TA}$, $\overline{TEA}$, $\overline{BI}$, $\overline{BB}$, $\overline{HRESET}$, $\overline{SRESET}$	V_{OL}	—	0.5	V

1 V_{IL}(max) for the I²C interface is 0.8 V rather than the 1.5 V as specified in the I²C standard.

2 Input capacitance is periodically sampled.

3 A(0:31), TSIZ0/$\overline{REG}$, TSIZ1, D(0:31), DP(0:3)/$\overline{IRQ}$(3:6), RD/$\overline{WR}$, $\overline{BURST}$, $\overline{RSV}$/$\overline{IRQ2}$, IP_B(0:1)/IWP(0:1)/VFLS(0:1), IP_B2/IOIS16_B/AT2, IP_B3/IWP2/VF2, IP_B4/LWP0/VF0, IP_B5/LWP1/VF1, IP_B6/DSDI/AT0, IP_B7/PTR/AT3, RXD1/PA15, RXD2/PA13, L1TXDB/PA11, L1RXDB/PA10, L1TXDA/PA9, L1RXDA/PA8, TIN1/L1RCLKA/BRGO1/CLK1/PA7, BRGCLK1/$\overline{TOUT1}$/CLK2/PA6, TIN2/L1TCLKA/BRGO2/CLK3/PA5, $\overline{TOUT2}$/CLK4/PA4, TIN3/BRGO3/CLK5/PA3, BRGCLK2/L1RCLKB/$\overline{TOUT3}$/CLK6/PA2, TIN4/BRGO4/CLK7/PA1, L1TCLKB/$\overline{TOUT4}$/CLK8/PA0, $\overline{REJCT1}$/$\overline{SPISEL}$/PB31, SPICLK/PB30,SPIMOSI/PB29, BRGO4/SPIMISO/PB28, BRGO1/I2CSDA/PB27, BRGO2/I2CSCL/PB26, SMTXD1/PB25, SMRXD1/PB24, $\overline{SMSYN1}$/$\overline{SDACK1}$/PB23, $\overline{SMSYN2}$/$\overline{SDACK2}$/PB22, SMTXD2/L1CLKOB/PB21, SMRXD2/L1CLKOA/PB20, L1ST1/$\overline{RTS1}$/PB19, L1ST2/$\overline{RTS2}$/PB18, L1ST3/$\overline{L1RQB}$/PB17, L1ST4/$\overline{L1RQA}$/PB16, BRGO3/PB15, $\overline{RSTRT1}$/PB14, L1ST1/$\overline{RTS1}$/$\overline{DREQ0}$/PC15, L1ST2/$\overline{RTS2}$/$\overline{DREQ1}$/PC14, L1ST3/$\overline{L1RQB}$/PC13, L1ST4/$\overline{L1RQA}$/PC12, $\overline{CTS1}$/PC11, $\overline{TGATE1}$/$\overline{CD1}$/PC10, $\overline{CTS2}$/PC9, $\overline{TGATE2}$/$\overline{CD2}$/PC8, $\overline{SDACK2}$/L1TSYNCB/PC7, L1RSYNCB/PC6, $\overline{SDACK1}$/L1TSYNCA/PC5, L1RSYNCA/PC4, PD15, PD14, PD13, PD12, PD11, PD10, PD9, PD8, PD5, PD6, PD7, PD4, PD3, MII_MDC, MII_TX_ER, MII_EN, MII_MDIO, and MII_TXD[0:3]

4 $\overline{BDIP}$/$\overline{GPL\_B}$(5), $\overline{BR}$, $\overline{BG}$, FRZ/$\overline{IRQ6}$, $\overline{CS}$(0:5), $\overline{CS}$(6)/$\overline{CE}$(1)_B, $\overline{CS}$(7)/$\overline{CE}$(2)_B, $\overline{WE0}$/$\overline{BS\_B0}$/$\overline{IORD}$, $\overline{WE1}$/$\overline{BS\_B1}$/$\overline{IOWR}$, $\overline{WE2}$/$\overline{BS\_B2}$/PCOE, $\overline{WE3}$/$\overline{BS\_B3}$/PCWE, $\overline{BS\_A}$(0:3), $\overline{GPL\_A0}$/$\overline{GPL\_B0}$, $\overline{OE}$/$\overline{GPL\_A1}$/$\overline{GPL\_B1}$, $\overline{GPL\_A}$(2:3)/$\overline{GPL\_B}$(2:3)/$\overline{CS}$(2:3), UPWAITA/$\overline{GPL\_A4}$, UPWAITB/$\overline{GPL\_B4}$, $\overline{GPL\_A5}$, ALE_A, $\overline{CE1\_A}$, $\overline{CE2\_A}$, ALE_B/DSCK/AT1, OP(0:1), OP2/MODCK1/$\overline{STS}$, OP3/MODCK2/DSDO, and BADDR(28:30)

where:

Ψ_{JT} = thermal characterization parameter

T_T = thermocouple temperature on top of package

P_D = power dissipation in package

The thermal characterization parameter is measured per JEDEC JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

7.6   References

Semiconductor Equipment and Materials International   (415) 964-5111
805 East Middlefield Rd.
Mountain View, CA 94043

MIL-SPEC and EIA/JESD (JEDEC) Specifications   800-854-7179 or
(Available from Global Engineering Documents)   303-397-7956

JEDEC Specifications   http://www.jedec.org

1. C.E. Triplett and B. Joiner, "An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module," Proceedings of SemiTherm, San Diego, 1998, pp. 47−54.

2. B. Joiner and V. Adams, "Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling," Proceedings of SemiTherm, San Diego, 1999, pp. 212−220.

8   Layout Practices

Each V_{DD} pin on the MPC860 should be provided with a low-impedance path to the board's supply. Each GND pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on the chip. The V_{DD} power supply should be bypassed to ground using at least four 0.1 µF-bypass capacitors located as close as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to chip V_{DD} and GND should be kept to less than half an inch per capacitor lead. A four-layer board employing two inner layers as V_{CC} and GND planes is recommended.

All output pins on the MPC860 have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized in order to minimize undershoot and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data buses. Maximum PC trace lengths of 6 inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the V_{CC} and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.

Table 7. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B9	CLKOUT to A(0:31), BADDR(28:30), RD/$\overline{\text{WR}}$, $\overline{\text{BURST}}$, D(0:31), DP(0:3), TSIZ(0:1), $\overline{\text{REG}}$, $\overline{\text{RSV}}$, AT(0:3), PTR High-Z	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.04	ns
B11	CLKOUT to $\overline{\text{TS}}$, $\overline{\text{BB}}$ assertion	7.58	13.58	6.25	12.25	5.00	11.00	3.80	11.29	ns
B11a	CLKOUT to $\overline{\text{TA}}$, $\overline{\text{BI}}$ assertion (when driven by the memory controller or PCMCIA interface)	2.50	9.25	2.50	9.25	2.50	9.25	2.50	9.75	ns
B12	CLKOUT to $\overline{\text{TS}}$, $\overline{\text{BB}}$ negation	7.58	14.33	6.25	13.00	5.00	11.75	3.80	8.54	ns
B12a	CLKOUT to $\overline{\text{TA}}$, $\overline{\text{BI}}$ negation (when driven by the memory controller or PCMCIA interface)	2.50	11.00	2.50	11.00	2.50	11.00	2.50	9.00	ns
B13	CLKOUT to $\overline{\text{TS}}$, $\overline{\text{BB}}$ High-Z	7.58	21.58	6.25	20.25	5.00	19.00	3.80	14.04	ns
B13a	CLKOUT to $\overline{\text{TA}}$, $\overline{\text{BI}}$ High-Z (when driven by the memory controller or PCMCIA interface)	2.50	15.00	2.50	15.00	2.50	15.00	2.50	15.00	ns
B14	CLKOUT to $\overline{\text{TEA}}$ assertion	2.50	10.00	2.50	10.00	2.50	10.00	2.50	9.00	ns
B15	CLKOUT to $\overline{\text{TEA}}$ High-Z	2.50	15.00	2.50	15.00	2.50	15.00	2.50	15.00	ns
B16	$\overline{\text{TA}}$, $\overline{\text{BI}}$ valid to CLKOUT (setup time)	9.75	—	9.75	—	9.75	—	6.00	—	ns
B16a	$\overline{\text{TEA}}$, $\overline{\text{KR}}$, $\overline{\text{RETRY}}$, $\overline{\text{CR}}$ valid to CLKOUT (setup time)	10.00	—	10.00	—	10.00	—	4.50	—	ns
B16b	$\overline{\text{BB}}$, $\overline{\text{BG}}$, $\overline{\text{BR}}$, valid to CLKOUT (setup time)[5]	8.50	—	8.50	—	8.50	—	4.00	—	ns
B17	CLKOUT to $\overline{\text{TA}}$, $\overline{\text{TEA}}$, $\overline{\text{BI}}$, $\overline{\text{BB}}$, $\overline{\text{BG}}$, $\overline{\text{BR}}$ valid (hold time)	1.00	—	1.00	—	1.00	—	2.00	—	ns
B17a	CLKOUT to $\overline{\text{KR}}$, $\overline{\text{RETRY}}$, $\overline{\text{CR}}$ valid (hold time)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B18	D(0:31), DP(0:3) valid to CLKOUT rising edge (setup time)[6]	6.00	—	6.00	—	6.00	—	6.00	—	ns
B19	CLKOUT rising edge to D(0:31), DP(0:3) valid (hold time)[6]	1.00	—	1.00	—	1.00	—	2.00	—	ns
B20	D(0:31), DP(0:3) valid to CLKOUT falling edge (setup time)[7]	4.00	—	4.00	—	4.00	—	4.00	—	ns
B21	CLKOUT falling edge to D(0:31), DP(0:3) valid (hold time)[7]	2.00	—	2.00	—	2.00	—	2.00	—	ns
B22	CLKOUT rising edge to $\overline{\text{CS}}$ asserted GPCM ACS = 00	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.04	ns
B22a	CLKOUT falling edge to $\overline{\text{CS}}$ asserted GPCM ACS = 10, TRLX = 0	—	8.00	—	8.00	—	8.00	—	8.00	ns
B22b	CLKOUT falling edge to $\overline{\text{CS}}$ asserted GPCM ACS = 11, TRLX = 0, EBDF = 0	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.54	ns
B22c	CLKOUT falling edge to $\overline{\text{CS}}$ asserted GPCM ACS = 11, TRLX = 0, EBDF = 1	10.86	17.99	8.88	16.00	7.00	14.13	5.18	12.31	ns

MPC860 PowerQUICC Family Hardware Specifications, Rev. 10

Table 7. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B23	CLKOUT rising edge to $\overline{CS}$ negated GPCM read access, GPCM write access ACS = 00, TRLX = 0, and CSNT = 0	2.00	8.00	2.00	8.00	2.00	8.00	2.00	8.00	ns
B24	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 0	5.58	—	4.25	—	3.00	—	1.79	—	ns
B24a	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 0	13.15	—	10.50	—	8.00	—	5.58	—	ns
B25	CLKOUT rising edge to $\overline{OE}$, $\overline{WE}$(0:3) asserted	—	9.00	—	9.00	—	9.00	—	9.00	ns
B26	CLKOUT rising edge to $\overline{OE}$ negated	2.00	9.00	2.00	9.00	2.00	9.00	2.00	9.00	ns
B27	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 1	35.88	—	29.25	—	23.00	—	16.94	—	ns
B27a	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 1	43.45	—	35.50	—	28.00	—	20.73	—	ns
B28	CLKOUT rising edge to $\overline{WE}$(0:3) negated GPCM write access CSNT = 0	—	9.00	—	9.00	—	9.00	—	9.00	ns
B28a	CLKOUT falling edge to $\overline{WE}$(0:3) negated GPCM write access TRLX = 0, 1, CSNT = 1, EBDF = 0	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.54	ns
B28b	CLKOUT falling edge to $\overline{CS}$ negated GPCM write access TRLX = 0, 1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 0	—	14.33	—	13.00	—	11.75	—	10.54	ns
B28c	CLKOUT falling edge to $\overline{WE}$(0:3) negated GPCM write access TRLX = 0, 1, CSNT = 1 write access TRLX = 0, CSNT = 1, EBDF = 1	10.86	17.99	8.88	16.00	7.00	14.13	5.18	12.31	ns
B28d	CLKOUT falling edge to $\overline{CS}$ negated GPCM write access TRLX = 0, 1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 1	—	17.99	—	16.00	—	14.13	—	12.31	ns
B29	$\overline{WE}$(0:3) negated to D(0:31), DP(0:3) High-Z GPCM write access CSNT = 0, EBDF = 0	5.58	—	4.25	—	3.00	—	1.79	—	ns
B29a	$\overline{WE}$(0:3) negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 0	13.15	—	10.5	—	8.00	—	5.58	—	ns
B29b	$\overline{CS}$ negated to D(0:31), DP(0:3), High-Z GPCM write access, ACS = 00, TRLX = 0, 1, and CSNT = 0	5.58	—	4.25	—	3.00	—	1.79	—	ns
B29c	$\overline{CS}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 0	13.15	—	10.5	—	8.00	—	5.58	—	ns

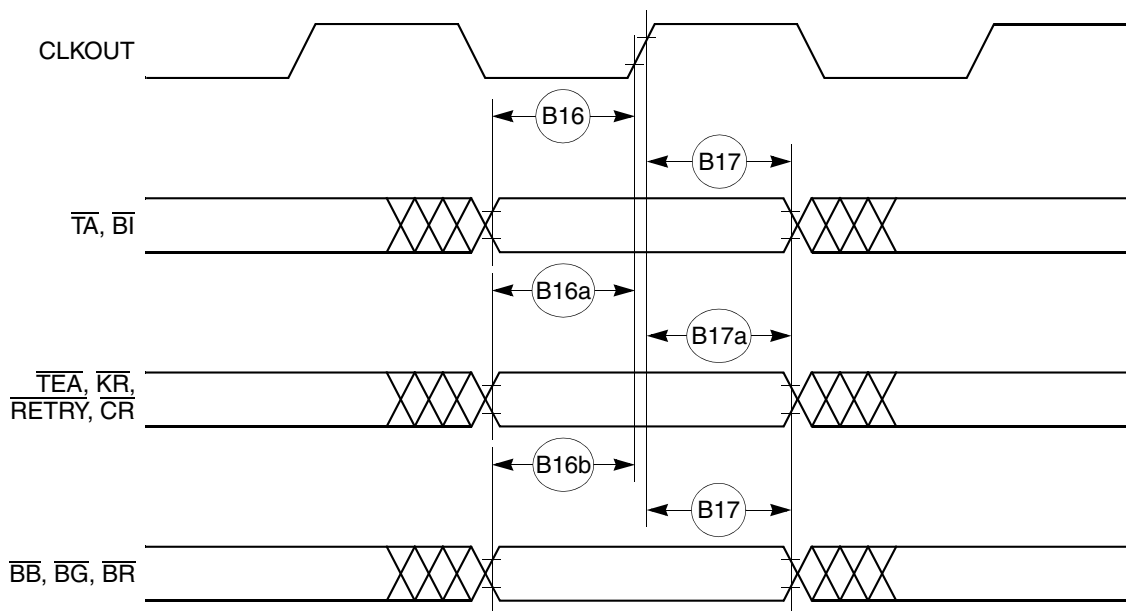Figure 7 provides the timing for the synchronous input signals.

Figure 7. Synchronous Input Signals Timing

Figure 8 provides normal case timing for input data. It also applies to normal read accesses under the control of the UPM in the memory controller.
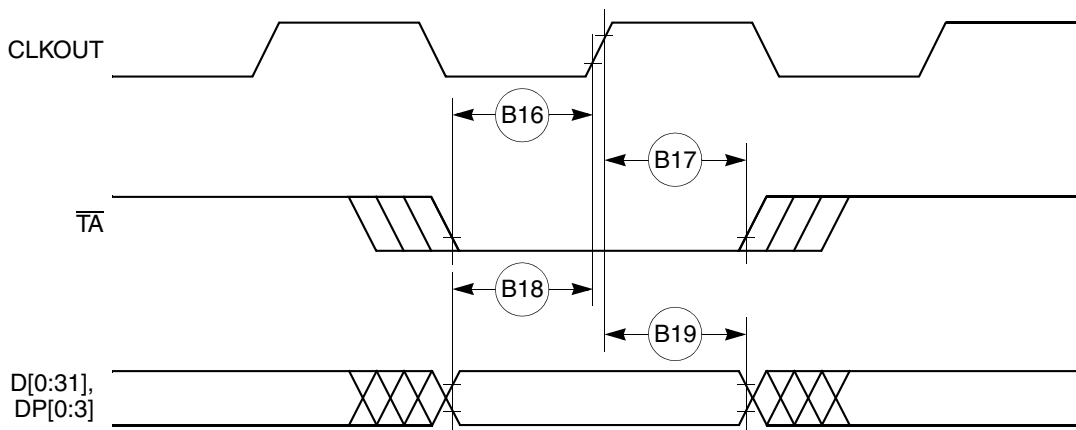

Figure 8. Input Data Timing in Normal Case

MPC860 PowerQUICC Family Hardware Specifications, Rev. 10

Figure 17 provides the timing for the external bus controlled by the UPM.
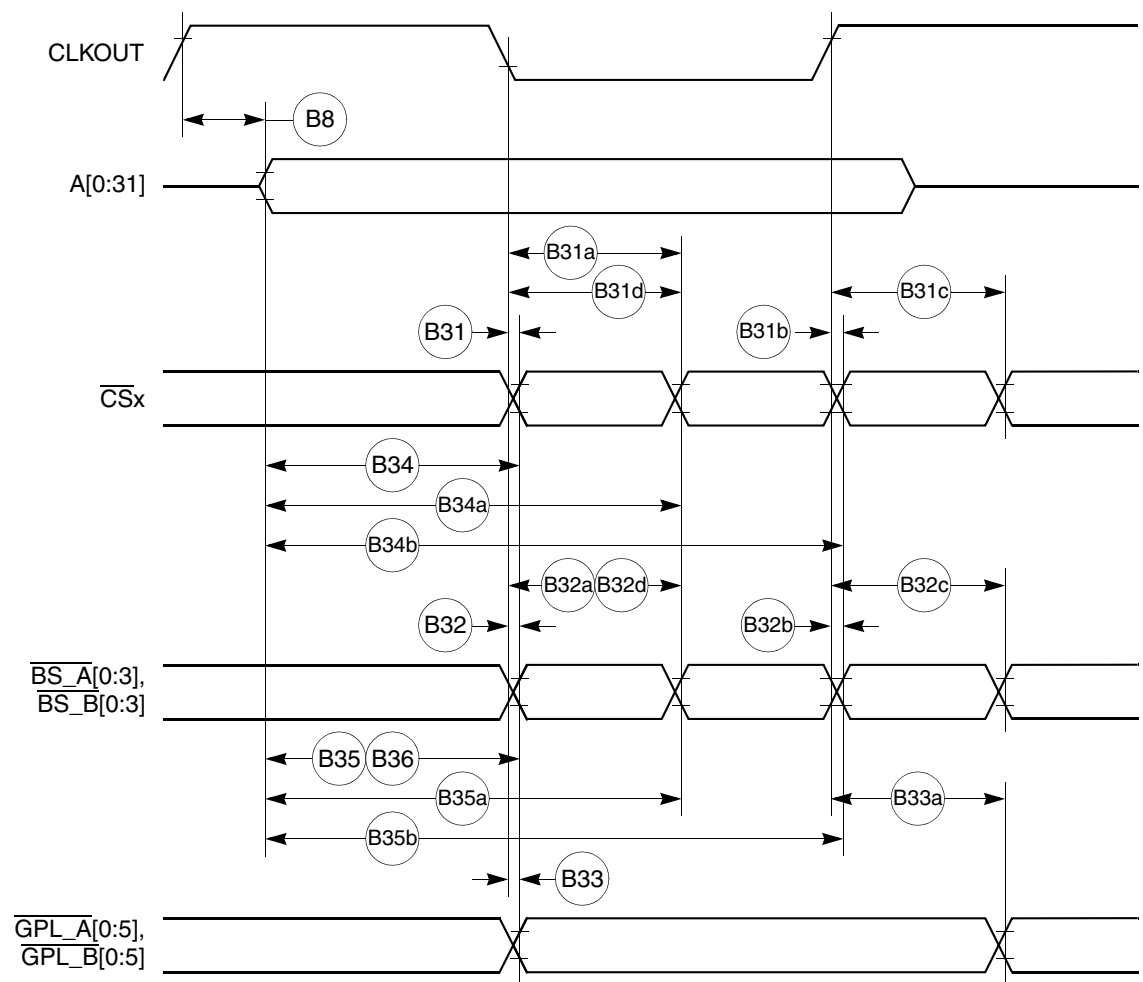
Figure 17. External Bus Timing (UPM Controlled Signals)

Figure 20 provides the timing for the synchronous external master access controlled by the GPCM.
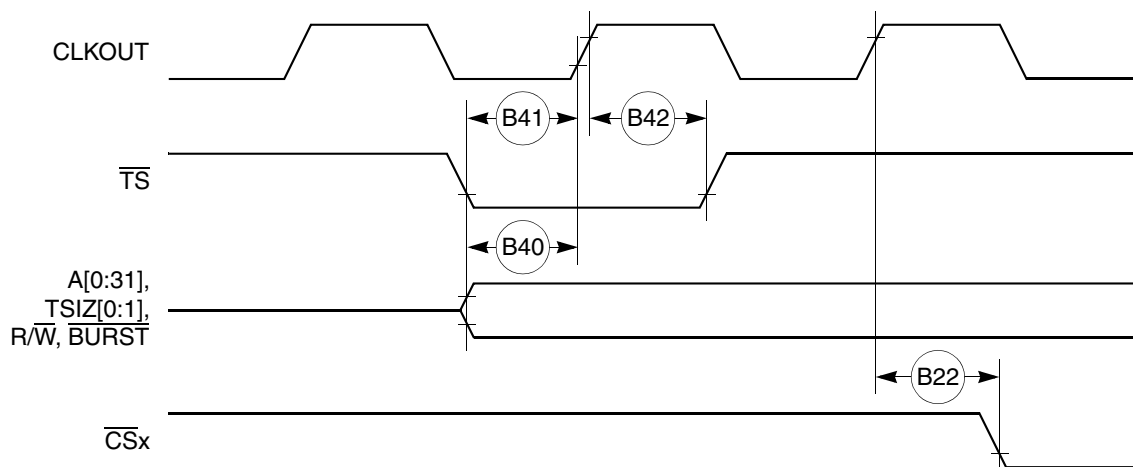
Figure 20. Synchronous External Master Access Timing (GPCM Handled ACS = 00)

Figure 21 provides the timing for the asynchronous external master memory access controlled by the GPCM.
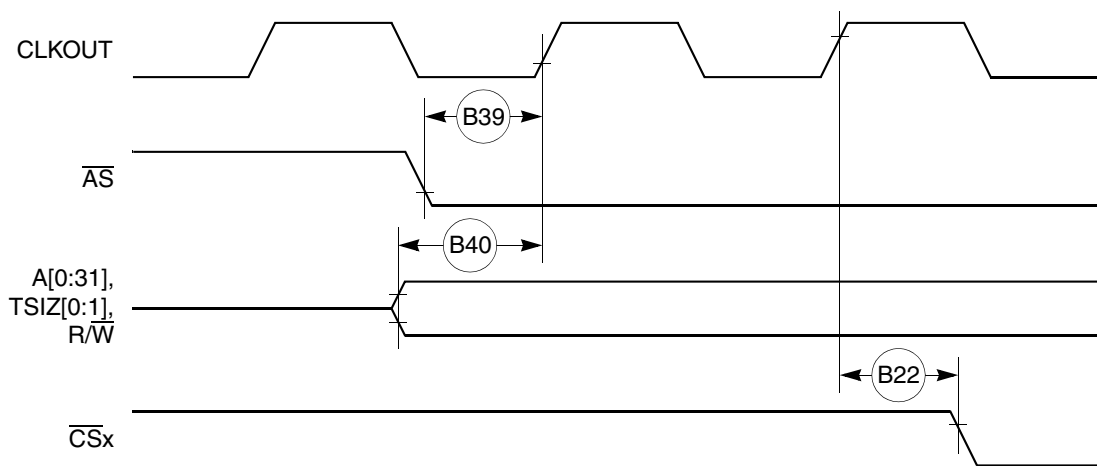
Figure 21. Asynchronous External Master Memory Access Timing (GPCM Controlled—ACS = 00)

Figure 22 provides the timing for the asynchronous external master control signals negation.
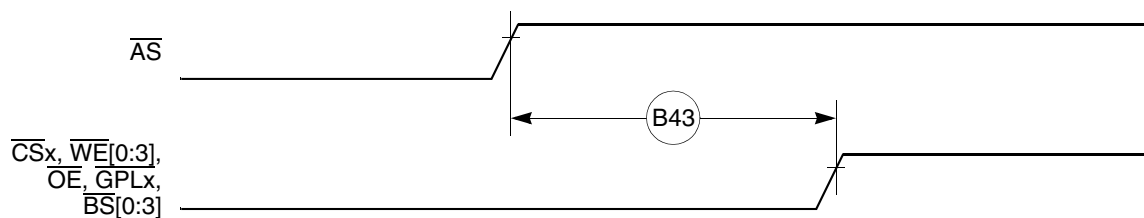
Figure 22. Asynchronous External Master—Control Signals Negation Timing

Figure 25 provides the PCMCIA access cycle timing for the external bus read.
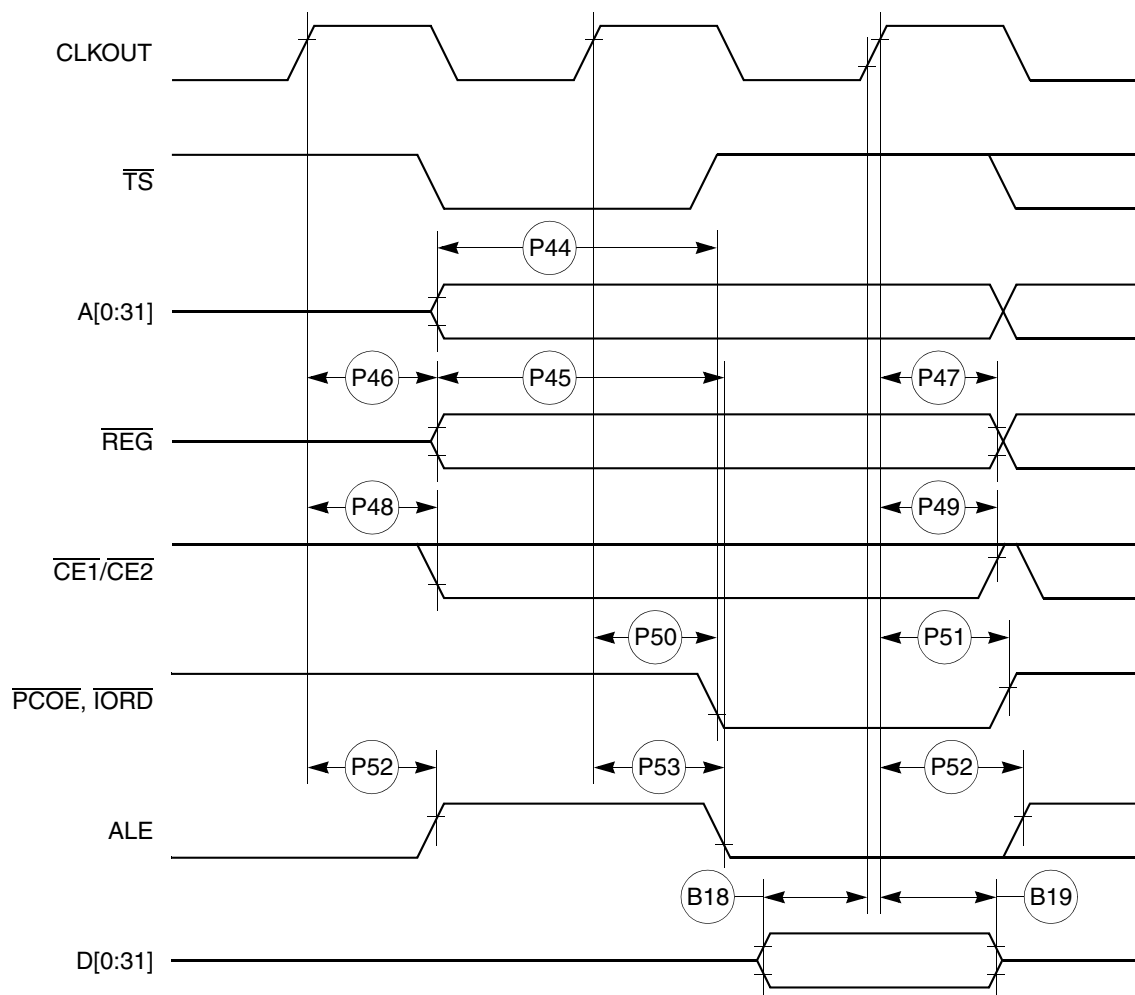
Figure 25. PCMCIA Access Cycle Timing External Bus Read

Figure 26 provides the PCMCIA access cycle timing for the external bus write.
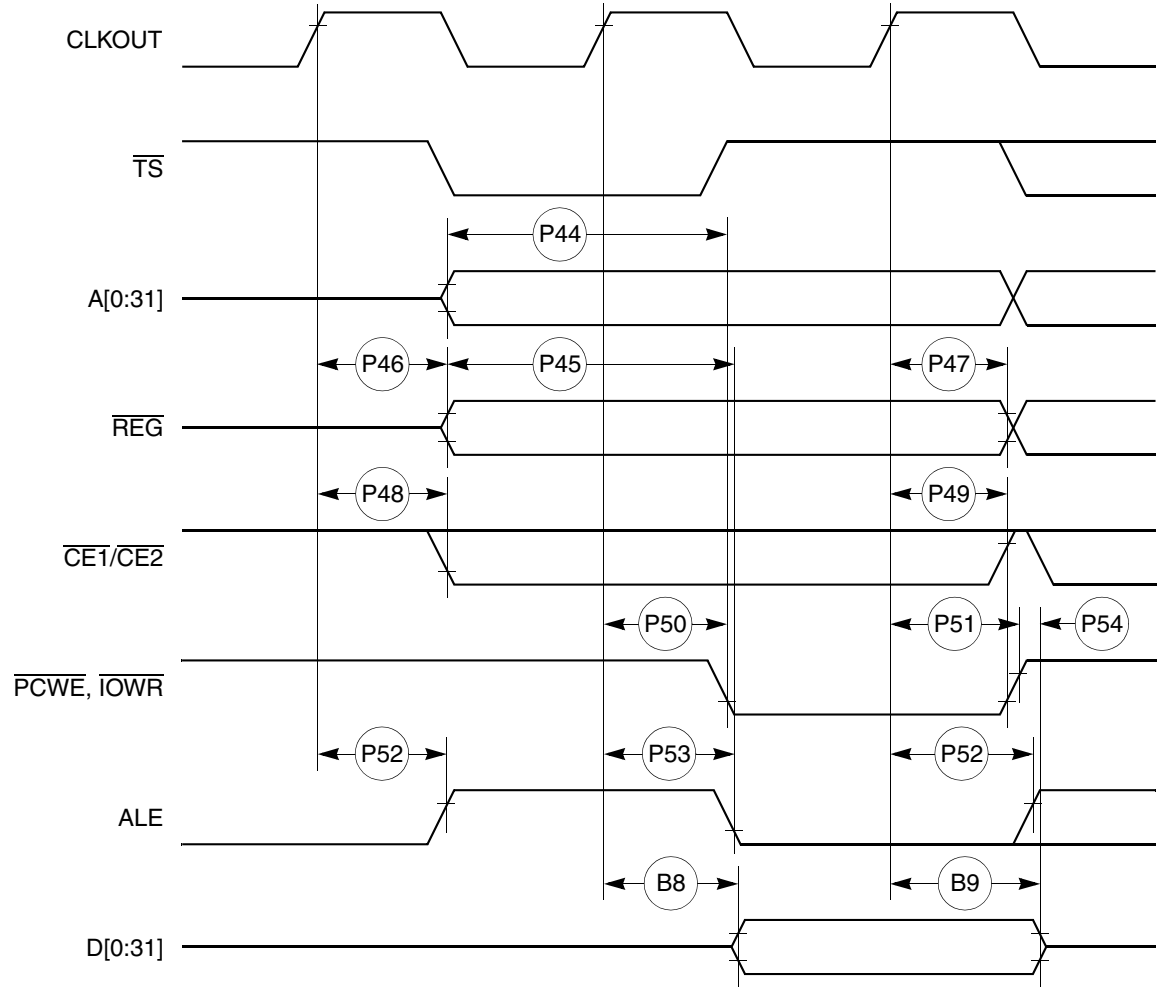
Figure 26. PCMCIA Access Cycle Timing External Bus Write

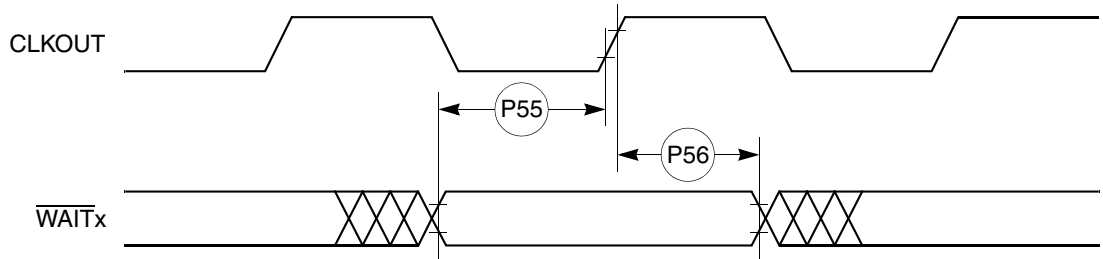Figure 27 provides the PCMCIA $\overline{\text{WAIT}}$ signal detection timing.

Figure 27. PCMCIA $\overline{\text{WAIT}}$ Signal Detection Timing

Table 11 shows the debug port timing for the MPC860.

Table 11. Debug Port Timing

Num	Characteristic	All Frequencies		Unit
		Min	**Max**	
P61	DSCK cycle time	$3 \times T_{CLOCKOUT}$	—	—
P62	DSCK clock pulse width	$1.25 \times T_{CLOCKOUT}$	—	—
P63	DSCK rise and fall times	0.00	3.00	ns
P64	DSDI input data setup time	8.00	—	ns
P65	DSDI data hold time	5.00	—	ns
P66	DSCK low to DSDO data valid	0.00	15.00	ns
P67	DSCK low to DSDO invalid	0.00	2.00	ns

Figure 30 provides the input timing for the debug port clock.
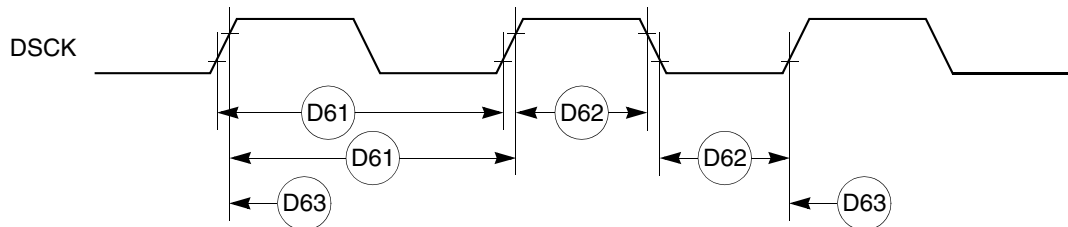
Figure 30. Debug Port Clock Input Timing

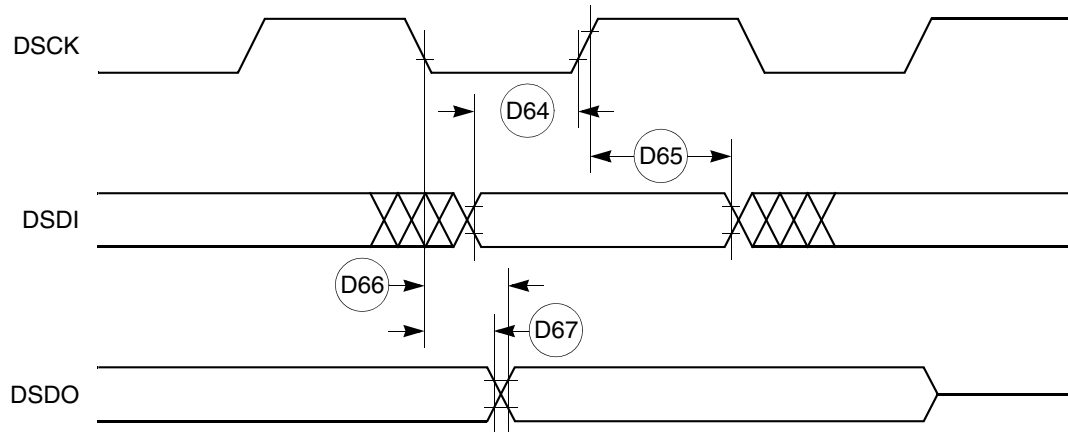Figure 31 provides the timing for the debug port.

Figure 31. Debug Port Timings

Figure 32 shows the reset timing for the data bus configuration.
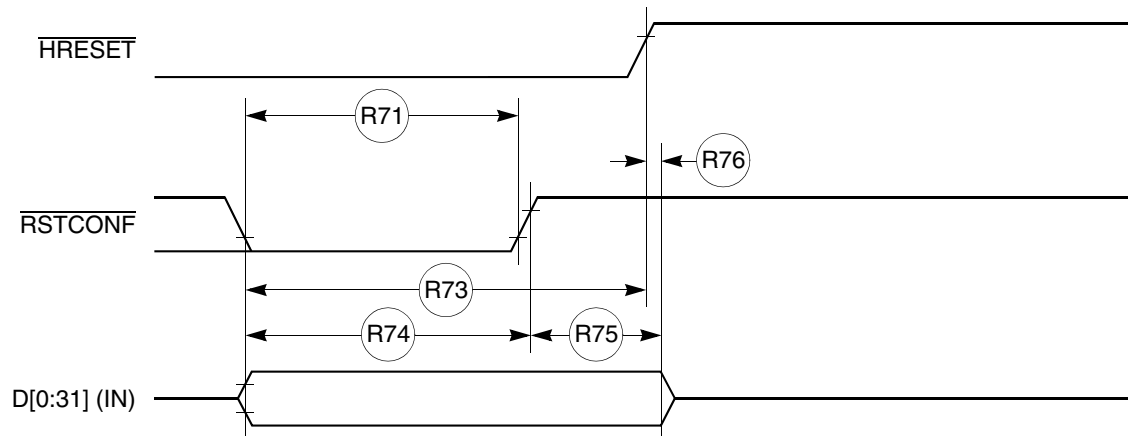

Figure 32. Reset Timing—Configuration from Data Bus

Figure 33 provides the reset timing for the data bus weak drive during configuration.
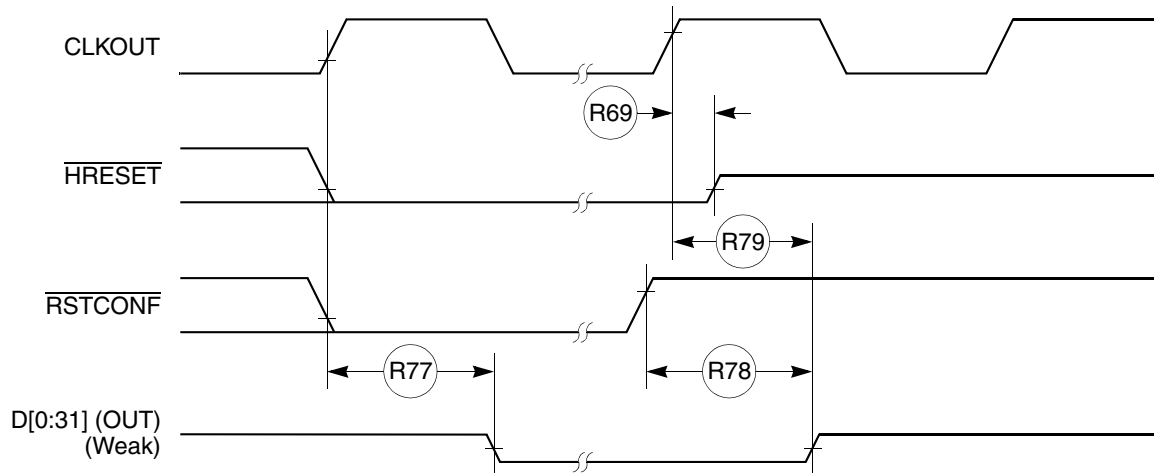

Figure 33. Reset Timing—Data Bus Weak Drive During Configuration

11 CPM Electrical Characteristics

This section provides the AC and DC electrical specifications for the communications processor module (CPM) of the MPC860.

11.1 PIP/PIO AC Electrical Specifications

Table 14 provides the PIP/PIO AC timings as shown in Figure 39 through Figure 43.

Table 14. PIP/PIO Timing

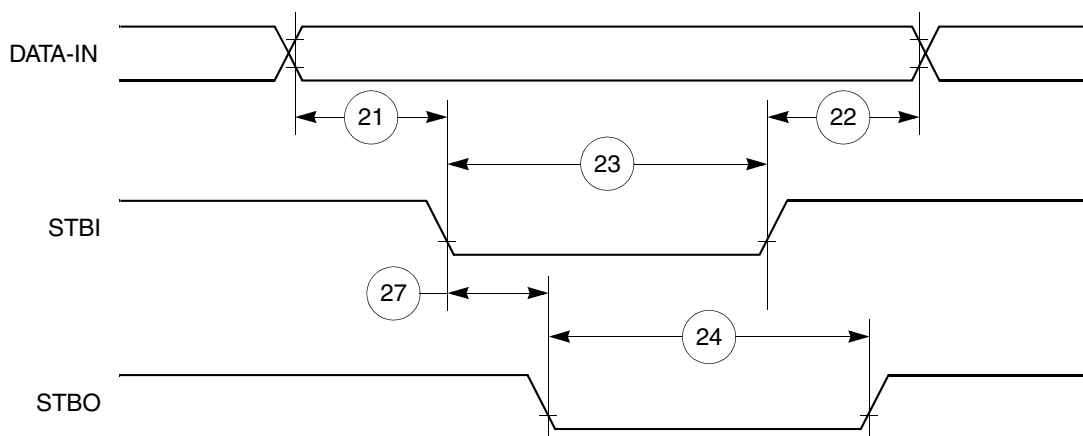| Num	Characteristic	All Frequencies		Unit
		Min	Max	
21	Data-in setup time to STBI low	0	—	ns
22	Data-in hold time to STBI high	2.5 – t3[1]	—	CLK
23	STBI pulse width	1.5	—	CLK
24	STBO pulse width	1 CLK – 5 ns	—	ns
25	Data-out setup time to STBO low	2	—	CLK
26	Data-out hold time from STBO high	5	—	CLK
27	STBI low to STBO low (Rx interlock)	—	2	CLK
28	STBI low to STBO high (Tx interlock)	2	—	CLK
29	Data-in setup time to clock high	15	—	ns
30	Data-in hold time from clock high	7.5	—	ns
31	Clock low to data-out valid (CPU writes data, control, or direction)	—	25	ns

[1] t3 = Specification 23.

Figure 39. PIP Rx (Interlock Mode) Timing Diagram

11.4 Baud Rate Generator AC Electrical Specifications

Table 17 provides the baud rate generator timings as shown in Figure 49.

Table 17. Baud Rate Generator Timing

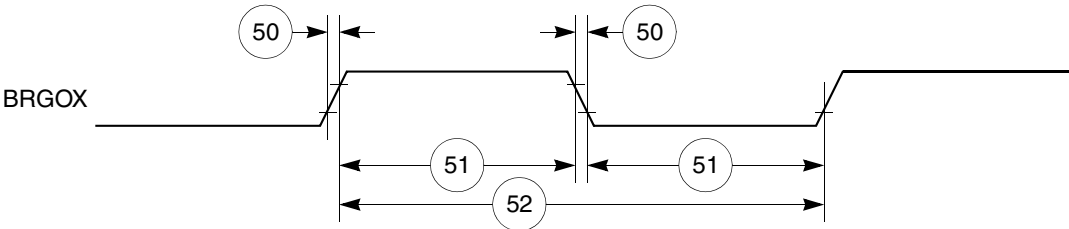| Num	Characteristic	All Frequencies		Unit
		Min	**Max**	
50	BRGO rise and fall time	—	10	ns
51	BRGO duty cycle	40	60	%
52	BRGO cycle	40	—	ns

Figure 49. Baud Rate Generator Timing Diagram

11.5 Timer AC Electrical Specifications

Table 18 provides the general-purpose timer timings as shown in Figure 50.

Table 18. Timer Timing

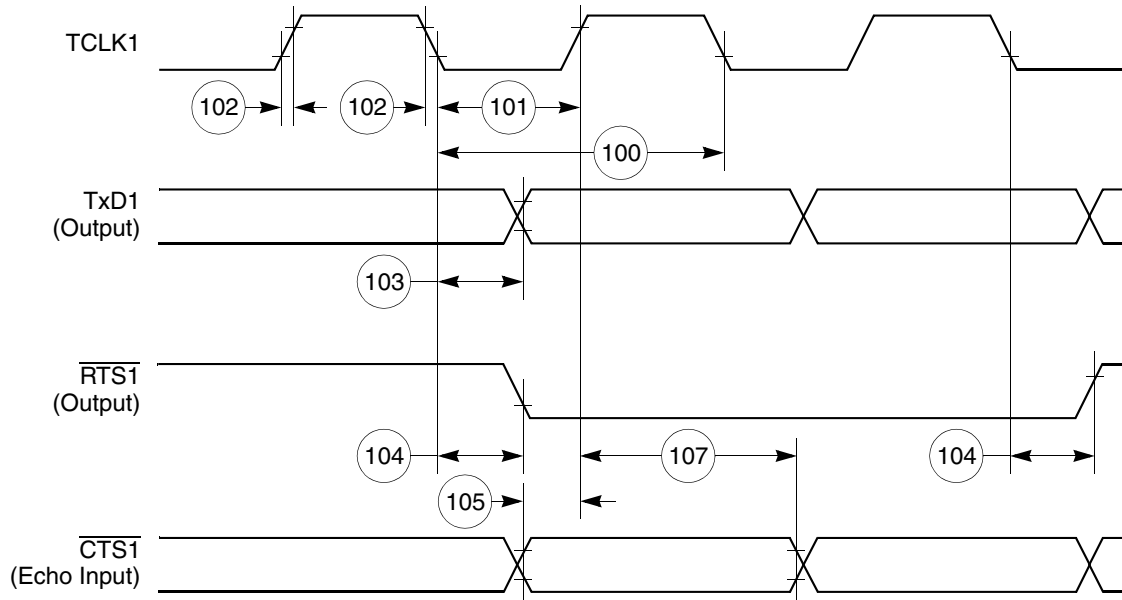| Num	Characteristic	All Frequencies		Unit
		Min	**Max**	
61	TIN/$\overline{\text{TGATE}}$ rise and fall time	10	—	ns
62	TIN/$\overline{\text{TGATE}}$ low time	1	—	CLK
63	TIN/$\overline{\text{TGATE}}$ high time	2	—	CLK
64	TIN/$\overline{\text{TGATE}}$ cycle time	3	—	CLK
65	CLKO low to $\overline{\text{TOUT}}$ valid	3	25	ns

Figure 58. HDLC Bus Timing Diagram

11.8 Ethernet Electrical Specifications

Table 22 provides the Ethernet timings as shown in Figure 59 through Figure 63.

Table 22. Ethernet Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
120	CLSN width high	40	—	ns
121	RCLK1 rise/fall time	—	15	ns
122	RCLK1 width low	40	—	ns
123	RCLK1 clock period[1]	80	120	ns
124	RXD1 setup time	20	—	ns
125	RXD1 hold time	5	—	ns
126	RENA active delay (from RCLK1 rising edge of the last data bit)	10	—	ns
127	RENA width low	100	—	ns
128	TCLK1 rise/fall time	—	15	ns
129	TCLK1 width low	40	—	ns
130	TCLK1 clock period[1]	99	101	ns
131	TXD1 active delay (from TCLK1 rising edge)	10	50	ns
132	TXD1 inactive delay (from TCLK1 rising edge)	10	50	ns
133	TENA active delay (from TCLK1 rising edge)	10	50	ns
134	TENA inactive delay (from TCLK1 rising edge)	10	50	ns
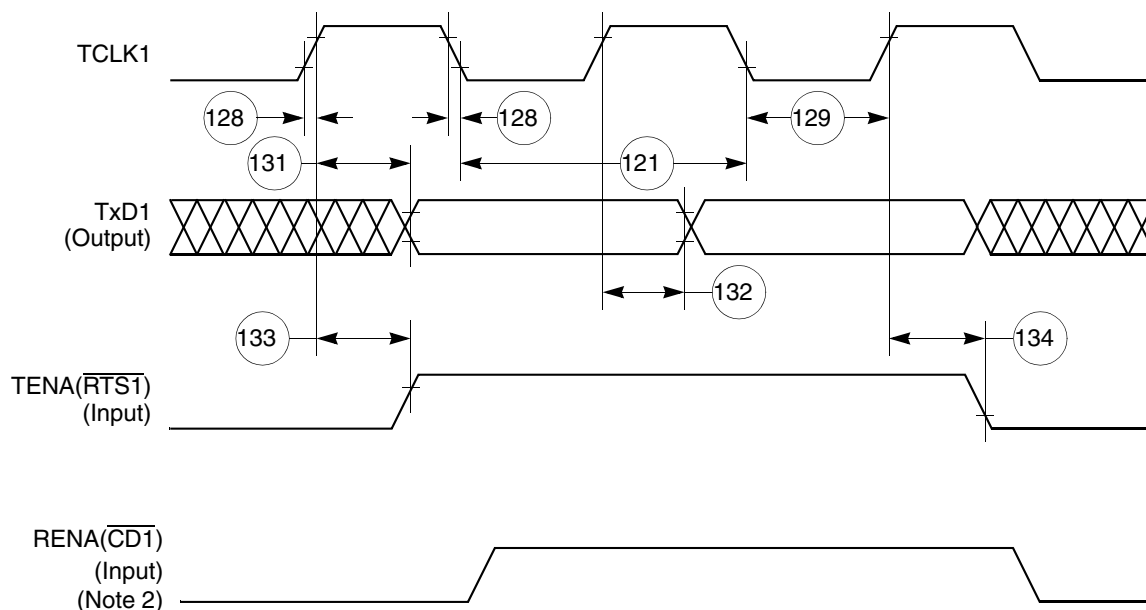
Notes:
1. Transmit clock invert (TCI) bit in GSMR is set.
2. If RENA is deasserted before TENA, or RENA is not asserted at all during transmit, then the CSL bit is set in the buffer descriptor at the end of the frame transmission.

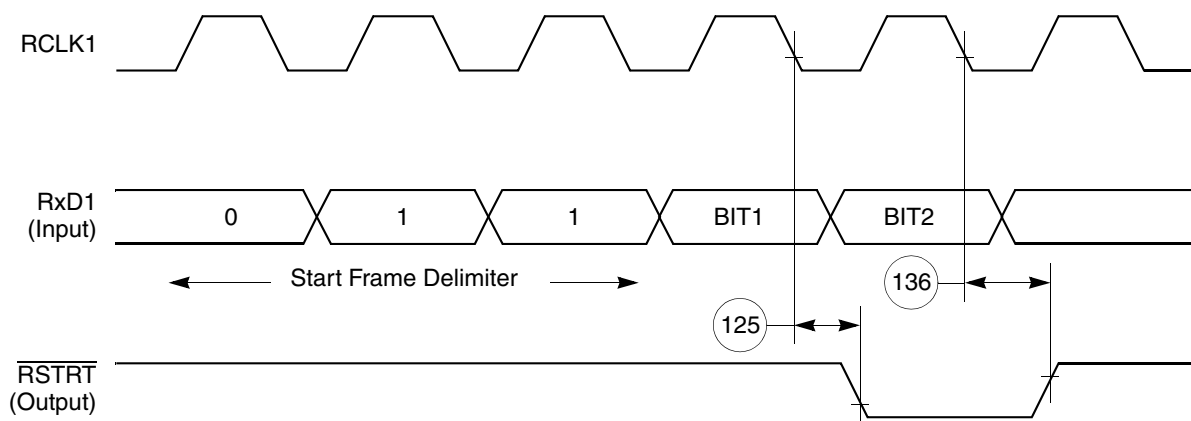**Figure 61. Ethernet Transmit Timing Diagram**

Figure 62. CAM Interface Receive Start Timing Diagram

Figure 63. CAM Interface REJECT Timing Diagram

Figure 70 shows signal timings during UTOPIA receive operations.
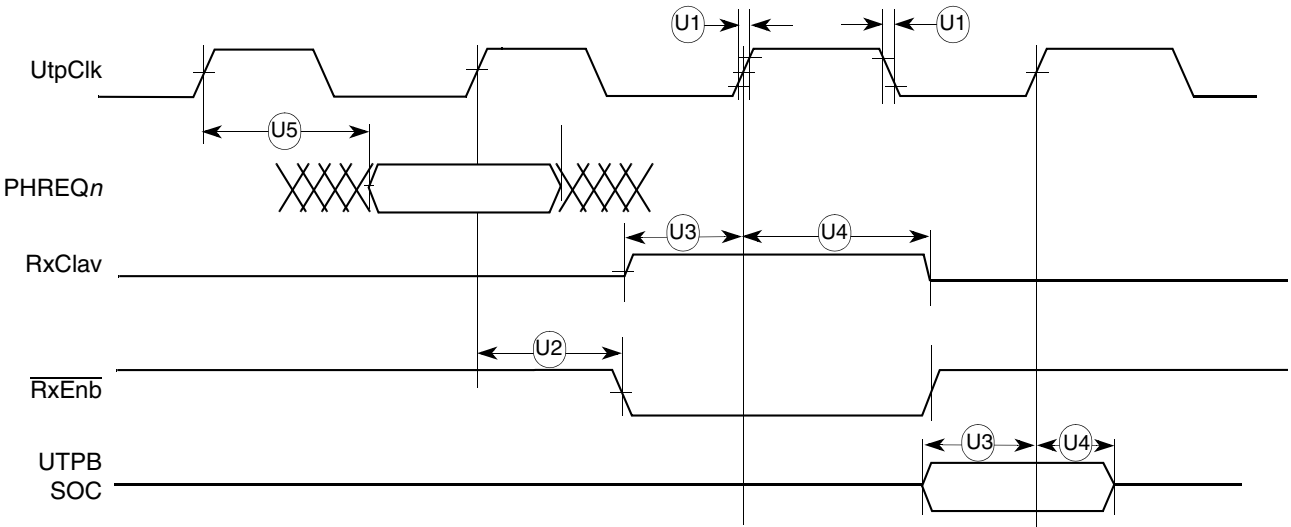

Figure 70. UTOPIA Receive Timing

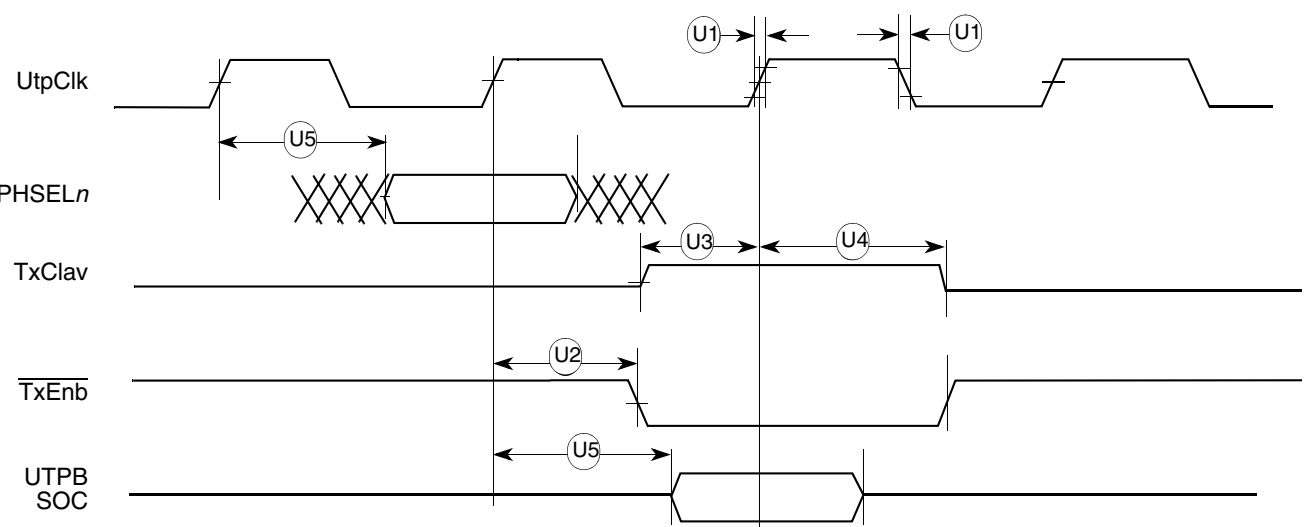Figure 71 shows signal timings during UTOPIA transmit operations.

Figure 71. UTOPIA Transmit Timing

Figure 78 shows the mechanical dimensions of the ZQ PBGA package.

NOTE

1. All Dimensions in millimeters.
2. Dimensions and tolerance per ASME Y14.5M, 1994.
3. Maximum Solder Ball Diameter measured parallel to Datum A.
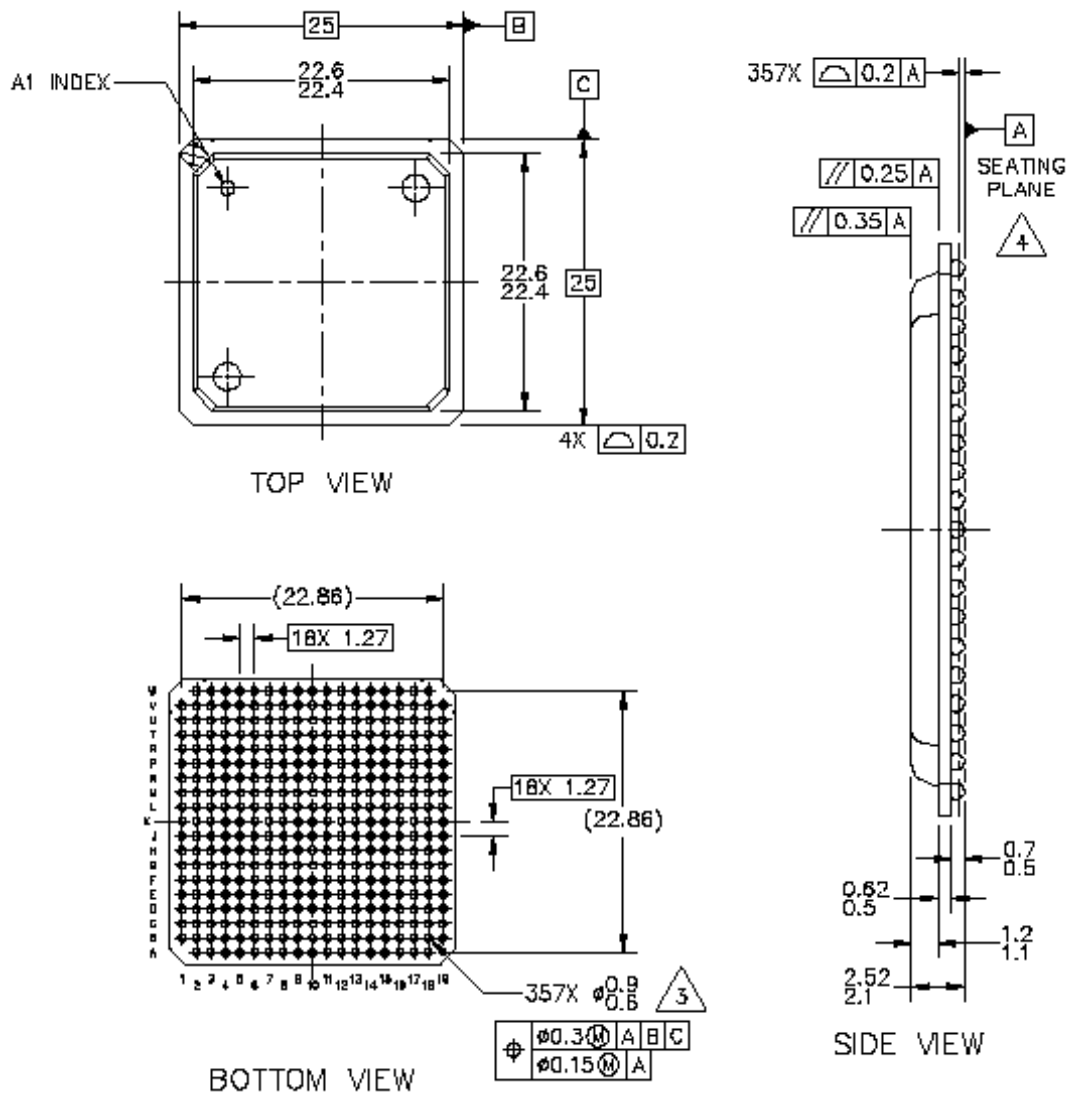4. Datum A, the seating plane, is defined by the spherical crowns of the solder balls.

Figure 78. Mechanical Dimensions and Bottom Surface Nomenclature of the ZQ PBGA Package