#### NXP USA Inc. - KMPC860PVR50D4 Datasheet



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#### Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

#### Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

#### Details

Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	50MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (4), 10/100Mbps (1)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 95°C (TA)
Security Features	-
Package / Case	357-BBGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc860pvr50d4

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Features

- Allows dynamic changes
- Can be internally connected to six serial channels (four SCCs and two SMCs)
- Parallel interface port (PIP)
  - Centronics interface support
  - Supports fast connection between compatible ports on the MPC860 or the MC68360
- PCMCIA interface
  - Master (socket) interface, release 2.1 compliant
  - Supports two independent PCMCIA sockets
  - Supports eight memory or I/O windows
- Low power support
  - Full on-all units fully powered
  - Doze—core functional units disabled except time base decrementer, PLL, memory controller, RTC, and CPM in low-power standby
  - Sleep-all units disabled except RTC and PIT, PLL active for fast wake up
  - Deep sleep—all units disabled including PLL except RTC and PIT
  - Power down mode—all units powered down except PLL, RTC, PIT, time base, and decrementer
- Debug interface
  - Eight comparators: four operate on instruction address, two operate on data address, and two
    operate on data
  - Supports conditions: =  $\neq < >$
  - Each watchpoint can generate a break-point internally.
- 3.3-V operation with 5-V TTL compatibility except EXTAL and EXTCLK
- 357-pin ball grid array (BGA) package



#### Thermal Characteristics

Figure 1 shows the undershoot and overshoot voltages at the interface of the MPC860.



1. t<sub>interface</sub> refers to the clock period associated with the bus clock interface.

Figure 1. Undershoot/Overshoot Voltage for V<sub>DDH</sub> and V<sub>DDL</sub>

# 4 Thermal Characteristics

#### Table 3. Package Description

Package Designator	Package Code (Case No.)	Package Description
ZP	5050 (1103-01)	PBGA 357 25*25*0.9P1.27
ZQ/VR	5058 (1103D-02)	PBGA 357 25*25*1.2P1.27



	Chavastavistis	33 MHz		40 MHz		50 MHz		66 MHz		
Num	Characteristic	Min	Мах	Min	Max	Min	Мах	Min	Max	Unit
B23	CLKOUT rising edge to $\overline{CS}$ negated GPCM read access, GPCM write access ACS = 00, TRLX = 0, and CSNT = 0	2.00	8.00	2.00	8.00	2.00	8.00	2.00	8.00	ns
B24	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 0	5.58	—	4.25	_	3.00	_	1.79	—	ns
B24a	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 0	13.15	—	10.50	—	8.00	—	5.58	—	ns
B25	CLKOUT rising edge to $\overline{OE}$ , $\overline{WE}$ (0:3) asserted	—	9.00	—	9.00	—	9.00	—	9.00	ns
B26	CLKOUT rising edge to OE negated	2.00	9.00	2.00	9.00	2.00	9.00	2.00	9.00	ns
B27	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 1	35.88	_	29.25	_	23.00	_	16.94	_	ns
B27a	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 1	43.45	—	35.50	—	28.00	—	20.73	—	ns
B28	CLKOUT rising edge to $\overline{WE}(0:3)$ negated GPCM write access CSNT = 0	—	9.00	—	9.00	—	9.00	—	9.00	ns
B28a	CLKOUT falling edge to $\overline{WE}(0:3)$ negated GPCM write access TRLX = 0, 1, CSNT = 1, EBDF = 0	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.54	ns
B28b	CLKOUT falling edge to $\overline{CS}$ negated GPCM write access TRLX = 0, 1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 0	—	14.33	—	13.00		11.75		10.54	ns
B28c	CLKOUT falling edge to $\overline{WE}$ (0:3) negated GPCM write access TRLX = 0, 1, CSNT = 1 write access TRLX = 0, CSNT = 1, EBDF = 1	10.86	17.99	8.88	16.00	7.00	14.13	5.18	12.31	ns
B28d	CLKOUT falling edge to $\overline{CS}$ negated GPCM write access TRLX = 0, 1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 1	_	17.99	_	16.00		14.13		12.31	ns
B29	$\overline{WE}(0:3)$ negated to D(0:31), DP(0:3) High-Z GPCM write access CSNT = 0, EBDF = 0	5.58	_	4.25	—	3.00	—	1.79	—	ns
B29a	$\overline{WE}(0:3)$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 0	13.15	—	10.5	—	8.00		5.58	—	ns
B29b	$\overline{\text{CS}}$ negated to D(0:31), DP(0:3), High-Z GPCM write access, ACS = 00, TRLX = 0, 1, and CSNT = 0	5.58		4.25		3.00		1.79		ns
B29c	$\overline{\text{CS}}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 0	13.15		10.5		8.00		5.58		ns

#### Table 7. Bus Operation Timings (continued)



Figure 3 is the control timing diagram.



Figure 4 provides the timing for the external clock.



Figure 4. External Clock Timing



**Bus Signal Timing** 

Figure 5 provides the timing for the synchronous output signals.



Figure 5. Synchronous Output Signals Timing

Figure 6 provides the timing for the synchronous active pull-up and open-drain output signals.



Figure 6. Synchronous Active Pull-Up Resistor and Open-Drain Outputs Signals Timing



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Table 8 provides interrupt timing for the MPC860.

#### Table 8. Interrupt Timing

Num	Characteristic1	All Freq	Unit	
	Characteristic	Min	Мах	Unit
139	IRQx valid to CLKOUT rising edge (setup time)	6.00	_	ns
140	IRQx hold time after CLKOUT	2.00	_	ns
141	IRQx pulse width low	3.00	—	ns
142	IRQx pulse width high	3.00	_	ns
143	IRQx edge-to-edge time	$4 \times T_{CLOCKOUT}$	—	—

The timings I39 and I40 describe the testing conditions under which the IRQ lines are tested when being defined as level-sensitive. The IRQ lines are synchronized internally and do not have to be asserted or negated with reference to the CLKOUT.

The timings I41, I42, and I43 are specified to allow the correct function of the IRQ lines detection circuitry and have no direct relation with the total system interrupt latency that the MPC860 is able to support.

Figure 23 provides the interrupt detection timing for the external level-sensitive lines.



Figure 23. Interrupt Detection Timing for External Level Sensitive Lines

Figure 24 provides the interrupt detection timing for the external edge-sensitive lines.



Figure 24. Interrupt Detection Timing for External Edge Sensitive Lines





Figure 34 provides the reset timing for the debug port configuration.

Figure 34. Reset Timing—Debug Port Configuration

# **10 IEEE 1149.1 Electrical Specifications**

Table 13 provides the JTAG timings for the MPC860 shown in Figure 35 through Figure 38.

Num	Charactariatia	All Freq	Unit	
Nulli	Characteristic	Min	Мах	Onit
J82	TCK cycle time	100.00	—	ns
J83	TCK clock pulse width measured at 1.5 V	40.00	—	ns
J84	TCK rise and fall times	0.00	10.00	ns
J85	TMS, TDI data setup time	5.00	—	ns
J86	TMS, TDI data hold time	25.00	—	ns
J87	TCK low to TDO data valid	—	27.00	ns
J88	TCK low to TDO data invalid	0.00	—	ns
J89	TCK low to TDO high impedance	—	20.00	ns
J90	TRST assert time	100.00	_	ns
J91	TRST setup time to TCK low	40.00	—	ns
J92	TCK falling edge to output valid	—	50.00	ns
J93	TCK falling edge to output valid out of high impedance	—	50.00	ns
J94	TCK falling edge to output high impedance	—	50.00	ns
J95	Boundary scan input valid to TCK rising edge	50.00	—	ns
J96	TCK rising edge to boundary scan input invalid	50.00		ns

Table 13. JTAG Timing



#### **IEEE 1149.1 Electrical Specifications**



#### Figure 35. JTAG Test Clock Input Timing



Figure 36. JTAG Test Access Port Timing Diagram



Figure 37. JTAG TRST Timing Diagram





# **11 CPM Electrical Characteristics**

This section provides the AC and DC electrical specifications for the communications processor module (CPM) of the MPC860.

## 11.1 PIP/PIO AC Electrical Specifications

Table 14 provides the PIP/PIO AC timings as shown in Figure 39 through Figure 43.

#### Table 14. PIP/PIO Timing

Num	Characteristic	All Freq	Unit	
Num	Onardetensite	Min	Max	Onit
21	Data-in setup time to STBI low	0	_	ns
22	Data-in hold time to STBI high	2.5 – t3 <sup>1</sup>	_	CLK
23	STBI pulse width	1.5	_	CLK
24	STBO pulse width	1 CLK – 5 ns	_	ns
25	Data-out setup time to STBO low	2	_	CLK
26	Data-out hold time from STBO high	5	_	CLK
27	STBI low to STBO low (Rx interlock)	_	2	CLK
28	STBI low to STBO high (Tx interlock)	2	_	CLK
29	Data-in setup time to clock high	15	_	ns
30	Data-in hold time from clock high	7.5	_	ns
31	Clock low to data-out valid (CPU writes data, control, or direction)		25	ns

<sup>1</sup> t3 = Specification 23.



Figure 39. PIP Rx (Interlock Mode) Timing Diagram





Figure 42. PIP TX (Pulse Mode) Timing Diagram





Figure 50. CPM General-Purpose Timers Timing Diagram

## **11.6 Serial Interface AC Electrical Specifications**

Table 19 provides the serial interface timings as shown in Figure 51 through Figure 55.

Num	Obevectovictie	All Frec	Unit	
NUM	Characteristic	Min	Max	Unit
70	L1RCLK, L1TCLK frequency (DSC = 0) <sup>1, 2</sup>	—	SYNCCLK/2.5	MHz
71	L1RCLK, L1TCLK width low $(DSC = 0)^2$	P + 10	—	ns
71a	L1RCLK, L1TCLK width high $(DSC = 0)^3$	P + 10	—	ns
72	L1TXD, L1ST(1–4), L1RQ, L1CLKO rise/fall time	—	15.00	ns
73	L1RSYNC, L1TSYNC valid to L1CLK edge (SYNC setup time)	20.00	—	ns
74	L1CLK edge to L1RSYNC, L1TSYNC, invalid (SYNC hold time)	35.00	—	ns
75	L1RSYNC, L1TSYNC rise/fall time	—	15.00	ns
76	L1RXD valid to L1CLK edge (L1RXD setup time)	17.00	—	ns
77	L1CLK edge to L1RXD invalid (L1RXD hold time)	13.00	—	ns
78	L1CLK edge to L1ST(1-4) valid <sup>4</sup>	10.00	45.00	ns
78A	L1SYNC valid to L1ST(1-4) valid	10.00	45.00	ns
79	L1CLK edge to L1ST(1-4) invalid	10.00	45.00	ns
80	L1CLK edge to L1TXD valid	10.00	55.00	ns
80A	L1TSYNC valid to L1TXD valid <sup>4</sup>	10.00	55.00	ns
81	L1CLK edge to L1TXD high impedance	0.00	42.00	ns
82	L1RCLK, L1TCLK frequency (DSC =1 ) - 16.00 or SYNCCLK/2		16.00 or SYNCCLK/2	MHz
83	L1RCLK, L1TCLK width low (DSC = 1)	P + 10	_	ns
83a	L1RCLK, L1TCLK width high $(DSC = 1)^3$	P + 10	—	ns

#### Table 19. SI Timing



**CPM Electrical Characteristics** 











**CPM Electrical Characteristics** 



MPC860 PowerQUICC Family Hardware Specifications, Rev. 10



#### SCC in NMSI Mode Electrical Specifications 11.7

Table 20 provides the NMSI external clock timing.

Table 2	20. NMSI	External	Clock	Timing
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Num	Characteristic	All Freq	Unit	
Nulli	Characteristic	Min	Мах	Unit
100	RCLK1 and TCLK1 width high <sup>1</sup>	1/SYNCCLK	_	ns
101	RCLK1 and TCLK1 width low	1/SYNCCLK + 5		ns
102	RCLK1 and TCLK1 rise/fall time	—	15.00	ns
103	TXD1 active delay (from TCLK1 falling edge)	0.00	50.00	ns
104	RTS1 active/inactive delay (from TCLK1 falling edge)	0.00	50.00	ns
105	CTS1 setup time to TCLK1 rising edge	5.00	—	ns
106	RXD1 setup time to RCLK1 rising edge	5.00	_	ns
107	RXD1 hold time from RCLK1 rising edge <sup>2</sup>	5.00	—	ns
108	CD1 setup Time to RCLK1 rising edge	5.00	_	ns

<sup>1</sup> The ratios SYNCCLK/RCLK1 and SYNCCLK/TCLK1 must be greater than or equal to 2.25/1.
 <sup>2</sup> Also applies to CD and CTS hold time when they are used as external sync signals.

#### Table 21 provides the NMSI internal clock timing.

#### Table 21. NMSI Internal Clock Timing

Num	Characteristic	All Freq	Unit	
Num	Characteristic	Min	Мах	Unit
100	RCLK1 and TCLK1 frequency <sup>1</sup>	0.00	SYNCCLK/3	MHz
102	RCLK1 and TCLK1 rise/fall time	—	—	ns
103	TXD1 active delay (from TCLK1 falling edge)	0.00	30.00	ns
104	RTS1 active/inactive delay (from TCLK1 falling edge)	0.00	30.00	ns
105	CTS1 setup time to TCLK1 rising edge	40.00	—	ns
106	RXD1 setup time to RCLK1 rising edge	40.00	—	ns
107	RXD1 hold time from RCLK1 rising edge <sup>2</sup>	0.00	_	ns
108	CD1 setup time to RCLK1 rising edge	40.00	_	ns

<sup>1</sup> The ratios SYNCCLK/RCLK1 and SYNCCLK/TCLK1 must be greater than or equal to 3/1.

<sup>2</sup> Also applies to  $\overline{CD}$  and  $\overline{CTS}$  hold time when they are used as external sync signals.







#### **UTOPIA AC Electrical Specifications**

Figure 70 shows signal timings during UTOPIA receive operations.



Figure 71 shows signal timings during UTOPIA transmit operations.



Figure 71. UTOPIA Transmit Timing



# 13.2 MII Transmit Signal Timing (MII\_TXD[3:0], MII\_TX\_EN, MII\_TX\_ER, MII\_TX\_CLK)

The transmitter functions correctly up to a MII\_TX\_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed the MII\_TX\_CLK frequency -1%.

Table 30 provides information on the MII transmit signal timing.

Table 30. MI	Transmit	Signal	Timing
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Num	Characteristic	Min	Max	Unit
M5	MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER invalid	5	_	ns
M6	MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER valid		25	
M7	MII_TX_CLK pulse width high	35	65%	MII_TX_CLK period
M8	MII_TX_CLK pulse width low	35%	65%	MII_TX_CLK period

Figure 73 shows the MII transmit signal timing diagram.



Figure 73. MII Transmit Signal Timing Diagram



# 13.3 MII Async Inputs Signal Timing (MII\_CRS, MII\_COL)

Table 31 provides information on the MII async inputs signal timing.

Table 31. MII Async Inputs Signal Timing

Num	Characteristic	Min	Мах	Unit
M9	MII_CRS, MII_COL minimum pulse width	1.5		MII_TX_CLK period

Figure 74 shows the MII asynchronous inputs signal timing diagram.



## 13.4 MII Serial Management Channel Timing (MII\_MDIO, MII\_MDC)

Table 32 provides information on the MII serial management channel signal timing. The FEC functions correctly with a maximum MDC frequency in excess of 2.5 MHz. The exact upper bound is under investigation.

Num	Characteristic	Min	Мах	Unit
M10	MII_MDC falling edge to MII_MDIO output invalid (minimum propagation delay)	0	_	ns
M11	MII_MDC falling edge to MII_MDIO output valid (max prop delay)	_	25	ns
M12	MII_MDIO (input) to MII_MDC rising edge setup	10	—	ns
M13	MII_MDIO (input) to MII_MDC rising edge hold		—	ns
M14	MII_MDC pulse width high	40%	60%	MII_MDC period
M15	MII_MDC pulse width low	40%	60%	MII_MDC period

#### Table 32. MII Serial Management Channel Timing



#### Mechanical Data and Ordering Information

Figure 75 shows the MII serial management channel timing diagram.



Figure 75. MII Serial Management Channel Timing Diagram

# 14 Mechanical Data and Ordering Information

### 14.1 Ordering Information

Table 33 provides information on the MPC860 Revision D.4 derivative devices.

Device	Number of SCCs <sup>1</sup>	Ethernet Support <sup>2</sup> (Mbps)	Multichannel HDLC Support	ATM Support
MPC855T	1	10/100	Yes	Yes
MPC860DE	2	10	N/A	N/A
MPC860DT		10/100	Yes	Yes
MPC860DP		10/100	Yes	Yes
MPC860EN	4	10	N/A	N/A
MPC860SR		10	Yes	Yes
MPC860T		10/100	Yes	Yes
MPC860P		10/100	Yes	Yes

Table 33. MPC860 Family Revision D.4 Derivatives

<sup>1</sup> Serial communications controller (SCC)

<sup>2</sup> Up to 4 channels at 40 MHz or 2 channels at 25 MHz