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Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	66MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (4), 10/100Mbps (1)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 95°C (TA)
Security Features	-
Package / Case	357-BBGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc860pvr66d4

1 Overview

The MPC860 power quad integrated communications controller (PowerQUICC™) is a versatile one-chip integrated microprocessor and peripheral combination designed for a variety of controller applications. It particularly excels in communications and networking systems. The PowerQUICC unit is referred to as the MPC860 in this hardware specification.

The MPC860 implements Power Architecture™ technology and contains a superset of Freescale's MC68360 quad integrated communications controller (QUICC), referred to here as the QUICC, RISC communications processor module (CPM). The CPU on the MPC860 is a 32-bit core built on Power Architecture technology that incorporates memory management units (MMUs) and instruction and data caches. The CPM from the MC68360 QUICC has been enhanced by the addition of the inter-integrated controller (I²C) channel. The memory controller has been enhanced, enabling the MPC860 to support any type of memory, including high-performance memories and new types of DRAMs. A PCMCIA socket controller supports up to two sockets. A real-time clock has also been integrated.

Table 1 shows the functionality supported by the MPC860 family.

Table 1. MPC860 Family Functionality

Part	Cache (Kbytes)		Ethernet		ATM	SCC	Reference ¹
	Instruction Cache	Data Cache	10T	10/100			
MPC860DE	4	4	Up to 2	—	—	2	1
MPC860DT	4	4	Up to 2	1	Yes	2	1
MPC860DP	16	8	Up to 2	1	Yes	2	1
MPC860EN	4	4	Up to 4	—	—	4	1
MPC860SR	4	4	Up to 4	—	Yes	4	1
MPC860T	4	4	Up to 4	1	Yes	4	1
MPC860P	16	8	Up to 4	1	Yes	4	1
MPC855T	4	4	1	1	Yes	1	2

¹ Supporting documentation for these devices refers to the following:

1. MPC860 PowerQUICC Family User's Manual (MPC860UM, Rev. 3)
2. MPC855T User's Manual (MPC855TUM, Rev. 1)

3 Maximum Tolerated Ratings

This section provides the maximum tolerated voltage and temperature ranges for the MPC860. [Table 2](#) provides the maximum ratings.

This device contains circuitry protecting against damage due to high-static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or V_{DD}).

Table 2. Maximum Tolerated Ratings

(GND = 0 V)

Rating	Symbol	Value	Unit
Supply voltage ¹	V_{DDH}	−0.3 to 4.0	V
	V_{DDL}	−0.3 to 4.0	V
	KAPWR	−0.3 to 4.0	V
	V_{DDSYN}	−0.3 to 4.0	V
Input voltage ²	V_{in}	GND − 0.3 to V_{DDH}	V
Temperature ³ (standard)	$T_{A(min)}$	0	°C
	$T_{j(max)}$	95	°C
Temperature ³ (extended)	$T_{A(min)}$	−40	°C
	$T_{j(max)}$	95	°C
Storage temperature range	T_{stg}	−55 to 150	°C

¹ The power supply of the device must start its ramp from 0.0 V.

² Functional operating conditions are provided with the DC electrical specifications in [Table 6](#). Absolute maximum ratings are stress ratings only; functional operation at the maxima is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device.

Caution: All inputs that tolerate 5 V cannot be more than 2.5 V greater than the supply voltage. This restriction applies to power-up and normal operation (that is, if the MPC860 is unpowered, voltage greater than 2.5 V must not be applied to its inputs).

³ Minimum temperatures are guaranteed as ambient temperature, T_A . Maximum temperatures are guaranteed as junction temperature, T_j .

5 Power Dissipation

Table 5 provides power dissipation information. The modes are 1:1, where CPU and bus speeds are equal, and 2:1, where CPU frequency is twice the bus speed.

Table 5. Power Dissipation (P_D)

Die Revision	Frequency (MHz)	Typical ¹	Maximum ²	Unit
D.4 (1:1 mode)	50	656	735	mW
	66	TBD	TBD	mW
D.4 (2:1 mode)	66	722	762	mW
	80	851	909	mW

¹ Typical power dissipation is measured at 3.3 V.

² Maximum power dissipation is measured at 3.5 V.

NOTE

Values in Table 5 represent V_{DDL} -based power dissipation and do not include I/O power dissipation over V_{DDH} . I/O power dissipation varies widely by application due to buffer current, depending on external circuitry.

6 DC Characteristics

Table 6 provides the DC electrical characteristics for the MPC860.

Table 6. DC Electrical Specifications

Characteristic	Symbol	Min	Max	Unit
Operating voltage at 40 MHz or less	V_{DDH} , V_{DDL} , V_{DDSYN}	3.0	3.6	V
	KAPWR (power-down mode)	2.0	3.6	V
	KAPWR (all other operating modes)	$V_{DDH} - 0.4$	V_{DDH}	V
Operating voltage greater than 40 MHz	V_{DDH} , V_{DDL} , KAPWR, V_{DDSYN}	3.135	3.465	V
	KAPWR (power-down mode)	2.0	3.6	V
	KAPWR (all other operating modes)	$V_{DDH} - 0.4$	V_{DDH}	V
Input high voltage (all inputs except EXTAL and EXTCLK)	V_{IH}	2.0	5.5	V
Input low voltage ¹	V_{IL}	GND	0.8	V
EXTAL, EXTCLK input high voltage	V_{IHC}	$0.7 \times (V_{DDH})$	$V_{DDH} + 0.3$	V
Input leakage current, $V_{in} = 5.5$ V (except TMS, $\overline{TRST}$, DSCK, and DSDI pins)	I_{in}	—	100	μA

Table 6. DC Electrical Specifications (continued)

Characteristic	Symbol	Min	Max	Unit
Input leakage current, $V_{in} = 3.6\text{ V}$ (except TMS, $\overline{\text{TRST}}$, DSCK, and DSDI pins)	I_{In}	—	10	μA
Input leakage current, $V_{in} = 0\text{ V}$ (except TMS, $\overline{\text{TRST}}$, DSCK, and DSDI pins)	I_{In}	—	10	μA
Input capacitance ²	C_{in}	—	20	pF
Output high voltage, $I_{OH} = -2.0\text{ mA}$, $V_{DDH} = 3.0\text{ V}$ (except XTAL, XFC, and open-drain pins)	V_{OH}	2.4	—	V
Output low voltage $I_{OL} = 2.0\text{ mA}$, CLKOUT $I_{OL} = 3.2\text{ mA}$ ³ $I_{OL} = 5.3\text{ mA}$ ⁴ $I_{OL} = 7.0\text{ mA}$, TXD1/PA14, TXD2/PA12 $I_{OL} = 8.9\text{ mA}$, $\overline{\text{TS}}$, $\overline{\text{TA}}$, $\overline{\text{TEA}}$, $\overline{\text{BI}}$, $\overline{\text{BB}}$, $\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$	V_{OL}	—	0.5	V

¹ $V_{IL}(\text{max})$ for the I²C interface is 0.8 V rather than the 1.5 V as specified in the I²C standard.

² Input capacitance is periodically sampled.

³ A(0:31), TSIZ0/ $\overline{\text{REG}}$, TSIZ1, D(0:31), DP(0:3)/ $\overline{\text{IRQ}}(3:6)$, RD/ $\overline{\text{WR}}$, $\overline{\text{BURST}}$, $\overline{\text{RSV}}/\overline{\text{IRQ2}}$, IP_B(0:1)/IWP(0:1)/VFLS(0:1), IP_B2/IOIS16_B/AT2, IP_B3/IWP2/VF2, IP_B4/LWP0/VF0, IP_B5/LWP1/VF1, IP_B6/DSDI/AT0, IP_B7/PTR/AT3, RXD1/PA15, RXD2/PA13, L1TXDB/PA11, L1RXDB/PA10, L1TXDA/PA9, L1RXDA/PA8, TIN1/L1RCLKA/BRGO1/CLK1/PA7, BRGCLK1/ $\overline{\text{TOUT1}}/\text{CLK2}/\text{PA6}$, TIN2/L1TCLKA/BRGO2/CLK3/PA5, $\overline{\text{TOUT2}}/\text{CLK4}/\text{PA4}$, TIN3/BRGO3/CLK5/PA3, BRGCLK2/L1RCLKB/ $\overline{\text{TOUT3}}/\text{CLK6}/\text{PA2}$, TIN4/BRGO4/CLK7/PA1, L1TCLKB/ $\overline{\text{TOUT4}}/\text{CLK8}/\text{PA0}$, $\overline{\text{REJCT1}}/\text{SPISEL}/\text{PB31}$, SPICLK/PB30, SPIMOSI/PB29, BRGO4/SPIMISO/PB28, BRGO1/I2CSDA/PB27, BRGO2/I2CSCL/PB26, SMTXD1/PB25, SMRXD1/PB24, $\overline{\text{SMSYN1}}/\overline{\text{SDACK1}}/\text{PB23}$, $\overline{\text{SMSYN2}}/\overline{\text{SDACK2}}/\text{PB22}$, SMTXD2/L1CLKOB/PB21, SMRXD2/L1CLKOA/PB20, L1ST1/ $\overline{\text{RTS1}}/\text{PB19}$, L1ST2/ $\overline{\text{RTS2}}/\text{PB18}$, L1ST3/L1RQB/PB17, L1ST4/L1RQA/PB16, BRGO3/PB15, $\overline{\text{RSTRT1}}/\text{PB14}$, L1ST1/ $\overline{\text{RTS1}}/\overline{\text{DREQ0}}/\text{PC15}$, L1ST2/ $\overline{\text{RTS2}}/\overline{\text{DREQ1}}/\text{PC14}$, L1ST3/L1RQB/PC13, L1ST4/L1RQA/PC12, $\overline{\text{CTS1}}/\text{PC11}$, $\overline{\text{TGATE1}}/\overline{\text{CD1}}/\text{PC10}$, $\overline{\text{CTS2}}/\text{PC9}$, $\overline{\text{TGATE2}}/\overline{\text{CD2}}/\text{PC8}$, $\overline{\text{SDACK2}}/\text{L1TSYNCA}/\text{PC7}$, L1RSYNCA/PC6, $\overline{\text{SDACK1}}/\text{L1TSYNCA}/\text{PC5}$, L1RSYNCA/PC4, PD15, PD14, PD13, PD12, PD11, PD10, PD9, PD8, PD5, PD6, PD7, PD4, PD3, MII_MDC, MII_TX_ER, MII_EN, MII_MDIO, and MII_TXD[0:3]

⁴ $\overline{\text{BDIP}}/\overline{\text{GPL}}_B(5)$, $\overline{\text{BR}}$, $\overline{\text{BG}}$, $\overline{\text{FRZ}}/\overline{\text{IRQ6}}$, $\overline{\text{CS}}(0:5)$, $\overline{\text{CS}}(6)/\overline{\text{CE}}(1)_B$, $\overline{\text{CS}}(7)/\overline{\text{CE}}(2)_B$, $\overline{\text{WE0}}/\overline{\text{BS}}_B0/\overline{\text{IORD}}$, $\overline{\text{WE1}}/\overline{\text{BS}}_B1/\overline{\text{IOWR}}$, $\overline{\text{WE2}}/\overline{\text{BS}}_B2/\overline{\text{PCOE}}$, $\overline{\text{WE3}}/\overline{\text{BS}}_B3/\overline{\text{PCWE}}$, $\overline{\text{BS}}_A(0:3)$, $\overline{\text{GPL}}_A0/\overline{\text{GPL}}_B0$, $\overline{\text{OE}}/\overline{\text{GPL}}_A1/\overline{\text{GPL}}_B1$, $\overline{\text{GPL}}_A(2:3)/\overline{\text{GPL}}_B(2:3)/\overline{\text{CS}}(2:3)$, UPWAITA/ $\overline{\text{GPL}}_A4$, UPWAITB/ $\overline{\text{GPL}}_B4$, $\overline{\text{GPL}}_A5$, ALE_A, $\overline{\text{CE1}}_A$, $\overline{\text{CE2}}_A$, ALE_B/DSCK/AT1, OP(0:1), OP2/MODCK1/ $\overline{\text{STS}}$, OP3/MODCK2/DSDO, and BADDR(28:30)

Figure 5 provides the timing for the synchronous output signals.

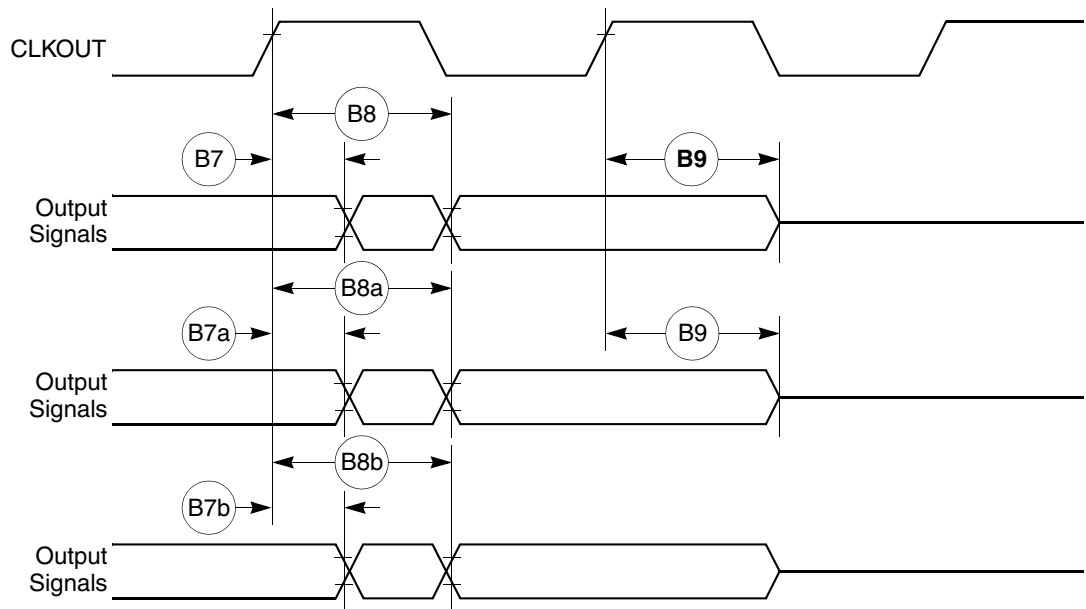


Figure 5. Synchronous Output Signals Timing

Figure 6 provides the timing for the synchronous active pull-up and open-drain output signals.

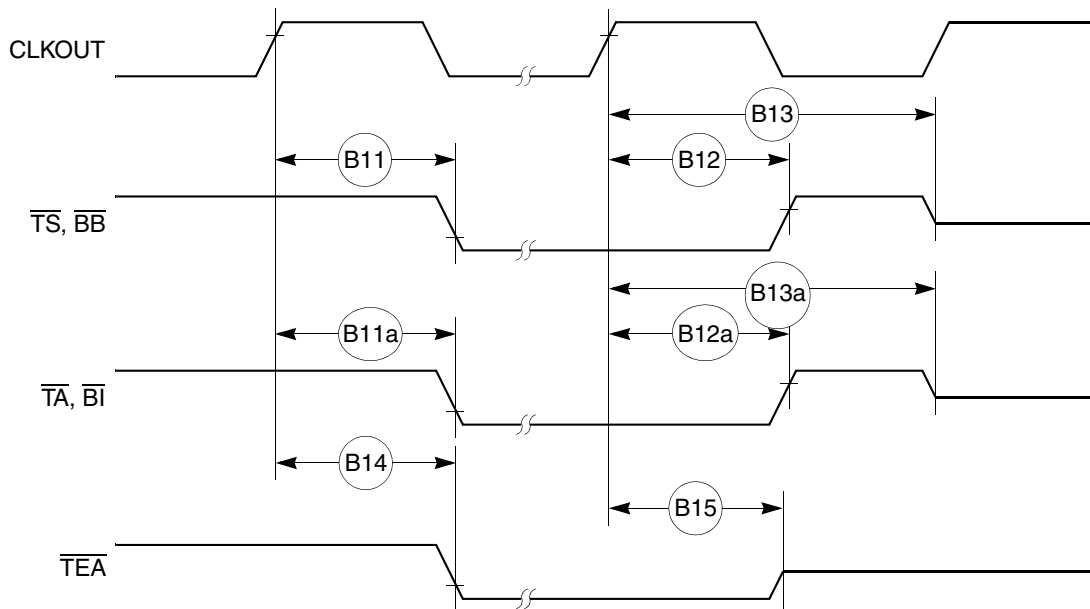


Figure 6. Synchronous Active Pull-Up Resistor and Open-Drain Outputs Signals Timing

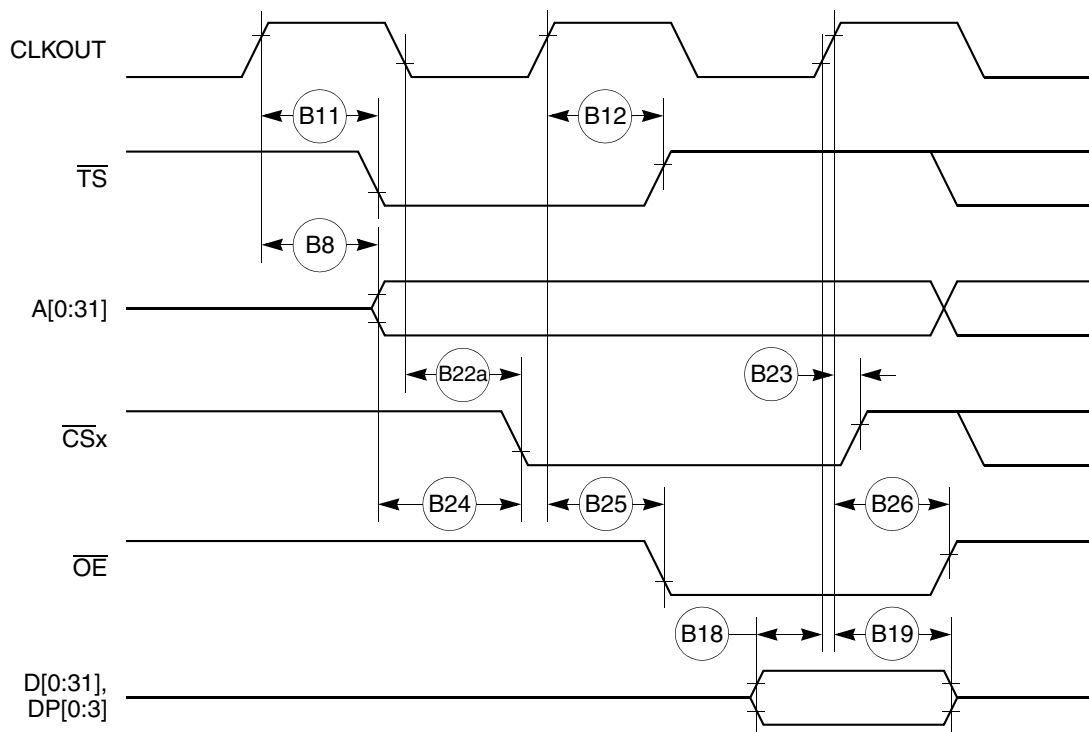


Figure 11. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 10)

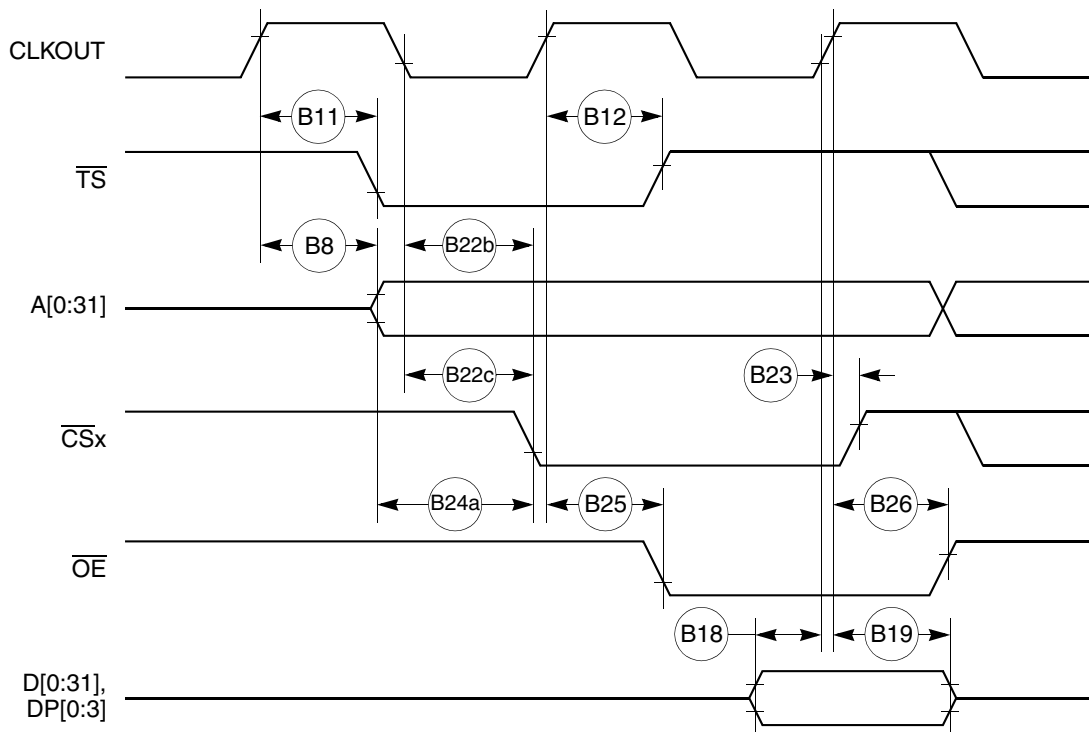


Figure 12. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 11)

Figure 14 through Figure 16 provide the timing for the external bus write controlled by various GPCM factors.

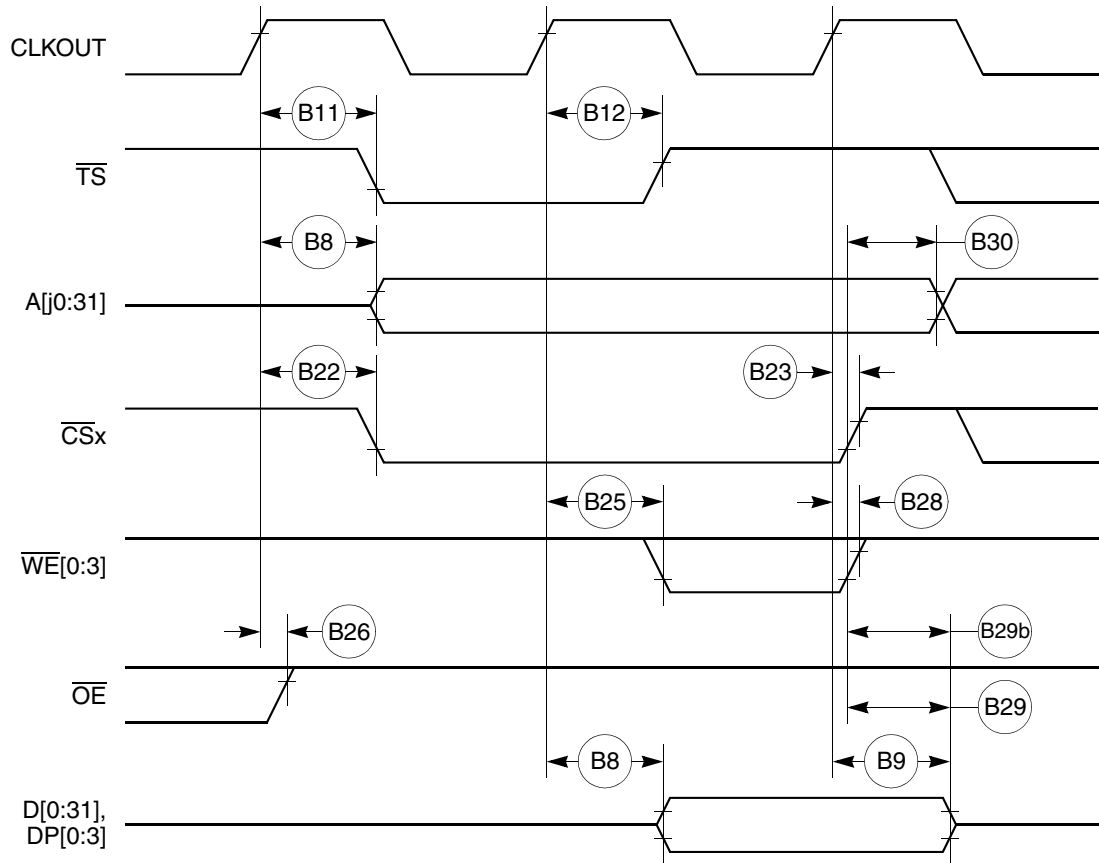


Figure 14. External Bus Write Timing (GPCM Controlled—TRLX = 0 or 1, CSNT = 0)

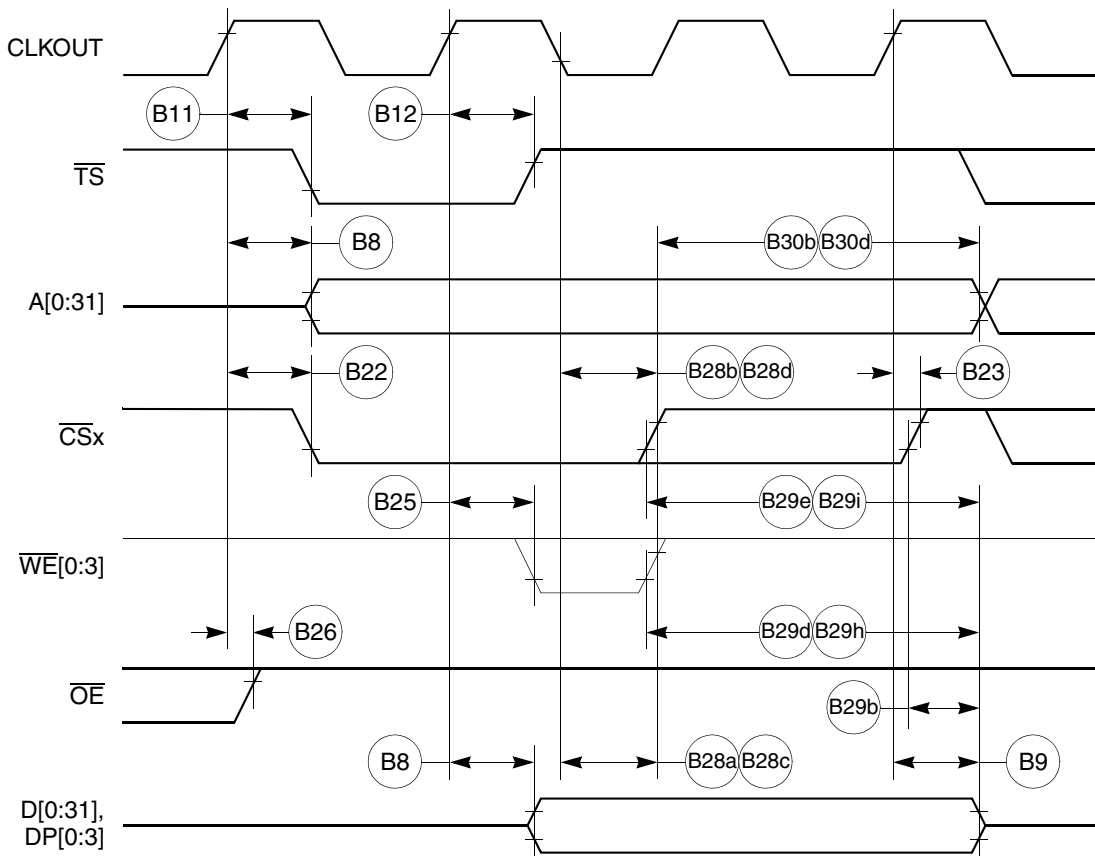


Figure 16. External Bus Write Timing (GPCM Controlled—TRLX = 0 or 1, CSNT = 1)

Figure 18 provides the timing for the asynchronous asserted UPWAIT signal controlled by the UPM.

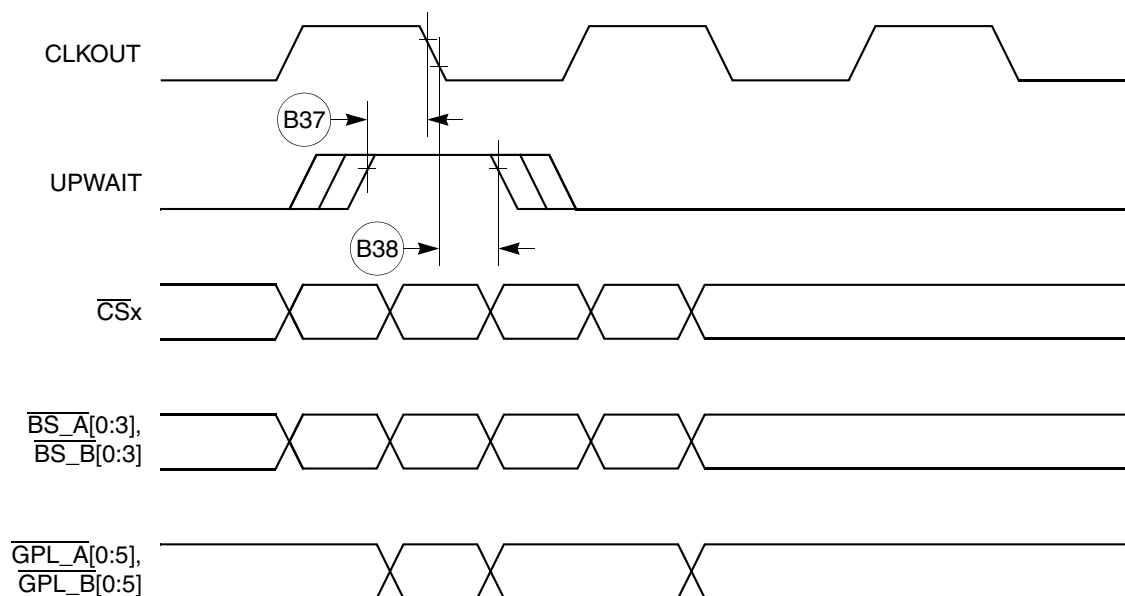


Figure 18. Asynchronous UPWAIT Asserted Detection in UPM Handled Cycles Timing

Figure 19 provides the timing for the asynchronous negated UPWAIT signal controlled by the UPM.

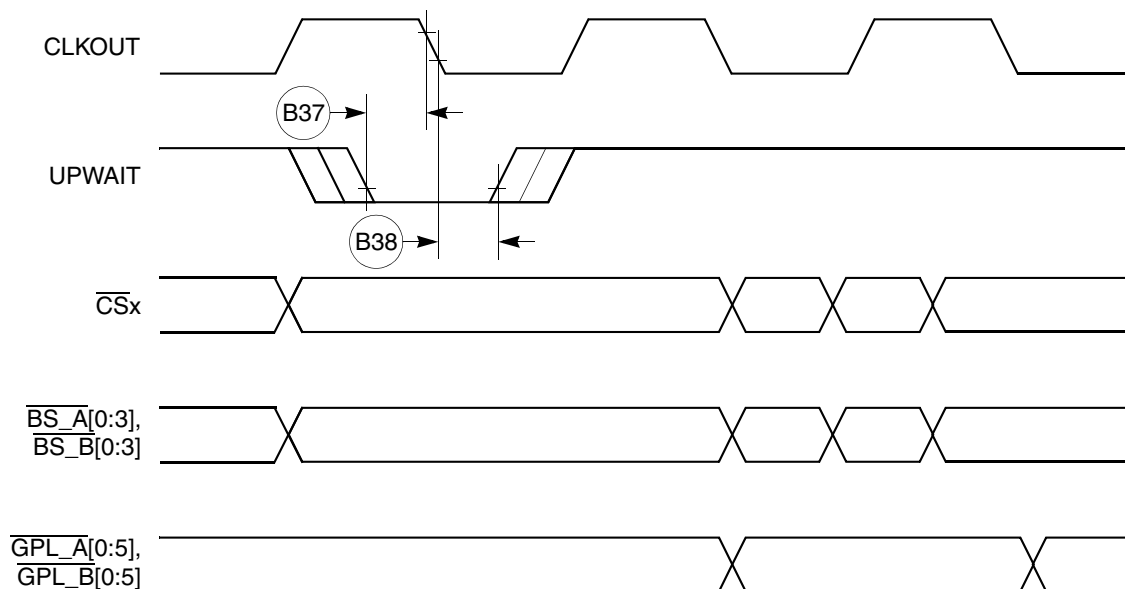


Figure 19. Asynchronous UPWAIT Negated Detection in UPM Handled Cycles Timing

Figure 26 provides the PCMCIA access cycle timing for the external bus write.

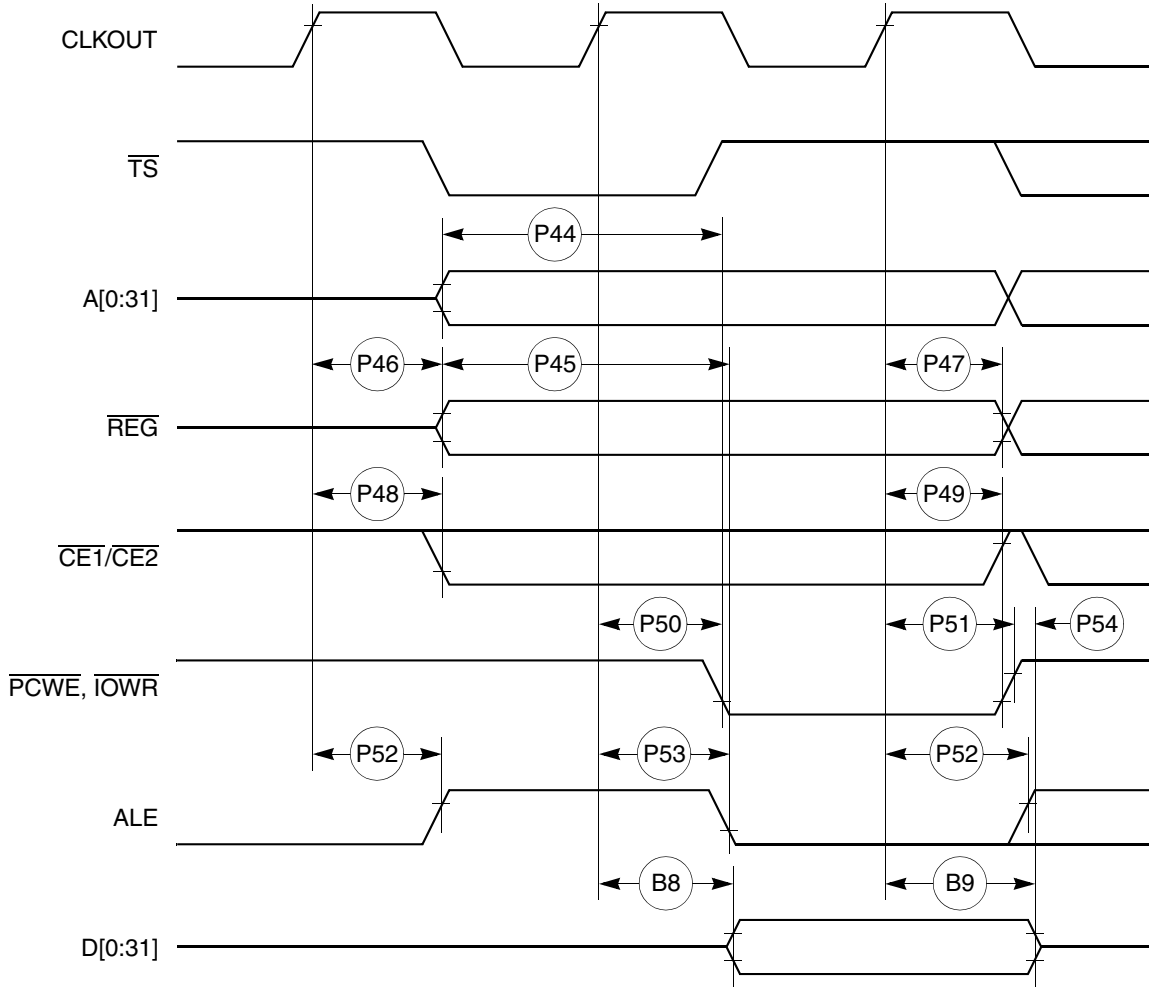


Figure 26. PCMCIA Access Cycle Timing External Bus Write

Figure 27 provides the PCMCIA $\overline{\text{WAIT}}$ signal detection timing.

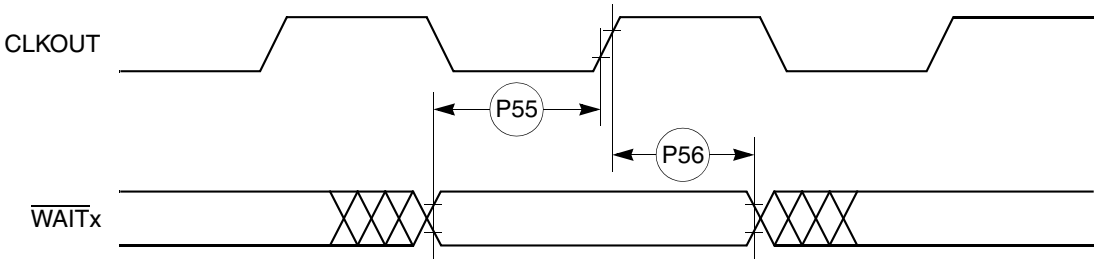


Figure 27. PCMCIA $\overline{\text{WAIT}}$ Signal Detection Timing

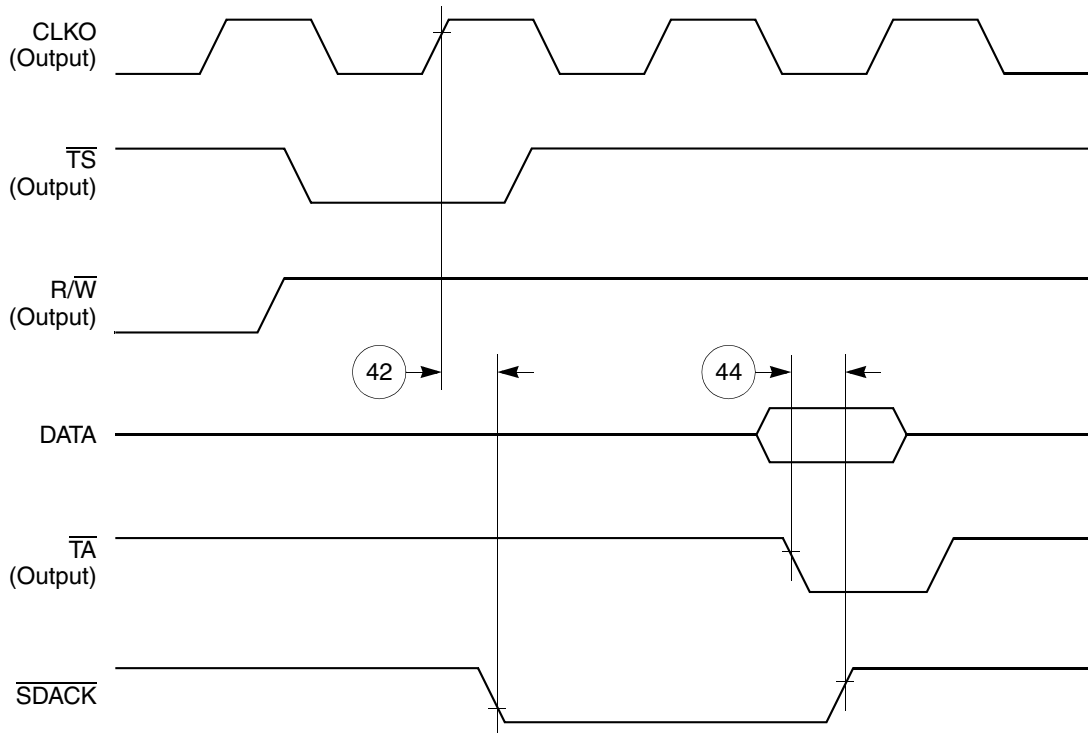


Figure 47. $\overline{SDACK}$ Timing Diagram—Peripheral Write, Internally-Generated $\overline{TA}$

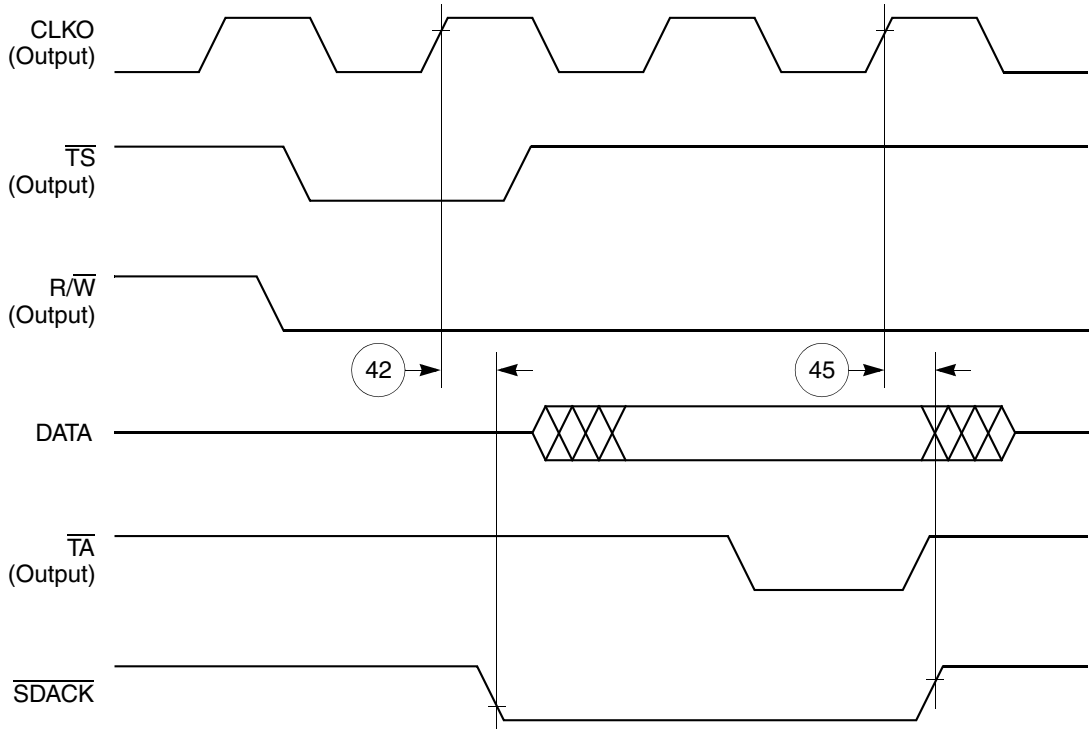


Figure 48. $\overline{SDACK}$ Timing Diagram—Peripheral Read, Internally-Generated $\overline{TA}$

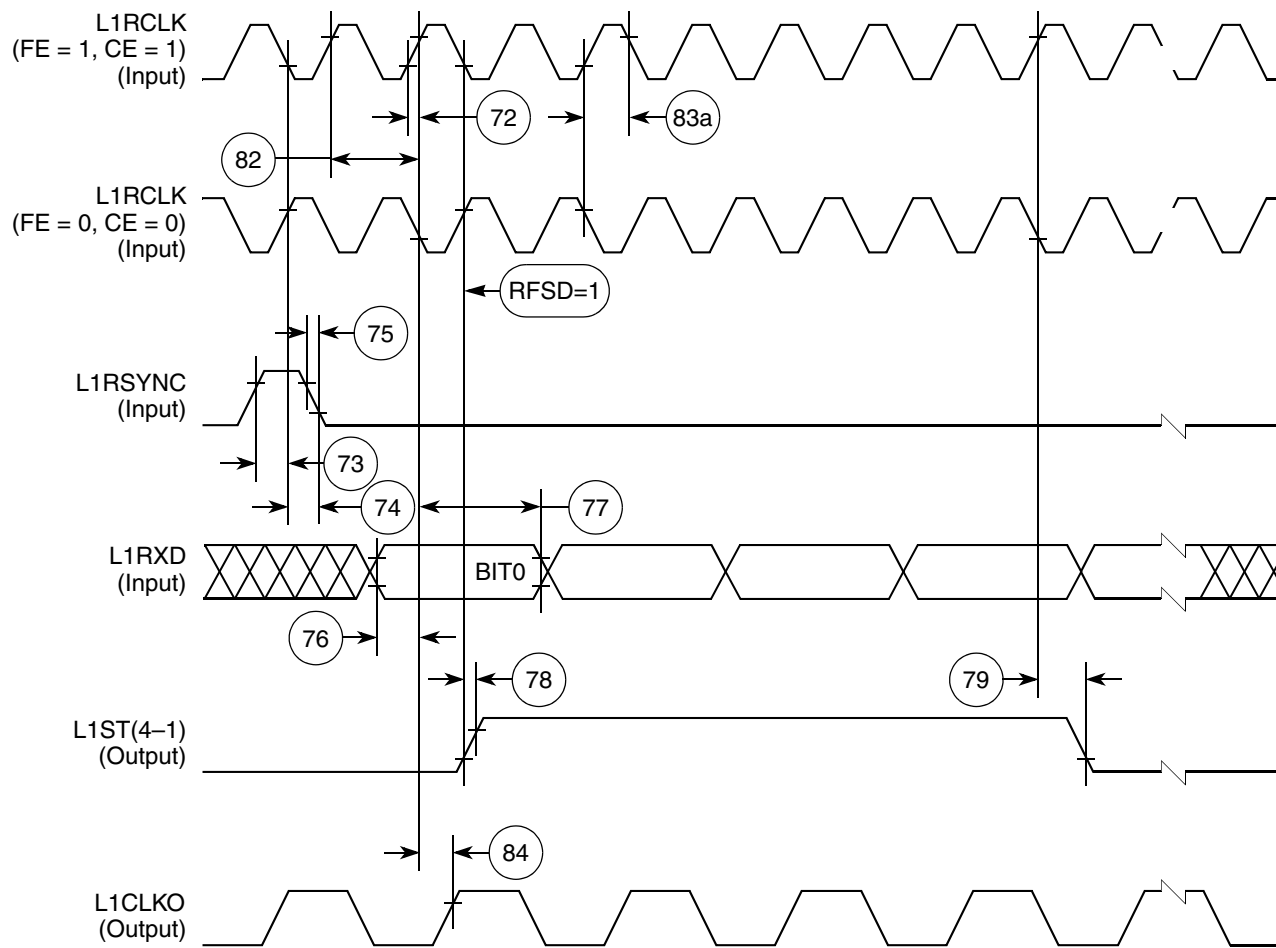


Figure 52. SI Receive Timing with Double-Speed Clocking (DSC = 1)

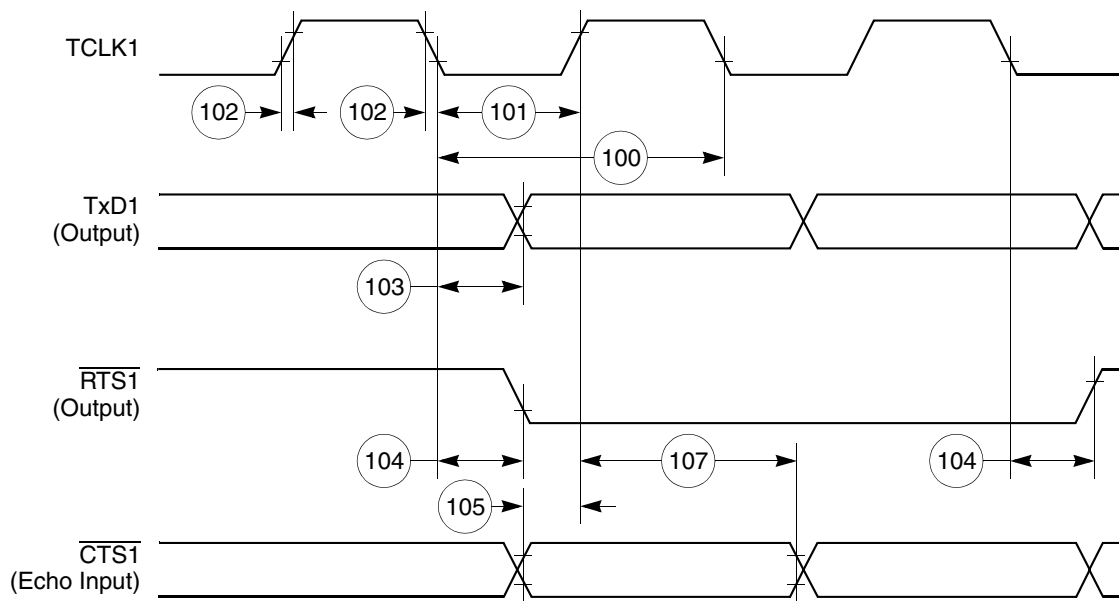


Figure 58. HDLC Bus Timing Diagram

11.8 Ethernet Electrical Specifications

Table 22 provides the Ethernet timings as shown in Figure 59 through Figure 63.

Table 22. Ethernet Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
120	CLSN width high	40	—	ns
121	RCLK1 rise/fall time	—	15	ns
122	RCLK1 width low	40	—	ns
123	RCLK1 clock period ¹	80	120	ns
124	RXD1 setup time	20	—	ns
125	RXD1 hold time	5	—	ns
126	RENA active delay (from RCLK1 rising edge of the last data bit)	10	—	ns
127	RENA width low	100	—	ns
128	TCLK1 rise/fall time	—	15	ns
129	TCLK1 width low	40	—	ns
130	TCLK1 clock period ¹	99	101	ns
131	TXD1 active delay (from TCLK1 rising edge)	10	50	ns
132	TXD1 inactive delay (from TCLK1 rising edge)	10	50	ns
133	TENA active delay (from TCLK1 rising edge)	10	50	ns
134	TENA inactive delay (from TCLK1 rising edge)	10	50	ns

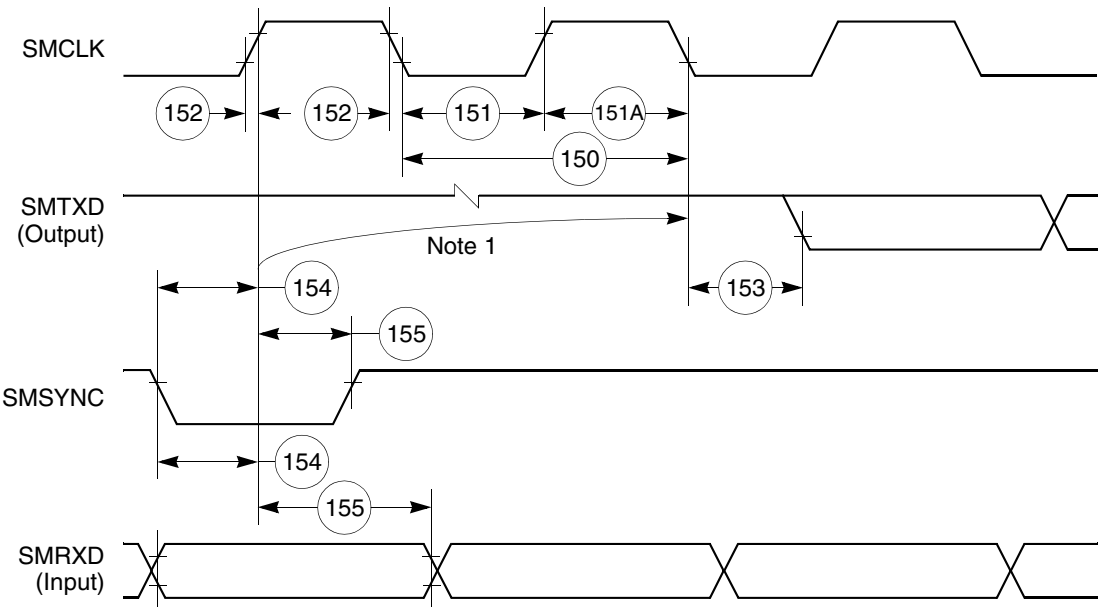
11.9 SMC Transparent AC Electrical Specifications

Table 23 provides the SMC transparent timings as shown in Figure 64.

Table 23. SMC Transparent Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
150	SMCLK clock period ¹	100	—	ns
151	SMCLK width low	50	—	ns
151A	SMCLK width high	50	—	ns
152	SMCLK rise/fall time	—	15	ns
153	SMTXD active delay (from SMCLK falling edge)	10	50	ns
154	SMRXD/SMSYNC setup time	20	—	ns
155	RXD1/SMSYNC hold time	5	—	ns

¹ SYNCCLK must be at least twice as fast as SMCLK.



Note:
1. This delay is equal to an integer number of character-length clocks.

Figure 64. SMC Transparent Timing Diagram

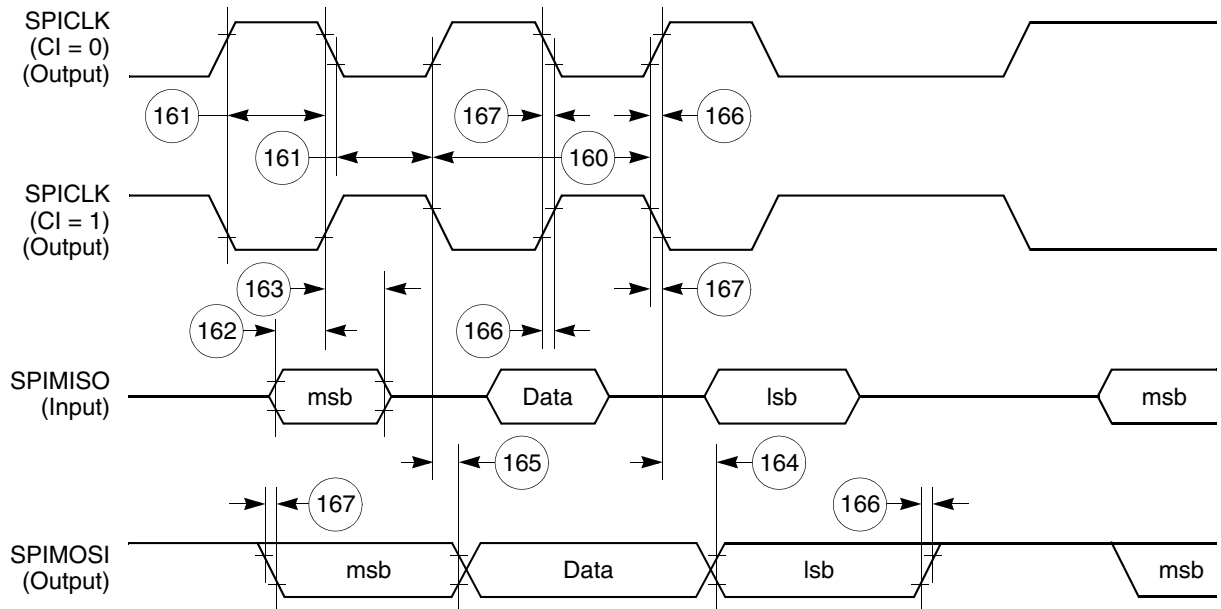


Figure 66. SPI Master (CP = 1) Timing Diagram

11.11 SPI Slave AC Electrical Specifications

Table 25 provides the SPI slave timings as shown in Figure 67 and Figure 68.

Table 25. SPI Slave Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
170	Slave cycle time	2	—	t_{cyc}
171	Slave enable lead time	15	—	ns
172	Slave enable lag time	15	—	ns
173	Slave clock (SPICLK) high or low time	1	—	t_{cyc}
174	Slave sequential transfer delay (does not require deselect)	1	—	t_{cyc}
175	Slave data setup time (inputs)	20	—	ns
176	Slave data hold time (inputs)	20	—	ns
177	Slave access time	—	50	ns

Figure 70 shows signal timings during UTOPIA receive operations.

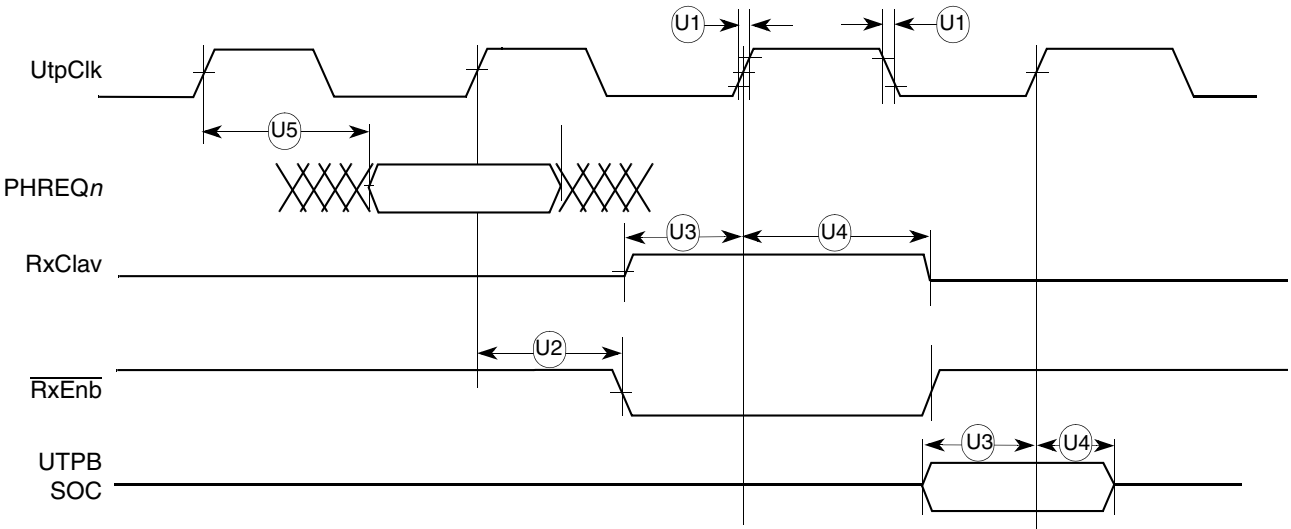


Figure 70. UTOPIA Receive Timing

Figure 71 shows signal timings during UTOPIA transmit operations.

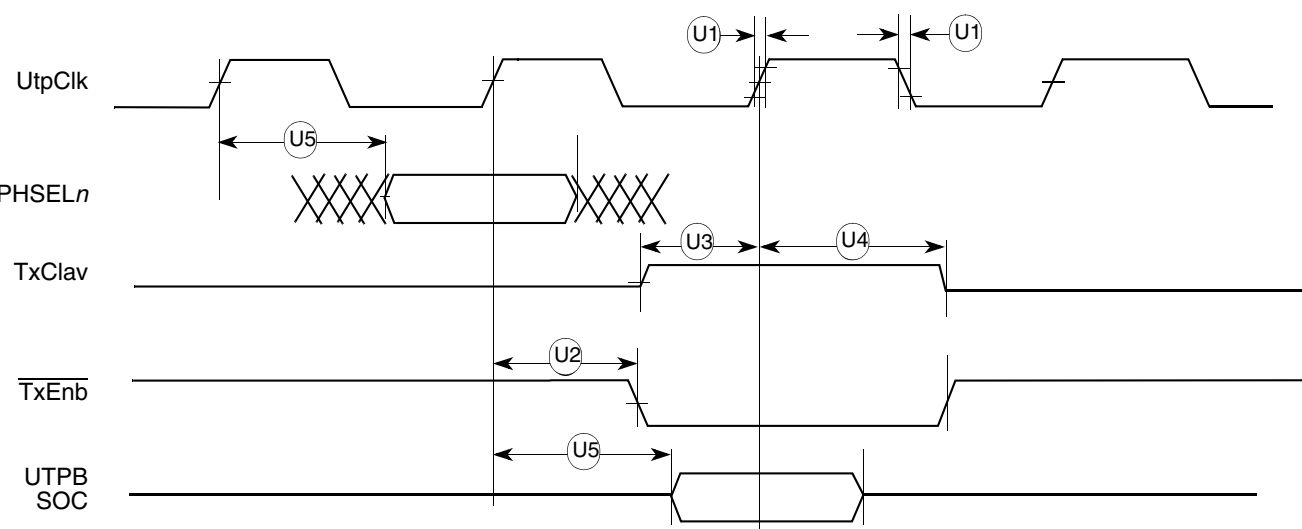


Figure 71. UTOPIA Transmit Timing

13.3 MII Async Inputs Signal Timing (MII_CRCS, MII_COL)

Table 31 provides information on the MII async inputs signal timing.

Table 31. MII Async Inputs Signal Timing

Num	Characteristic	Min	Max	Unit
M9	MII_CRCS, MII_COL minimum pulse width	1.5	—	MII_TX_CLK period

Figure 74 shows the MII asynchronous inputs signal timing diagram.

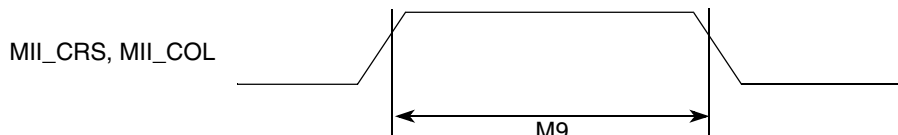


Figure 74. MII Async Inputs Timing Diagram

13.4 MII Serial Management Channel Timing (MII_MDIO, MII_MDC)

Table 32 provides information on the MII serial management channel signal timing. The FEC functions correctly with a maximum MDC frequency in excess of 2.5 MHz. The exact upper bound is under investigation.

Table 32. MII Serial Management Channel Timing

Num	Characteristic	Min	Max	Unit
M10	MII_MDC falling edge to MII_MDIO output invalid (minimum propagation delay)	0	—	ns
M11	MII_MDC falling edge to MII_MDIO output valid (max prop delay)	—	25	ns
M12	MII_MDIO (input) to MII_MDC rising edge setup	10	—	ns
M13	MII_MDIO (input) to MII_MDC rising edge hold	0	—	ns
M14	MII_MDC pulse width high	40%	60%	MII_MDC period
M15	MII_MDC pulse width low	40%	60%	MII_MDC period

Table 34 identifies the packages and operating frequencies available for the MPC860.

Table 34. MPC860 Family Package/Frequency Availability

Package Type	Freq. (MHz) / Temp. (Tj)	Package	Order Number
Ball grid array ZP suffix—leaded ZQ suffix—leaded VR suffix—lead-free	50 0° to 95°C	ZP/ZQ ¹	MPC855TZQ50D4 MPC860DEZQ50D4 MPC860DTZQ50D4 MPC860ENZQ50D4 MPC860SRZQ50D4 MPC860TZQ50D4 MPC860DPZQ50D4 MPC860PZQ50D4
		Tape and Reel	MPC855TZQ50D4R2 MPC860DEZQ50D4R2 MPC860ENZQ50D4R2 MPC860SRZQ50D4R2 MPC860TZQ50D4R2 MPC860DPZQ50D4R2 MPC855TVR50D4R2 MPC860ENVR50D4R2 MPC860SRVR50D4R2 MPC860TVR50D4R2
		VR	MPC855TVR50D4 MPC860DEV50D4 MPC860DPVR50D4 MPC860DTPVR50D4 MPC860ENVR50D4 MPC860PVR50D4 MPC860SRVR50D4 MPC860TVR50D4
	66 0° to 95°C	ZP/ZQ ¹	MPC855TZQ66D4 MPC860DEZQ66D4 MPC860DTZQ66D4 MPC860ENZQ66D4 MPC860SRZQ66D4 MPC860TZQ66D4 MPC860DPZQ66D4 MPC860PZQ66D4
		Tape and Reel	MPC860SRZQ66D4R2 MPC860PZQ66D4R2
		VR	MPC855TVR66D4 MPC860DEV66D4 MPC860DPVR66D4 MPC860DTPVR66D4 MPC860ENVR66D4 MPC860PVR66D4 MPC860SRVR66D4 MPC860TVR66D4

14.2 Pin Assignments

Figure 76 shows the top view pinout of the PBGA package. For additional information, see the *MPC860 PowerQUICC User's Manual*, or the *MPC855T User's Manual*.

NOTE: This is the top view of the device.

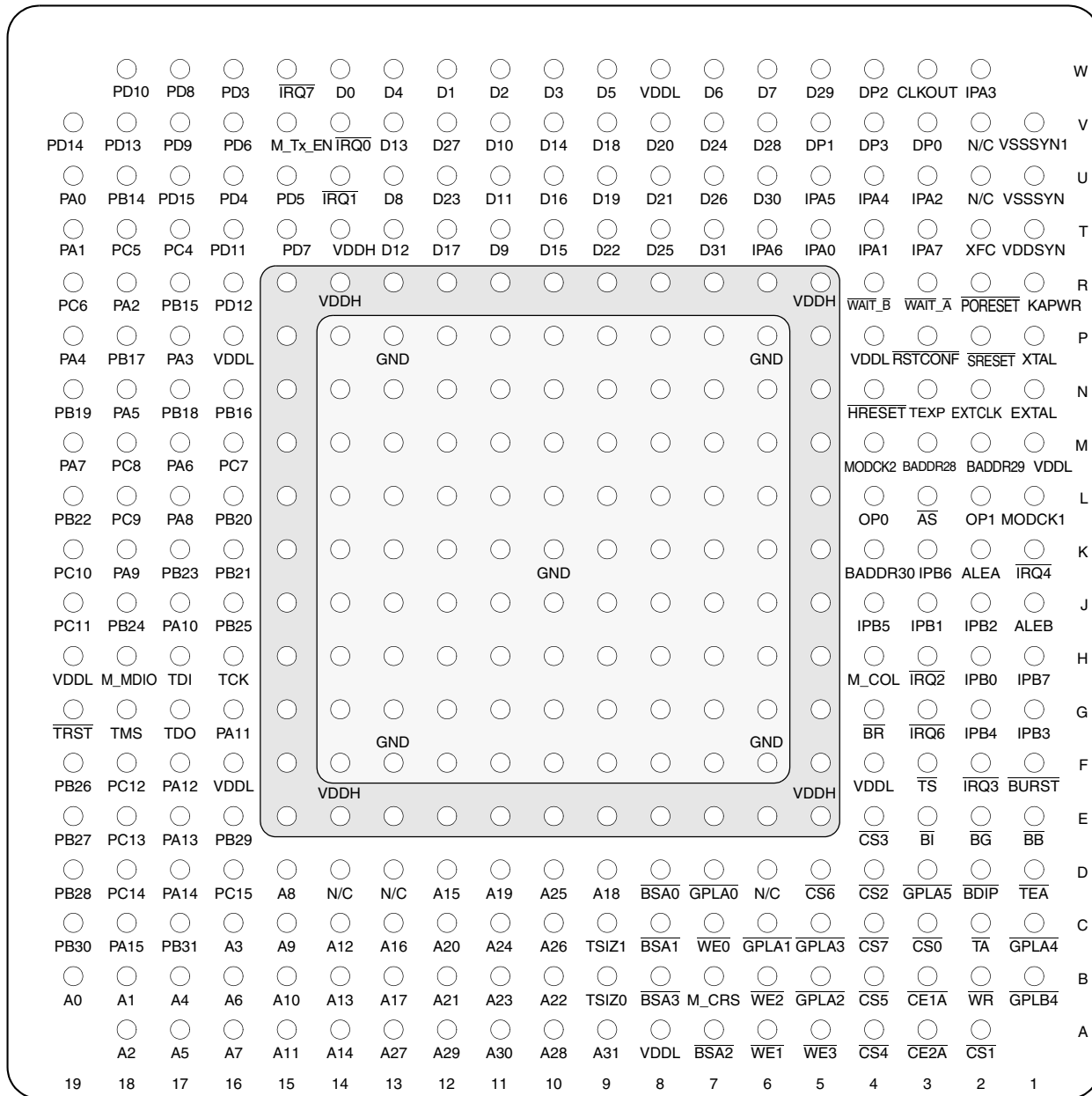
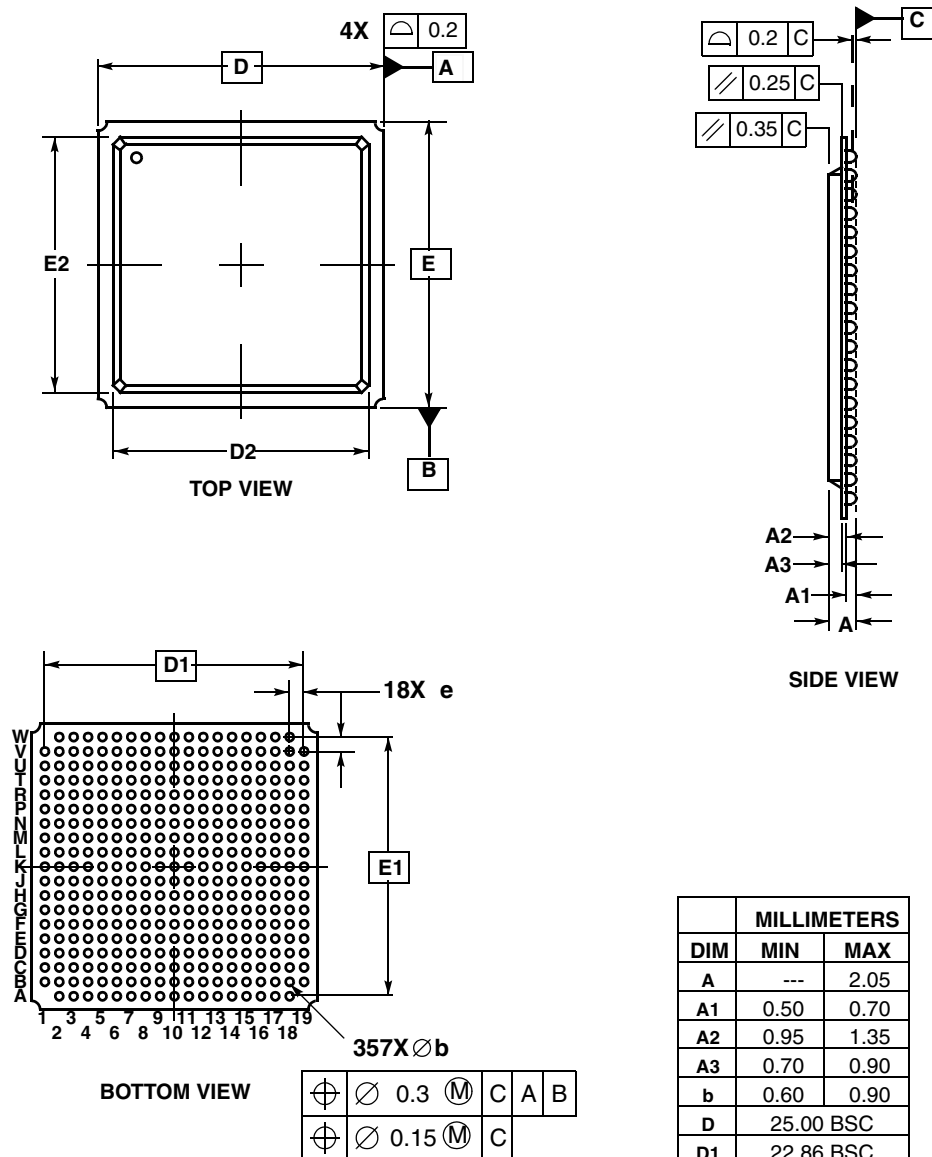


Figure 76. Pinout of the PBGA Package

14.3 Mechanical Dimensions of the PBGA Package

Figure 77 shows the mechanical dimensions of the ZP PBGA package.



NOTE

1. Dimensions and tolerance per ASME Y14.5M, 1994.
2. Dimensions in millimeters.
3. Dimension b is the maximum solder ball diameter measured parallel to data C.

Figure 77. Mechanical Dimensions and Bottom Surface Nomenclature of the ZP PBGA Package