NXP USA Inc. - KMPC860PVR80D4 Datasheet



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Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Obsolete
MPC8xx
1 Core, 32-Bit
80MHz
Communications; CPM
DRAM
No
-
10Mbps (4), 10/100Mbps (1)
-
-
3.3V
0°C ~ 95°C (TA)
-
357-BBGA
357-PBGA (25x25)
https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc860pvr80d4

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2 Features

The following list summarizes the key MPC860 features:

- Embedded single-issue, 32-bit core (implementing the Power Architecture technology) with thirty-two 32-bit general-purpose registers (GPRs)
 - The core performs branch prediction with conditional prefetch without conditional execution.
 - 4- or 8-Kbyte data cache and 4- or 16-Kbyte instruction cache (see Table 1)
 - 16-Kbyte instruction caches are four-way, set-associative with 256 sets; 4-Kbyte instruction caches are two-way, set-associative with 128 sets.
 - 8-Kbyte data caches are two-way, set-associative with 256 sets; 4-Kbyte data caches are two-way, set-associative with 128 sets.
 - Cache coherency for both instruction and data caches is maintained on 128-bit (4-word) cache blocks.
 - Caches are physically addressed, implement a least recently used (LRU) replacement algorithm, and are lockable on a cache block basis.
 - MMUs with 32-entry TLB, fully-associative instruction, and data TLBs
 - MMUs support multiple page sizes of 4-, 16-, and 512-Kbytes, and 8-Mbytes; 16 virtual address spaces and 16 protection groups
 - Advanced on-chip-emulation debug mode
- Up to 32-bit data bus (dynamic bus sizing for 8, 16, and 32 bits)
- 32 address lines
- Operates at up to 80 MHz
- Memory controller (eight banks)
 - Contains complete dynamic RAM (DRAM) controller
 - Each bank can be a chip select or \overline{RAS} to support a DRAM bank.
 - Up to 15 wait states programmable per memory bank
 - Glueless interface to DRAM, SIMMS, SRAM, EPROM, Flash EPROM, and other memory devices
 - DRAM controller programmable to support most size and speed memory interfaces
 - Four $\overline{\text{CAS}}$ lines, four $\overline{\text{WE}}$ lines, and one $\overline{\text{OE}}$ line
 - Boot chip-select available at reset (options for 8-, 16-, or 32-bit memory)
 - Variable block sizes (32 Kbytes to 256 Mbytes)
 - Selectable write protection
 - On-chip bus arbitration logic
- General-purpose timers
 - Four 16-bit timers or two 32-bit timers
 - Gate mode can enable/disable counting
 - Interrupt can be masked on reference match and event capture.



3 Maximum Tolerated Ratings

This section provides the maximum tolerated voltage and temperature ranges for the MPC860. Table 2 provides the maximum ratings.

This device contains circuitry protecting against damage due to high-static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or V_{DD}).

(GND = 0 V)

Table 2. Maximum Tolerated Ratings

Rating	Symbol	Value	Unit
Supply voltage ¹	V _{DDH}	-0.3 to 4.0	V
	V _{DDL}	-0.3 to 4.0	V
	KAPWR	-0.3 to 4.0	V
	V _{DDSYN}	-0.3 to 4.0	V
Input voltage ²	V _{in}	GND – 0.3 to V _{DDH}	V
Temperature ³ (standard)	T _{A(min)}	0	°C
	T _{j(max)}	95	°C
Temperature ³ (extended)	T _{A(min)}	-40	°C
	T _{j(max)}	95	°C
Storage temperature range	T _{stg}	-55 to 150	°C

¹ The power supply of the device must start its ramp from 0.0 V.

² Functional operating conditions are provided with the DC electrical specifications in Table 6. Absolute maximum ratings are stress ratings only; functional operation at the maxima is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device.

Caution: All inputs that tolerate 5 V cannot be more than 2.5 V greater than the supply voltage. This restriction applies to power-up and normal operation (that is, if the MPC860 is unpowered, voltage greater than 2.5 V must not be applied to its inputs).

³ Minimum temperatures are guaranteed as ambient temperature, T_A. Maximum temperatures are guaranteed as junction temperature, T_j.



Thermal Characteristics

Figure 1 shows the undershoot and overshoot voltages at the interface of the MPC860.



1. t_{interface} refers to the clock period associated with the bus clock interface.

Figure 1. Undershoot/Overshoot Voltage for V_{DDH} and V_{DDL}

4 Thermal Characteristics

Table 3. Package Description

Package Designator	Package Code (Case No.)	Package Description
ZP	5050 (1103-01)	PBGA 357 25*25*0.9P1.27
ZQ/VR	5058 (1103D-02)	PBGA 357 25*25*1.2P1.27



Power Dissipation

5 **Power Dissipation**

Table 5 provides power dissipation information. The modes are 1:1, where CPU and bus speeds are equal, and 2:1, where CPU frequency is twice the bus speed.

Die Revision	Frequency (MHz)	Typical ¹	Maximum ²	Unit
D.4	50	656	735	mW
(1:1 mode)	66	TBD	TBD	mW
D.4	66	722	762	mW
(2:1 mode)	80	851	909	mW

Table 5. Power Dissipation (PD)

¹ Typical power dissipation is measured at 3.3 V.

² Maximum power dissipation is measured at 3.5 V.

NOTE

Values in Table 5 represent V_{DDL} -based power dissipation and do not include I/O power dissipation over V_{DDH} . I/O power dissipation varies widely by application due to buffer current, depending on external circuitry.

6 DC Characteristics

Table 6 provides the DC electrical characteristics for the MPC860.

 Table 6. DC Electrical Specifications

Characteristic	Symbol	Min	Мах	Unit
Operating voltage at 40 MHz or less	V _{DDH} , V _{DDL} , V _{DDSYN}	3.0	3.6	V
	KAPWR (power-down mode)	2.0	3.6	V
	KAPWR (all other operating modes)	V _{DDH} – 0.4	V _{DDH}	V
Operating voltage greater than 40 MHz	V _{DDH} , V _{DDL} , KAPWR, V _{DDSYN}	3.135	3.465	V
	KAPWR (power-down mode)	2.0	3.6	V
	KAPWR (all other operating modes)	V _{DDH} – 0.4	V _{DDH}	V
Input high voltage (all inputs except EXTAL and EXTCLK)	V _{IH}	2.0	5.5	V
Input low voltage ¹	V _{IL}	GND	0.8	V
EXTAL, EXTCLK input high voltage	V _{IHC}	$0.7 imes (V_{DDH})$	V _{DDH} + 0.3	V
Input leakage current, $V_{in} = 5.5 \text{ V}$ (except TMS, TRST, DSCK, and DSDI pins)	l _{in}	—	100	μA



Characteristic	Symbol	Min	Max	Unit
Input leakage current, V_{in} = 3.6 V (except TMS, TRST, DSCK, and DSDI pins)	l _{in}	—	10	μA
Input leakage current, V _{in} = 0 V (except TMS, TRST, DSCK, and DSDI pins)	l _{in}	—	10	μA
Input capacitance ²	C _{in}	—	20	pF
Output high voltage, $I_{OH} = -2.0$ mA, $V_{DDH} = 3.0$ V (except XTAL, XFC, and open-drain pins)	V _{OH}	2.4	—	V
$\label{eq:IDE_Interm} \begin{array}{ c c c c c } \hline Output low voltage \\ I_{OL} = 2.0 \text{ mA, CLKOUT} \\ I_{OL} = 3.2 \text{ mA}^3 \\ I_{OL} = 5.3 \text{ mA}^4 \\ I_{OL} = 7.0 \text{ mA, TXD1/PA14, TXD2/PA12} \\ I_{OL} = 8.9 \text{ mA, TS, TA, TEA, BI, BB, HRESET, SRESET} \end{array}$	V _{OL}		0.5	V

Table 6. DC Electrical Specifications (continued)

 1 V_{IL}(max) for the I²C interface is 0.8 V rather than the 1.5 V as specified in the I²C standard.

² Input capacitance is periodically sampled.

- ³ A(0:31), TSIZ0/REG, TSIZ1, D(0:31), DP(0:3)/IRQ(3:6), RD/WR, BURST, RSV/IRQ2, IP_B(0:1)/IWP(0:1)/VFLS(0:1), IP_B2/IOIS16_B/AT2, IP_B3/IWP2/VF2, IP_B4/LWP0/VF0, IP_B5/LWP1/VF1, IP_B6/DSDI/AT0, IP_B7/PTR/AT3, RXD1/PA15, RXD2/PA13, L1TXDB/PA11, L1RXDB/PA10, L1TXDA/PA9, L1RXDA/PA8, TIN1/L1RCLKA/BRGO1/CLK1/PA7, BRGCLK1/TOUT1/CLK2/PA6, TIN2/L1TCLKA/BRGO2/CLK3/PA5, TOUT2/CLK4/PA4, TIN3/BRGO3/CLK5/PA3, BRGCLK2/ L1RCLKB/TOUT3/CLK6/PA2, TIN4/BRGO4/CLK7/PA1, L1TCLKB/TOUT4/CLK8/PA0, REJCT1/SPISEL/PB31, SPICLK/ PB30,SPIMOSI/PB29, BRGO4/SPIMISO/PB28, BRGO1/I2CSDA/PB27, BRGO2/I2CSCL/PB26, SMTXD1/PB25, SMRXD1/ PB24, SMSYN1/SDACK1/PB23, SMSYN2/SDACK2/PB22, SMTXD2/L1CLKOB/PB21, SMRXD2/L1CLKOA/PB20, L1ST1/ RTS1/PB19, L1ST2/RTS2/PB18, L1ST3/L1RQB/PB17, L1ST4/L1RQA/PB16, BRGO3/PB15, RSTRT1/PB14, L1ST1/RTS1/ DREQ0/PC15, L1ST2/RTS2/DREQ1/PC14, L1ST3/L1RQB/PC13, L1ST4/L1RQA/PC12, CTS1/PC11, TGATE1/CD1/PC10, CTS2/PC9, TGATE2/CD2/PC8, SDACK2/L1TSYNCB/PC7, L1RSYNCB/PC6, SDACK1/L1TSYNCA/PC5, L1RSYNCA/PC4, PD15, PD14, PD13, PD12, PD11, PD10, PD9, PD8, PD5, PD6, PD7, PD4, PD3, MII_MDC, MII_TX_ER, MII_EN, MII_MDIO, and MII_TXD[0:3]
- ⁴ BDIP/GPL_B(5), BR, BG, FRZ/IRQ6, CS(0:5), CS(6)/CE(1)_B, CS(7)/CE(2)_B, WE0/BS_B0/IORD, WE1/BS_B1/IOWR, WE2/BS_B2/PCOE, WE3/BS_B3/PCWE, BS_A(0:3), GPL_A0/GPL_B0, OE/GPL_A1/GPL_B1, GPL_A(2:3)/GPL_B(2:3)/ CS(2:3), UPWAITA/GPL_A4, UPWAITB/GPL_B4, GPL_A5, ALE_A, CE1_A, CE2_A, ALE_B/DSCK/AT1, OP(0:1), OP2/MODCK1/STS, OP3/MODCK2/DSDO, and BADDR(28:30)



	Ohennetheristie	33 MHz		40 MHz		50 MHz		66 MHz		
Num	Characteristic	Min	Мах	Min	Max	Min	Мах	Min	Max	Unit
B23	CLKOUT rising edge to \overline{CS} negated GPCM read access, GPCM write access ACS = 00, TRLX = 0, and CSNT = 0	2.00	8.00	2.00	8.00	2.00	8.00	2.00	8.00	ns
B24	A(0:31) and BADDR(28:30) to \overline{CS} asserted GPCM ACS = 10, TRLX = 0	5.58	—	4.25	_	3.00	_	1.79	—	ns
B24a	A(0:31) and BADDR(28:30) to \overline{CS} asserted GPCM ACS = 11, TRLX = 0	13.15	—	10.50	—	8.00	—	5.58	—	ns
B25	CLKOUT rising edge to \overline{OE} , \overline{WE} (0:3) asserted	—	9.00	—	9.00	—	9.00	—	9.00	ns
B26	CLKOUT rising edge to OE negated	2.00	9.00	2.00	9.00	2.00	9.00	2.00	9.00	ns
B27	A(0:31) and BADDR(28:30) to \overline{CS} asserted GPCM ACS = 10, TRLX = 1	35.88	_	29.25	_	23.00	_	16.94	_	ns
B27a	A(0:31) and BADDR(28:30) to \overline{CS} asserted GPCM ACS = 11, TRLX = 1	43.45	—	35.50	—	28.00	—	20.73	—	ns
B28	CLKOUT rising edge to $\overline{WE}(0:3)$ negated GPCM write access CSNT = 0	—	9.00	—	9.00	—	9.00	—	9.00	ns
B28a	CLKOUT falling edge to $\overline{WE}(0:3)$ negated GPCM write access TRLX = 0, 1, CSNT = 1, EBDF = 0	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.54	ns
B28b	CLKOUT falling edge to \overline{CS} negated GPCM write access TRLX = 0, 1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 0	—	14.33	—	13.00		11.75		10.54	ns
B28c	CLKOUT falling edge to \overline{WE} (0:3) negated GPCM write access TRLX = 0, 1, CSNT = 1 write access TRLX = 0, CSNT = 1, EBDF = 1	10.86	17.99	8.88	16.00	7.00	14.13	5.18	12.31	ns
B28d	CLKOUT falling edge to \overline{CS} negated GPCM write access TRLX = 0, 1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 1	_	17.99	_	16.00		14.13		12.31	ns
B29	$\overline{WE}(0:3)$ negated to D(0:31), DP(0:3) High-Z GPCM write access CSNT = 0, EBDF = 0	5.58	_	4.25	—	3.00	—	1.79	—	ns
B29a	$\overline{WE}(0:3)$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 0	13.15	—	10.5	—	8.00		5.58	—	ns
B29b	$\overline{\text{CS}}$ negated to D(0:31), DP(0:3), High-Z GPCM write access, ACS = 00, TRLX = 0, 1, and CSNT = 0	5.58		4.25		3.00		1.79		ns
B29c	$\overline{\text{CS}}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 0	13.15		10.5		8.00		5.58		ns

Table 7. Bus Operation Timings (continued)



Bus Signal Timing

	Oh ann atamiatia	33 MHz		40 MHz		50 MHz		66 MHz		11
NUM	Characteristic	Min	Max	Min	Max	Min	Max	Min	Max	Unit
B35	A(0:31), BADDR(28:30) to \overline{CS} valid—as requested by control bit BST4 in the corresponding word in UPM	5.58	_	4.25	_	3.00	_	1.79	_	ns
B35a	A(0:31), BADDR(28:30), and D(0:31) to $\overline{\text{BS}}$ valid—as requested by control bit BST1 in the corresponding word in UPM	13.15	—	10.50	—	8.00	—	5.58	_	ns
B35b	A(0:31), BADDR(28:30), and D(0:31) to $\overline{\text{BS}}$ valid—as requested by control bit BST2 in the corresponding word in UPM	20.73	—	16.75	—	13.00	—	9.36		ns
B36	A(0:31), BADDR(28:30), and D(0:31) to GPL valid—as requested by control bit GxT4 in the corresponding word in UPM	5.58	—	4.25	—	3.00	—	1.79	_	ns
B37	UPWAIT valid to CLKOUT falling edge ⁹	6.00	—	6.00	—	6.00	—	6.00		ns
B38	CLKOUT falling edge to UPWAIT valid ⁹	1.00	—	1.00	_	1.00	_	1.00	_	ns
B39	AS valid to CLKOUT rising edge ¹⁰	7.00	_	7.00	_	7.00	_	7.00	_	ns
B40	A(0:31), TSIZ(0:1), RD/WR, BURST, valid to CLKOUT rising edge	7.00	—	7.00	—	7.00	—	7.00	_	ns
B41	$\overline{\text{TS}}$ valid to CLKOUT rising edge (setup time)	7.00	—	7.00	_	7.00	_	7.00	_	ns
B42	CLKOUT rising edge to \overline{TS} valid (hold time)	2.00	—	2.00	—	2.00	—	2.00	_	ns
B43	AS negation to memory controller signals negation	_	TBD	_	TBD	_	TBD	_	TBD	ns

¹ Phase and frequency jitter performance results are only valid if the input jitter is less than the prescribed value.

² If the rate of change of the frequency of EXTAL is slow (that is, it does not jump between the minimum and maximum values in one cycle) or the frequency of the jitter is fast (that is, it does not stay at an extreme value for a long time) then the maximum allowed jitter on EXTAL can be up to 2%.

³ The timings specified in B4 and B5 are based on full strength clock.

⁴ The timing for BR output is relevant when the MPC860 is selected to work with external bus arbiter. The timing for BG output is relevant when the MPC860 is selected to work with internal bus arbiter.

⁵ The timing required for BR input is relevant when the MPC860 is selected to work with internal bus arbiter. The timing for BG input is relevant when the MPC860 is selected to work with external bus arbiter.

⁶ The D(0:31) and DP(0:3) input timings B18 and B19 refer to the rising edge of the CLKOUT in which the TA input signal is asserted.

⁷ The D(0:31) and DP(0:3) input timings B20 and B21 refer to the falling edge of the CLKOUT. This timing is valid only for read accesses controlled by chip-selects under control of the UPM in the memory controller, for data beats where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

⁸ The timing B30 refers to \overline{CS} when ACS = 00 and to $\overline{WE}(0:3)$ when CSNT = 0.

⁹ The signal UPWAIT is considered asynchronous to the CLKOUT and synchronized internally. The timings specified in B37 and B38 are specified to enable the freeze of the UPM output signals as described in Figure 18.

¹⁰ The AS signal is considered asynchronous to the CLKOUT. The timing B39 is specified in order to allow the behavior specified in Figure 21.



Figure 3 is the control timing diagram.



Figure 4 provides the timing for the external clock.



Figure 4. External Clock Timing









Figure 12. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 11)



Bus Signal Timing



Figure 15. External Bus Write Timing (GPCM Controlled—TRLX = 0 or 1, CSNT = 1)



Bus Signal Timing

Table 11 shows the debug port timing for the MPC860.

Table 11. Debug Port Timing

Num	Characteristic	All Freq	Unit	
Num	Unaracteristic		Мах	Unit
P61	DSCK cycle time	$3 \times T_{CLOCKOUT}$	_	
P62	DSCK clock pulse width	$1.25 \times T_{CLOCKOUT}$	—	—
P63	DSCK rise and fall times	0.00	3.00	ns
P64	DSDI input data setup time	8.00	—	ns
P65	DSDI data hold time	5.00	—	ns
P66	DSCK low to DSDO data valid	0.00	15.00	ns
P67	DSCK low to DSDO invalid	0.00	2.00	ns

Figure 30 provides the input timing for the debug port clock.



Figure 30. Debug Port Clock Input Timing

Figure 31 provides the timing for the debug port.



Figure 31. Debug Port Timings



11 CPM Electrical Characteristics

This section provides the AC and DC electrical specifications for the communications processor module (CPM) of the MPC860.

11.1 PIP/PIO AC Electrical Specifications

Table 14 provides the PIP/PIO AC timings as shown in Figure 39 through Figure 43.

Table 14. PIP/PIO Timing

Num	Characteristic	All Freq	Unit	
Num			Max	Onit
21	Data-in setup time to STBI low	0	_	ns
22	Data-in hold time to STBI high	2.5 – t3 ¹	_	CLK
23	STBI pulse width	1.5	_	CLK
24	STBO pulse width	1 CLK – 5 ns	_	ns
25	Data-out setup time to STBO low	2	_	CLK
26	Data-out hold time from STBO high	5	_	CLK
27	STBI low to STBO low (Rx interlock)	_	2	CLK
28	STBI low to STBO high (Tx interlock)	2	_	CLK
29	Data-in setup time to clock high	15	_	ns
30	Data-in hold time from clock high	7.5	_	ns
31	Clock low to data-out valid (CPU writes data, control, or direction)		25	ns

¹ t3 = Specification 23.



Figure 39. PIP Rx (Interlock Mode) Timing Diagram





Figure 42. PIP TX (Pulse Mode) Timing Diagram



Num	Characteristic	All Freq	Unit	
Nulli			Мах	Onit
84	L1CLK edge to L1CLKO valid (DSC = 1)	—	30.00	ns
85	L1RQ valid before falling edge of L1TSYNC ⁴	1.00	—	L1TCL K
86	L1GR setup time ²	42.00	—	ns
87	L1GR hold time	42.00	—	ns
88	L1CLK edge to L1SYNC valid (FSD = 00) CNT = 0000, BYT = 0, DSC = 0)	—	0.00	ns

Table 19. SI Timing (continued)

¹ The ratio SYNCCLK/L1RCLK must be greater than 2.5/1.

² These specs are valid for IDL mode only.

³ Where P = 1/CLKOUT. Thus, for a 25-MHz CLKO1 rate, P = 40 ns.

⁴ These strobes and TxD on the first bit of the frame become valid after L1CLK edge or L1SYNC, whichever comes later.



Figure 51. SI Receive Timing Diagram with Normal Clocking (DSC = 0)





MPC860 PowerQUICC Family Hardware Specifications, Rev. 10





11.11 SPI Slave AC Electrical Specifications

Table 25 provides the SPI slave timings as shown in Figure 67 and Figure 68.

Table 25. SPI Slave Timing

Num	Characteristic	All Freq	Unit	
		Min	Мах	Unit
170	Slave cycle time	2	—	t _{cyc}
171	Slave enable lead time	15	—	ns
172	Slave enable lag time	15	—	ns
173	Slave clock (SPICLK) high or low time	1	—	t _{cyc}
174	Slave sequential transfer delay (does not require deselect)	1	—	t _{cyc}
175	Slave data setup time (inputs)	20	—	ns
176	Slave data hold time (inputs)	20	—	ns
177	Slave access time	_	50	ns







UTOPIA AC Electrical Specifications

Figure 70 shows signal timings during UTOPIA receive operations.



Figure 71 shows signal timings during UTOPIA transmit operations.



Figure 71. UTOPIA Transmit Timing



This section provides the AC electrical specifications for the Fast Ethernet controller (FEC). Note that the timing specifications for the MII signals are independent of system clock frequency (part speed designation). Also, MII signals use TTL signal levels compatible with devices operating at either 5.0 V or 3.3 V.

13.1 MII Receive Signal Timing (MII_RXD[3:0], MII_RX_DV, MII_RX_ER, MII_RX_CLK)

The receiver functions correctly up to a MII_RX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed the MII_RX_CLK frequency - 1%.

Table 29 provides information on the MII receive signal timing.

Num	Characteristic	Min	Max	Unit
M1	MII_RXD[3:0], MII_RX_DV, MII_RX_ER to MII_RX_CLK setup	5		ns
M2	MII_RX_CLK to MII_RXD[3:0], MII_RX_DV, MII_RX_ER hold	5		ns
М3	MII_RX_CLK pulse width high	35%	65%	MII_RX_CLK period
M4	MII_RX_CLK pulse width low	35%	65%	MII_RX_CLK period

Table 29. Mll Receive Signal Timing

Figure 72 shows MII receive signal timing.



Figure 72. MII Receive Signal Timing Diagram



Mechanical Data and Ordering Information

Package Type	Freq. (MHz) / Temp. (Tj)	Package	Order Number
Ball grid array <i>(continued)</i> ZP suffix—leaded ZQ suffix—leaded VR suffix—lead-free	80 0° to 95°C	ZP/ZQ ¹	MPC855TZQ80D4 MPC860DEZQ80D4 MPC860DTZQ80D4 MPC860ENZQ80D4 MPC860SRZQ80D4 MPC860TZQ80D4 MPC860DPZQ80D4 MPC860PZQ80D4
		Tape and Reel	MPC860PZQ80D4R2 MPC860PVR80D4R2
		VR	MPC855TVR80D4 MPC860DEVR80D4 MPC860DPVR80D4 MPC860ENVR80D4 MPC860PVR80D4 MPC860SRVR80D4 MPC860SRVR80D4
Ball grid array (CZP suffix) CZP suffix—leaded CZQ suffix—leaded CVR suffix—lead-free	50 −40° to 95°C	ZP/ZQ ¹	MPC855TCZQ50D4 MPC855TCVR50D4 MPC860DECZQ50D4 MPC860DTCZQ50D4 MPC860ENCZQ50D4 MPC860SRCZQ50D4 MPC860TCZQ50D4 MPC860DPCZQ50D4 MPC860PCZQ50D4
		Tape and Reel	MPC855TCZQ50D4R2 MC860ENCVR50D4R2
		CVR	MPC860DECVR50D4 MPC860DTCVR50D4 MPC860ENCVR50D4 MPC860PCVR50D4 MPC860SRCVR50D4 MPC860TCVR50D4
	66 –40° to 95°C	ZP/ZQ ¹	MPC855TCZQ66D4 MPC855TCVR66D4 MPC860ENCZQ66D4 MPC860SRCZQ66D4 MPC860TCZQ66D4 MPC860DPCZQ66D4 MPC860PCZQ66D4
		CVR	MPC860DTCVR66D4 MPC860ENCVR66D4 MPC860PCVR66D4 MPC860SRCVR66D4 MPC860TCVR66D4

Table 34. MPC860 Family Package/Frequency Availability (continued)

¹ The ZP package is no longer recommended for use. The ZQ package replaces the ZP package.