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### Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

### Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

#### Details

Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	80MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (4)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 95°C (TA)
Security Features	-
Package / Case	357-BBGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc860srvr80d4">https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc860srvr80d4</a>

# 1 Overview

The MPC860 power quad integrated communications controller (PowerQUICC™) is a versatile one-chip integrated microprocessor and peripheral combination designed for a variety of controller applications. It particularly excels in communications and networking systems. The PowerQUICC unit is referred to as the MPC860 in this hardware specification.

The MPC860 implements Power Architecture™ technology and contains a superset of Freescale's MC68360 quad integrated communications controller (QUICC), referred to here as the QUICC, RISC communications processor module (CPM). The CPU on the MPC860 is a 32-bit core built on Power Architecture technology that incorporates memory management units (MMUs) and instruction and data caches. The CPM from the MC68360 QUICC has been enhanced by the addition of the inter-integrated controller (I<sup>2</sup>C) channel. The memory controller has been enhanced, enabling the MPC860 to support any type of memory, including high-performance memories and new types of DRAMs. A PCMCIA socket controller supports up to two sockets. A real-time clock has also been integrated.

Table 1 shows the functionality supported by the MPC860 family.

**Table 1. MPC860 Family Functionality**

Part	Cache (Kbytes)		Ethernet		ATM	SCC	Reference <sup>1</sup>
	Instruction Cache	Data Cache	10T	10/100			
MPC860DE	4	4	Up to 2	—	—	2	1
MPC860DT	4	4	Up to 2	1	Yes	2	1
MPC860DP	16	8	Up to 2	1	Yes	2	1
MPC860EN	4	4	Up to 4	—	—	4	1
MPC860SR	4	4	Up to 4	—	Yes	4	1
MPC860T	4	4	Up to 4	1	Yes	4	1
MPC860P	16	8	Up to 4	1	Yes	4	1
MPC855T	4	4	1	1	Yes	1	2

<sup>1</sup> Supporting documentation for these devices refers to the following:

1. MPC860 PowerQUICC Family User's Manual (MPC860UM, Rev. 3)
2. MPC855T User's Manual (MPC855TUM, Rev. 1)

- System integration unit (SIU)
  - Bus monitor
  - Software watchdog
  - Periodic interrupt timer (PIT)
  - Low-power stop mode
  - Clock synthesizer
  - Decrementer, time base, and real-time clock (RTC)
  - Reset controller
  - IEEE 1149.1™ Std. test access port (JTAG)
- Interrupts
  - Seven external interrupt request (IRQ) lines
  - 12 port pins with interrupt capability
  - 23 internal interrupt sources
  - Programmable priority between SCCs
  - Programmable highest priority request
- 10/100 Mbps Ethernet support, fully compliant with the IEEE 802.3u® Standard (not available when using ATM over UTOPIA interface)
- ATM support compliant with ATM forum UNI 4.0 specification
  - Cell processing up to 50–70 Mbps at 50-MHz system clock
  - Cell multiplexing/demultiplexing
  - Support of AAL5 and AAL0 protocols on a per-VC basis. AAL0 support enables OAM and software implementation of other protocols.
  - ATM pace control (APC) scheduler, providing direct support for constant bit rate (CBR) and unspecified bit rate (UBR) and providing control mechanisms enabling software support of available bit rate (ABR)
  - Physical interface support for UTOPIA (10/100-Mbps is not supported with this interface) and byte-aligned serial (for example, T1/E1/ADSL)
  - UTOPIA-mode ATM supports level-1 master with cell-level handshake, multi-PHY (up to four physical layer devices), connection to 25-, 51-, or 155-Mbps framers, and UTOPIA/system clock ratios of 1/2 or 1/3.
  - Serial-mode ATM connection supports transmission convergence (TC) function for T1/E1/ADSL lines, cell delineation, cell payload scrambling/descrambling, automatic idle/unassigned cell insertion/stripping, header error control (HEC) generation, checking, and statistics.
- Communications processor module (CPM)
  - RISC communications processor (CP)
  - Communication-specific commands (for example, GRACEFUL STOP TRANSMIT, ENTER HUNT MODE, and RESTART TRANSMIT)
  - Supports continuous mode transmission and reception on all serial channels

## Features

- Allows dynamic changes
- Can be internally connected to six serial channels (four SCCs and two SMCs)
- Parallel interface port (PIP)
  - Centronics interface support
  - Supports fast connection between compatible ports on the MPC860 or the MC68360
- PCMCIA interface
  - Master (socket) interface, release 2.1 compliant
  - Supports two independent PCMCIA sockets
  - Supports eight memory or I/O windows
- Low power support
  - Full on—all units fully powered
  - Doze—core functional units disabled except time base decrementer, PLL, memory controller, RTC, and CPM in low-power standby
  - Sleep—all units disabled except RTC and PIT, PLL active for fast wake up
  - Deep sleep—all units disabled including PLL except RTC and PIT
  - Power down mode—all units powered down except PLL, RTC, PIT, time base, and decrementer
- Debug interface
  - Eight comparators: four operate on instruction address, two operate on data address, and two operate on data
  - Supports conditions: = ≠ < >
  - Each watchpoint can generate a break-point internally.
- 3.3-V operation with 5-V TTL compatibility except EXTAL and EXTCLK
- 357-pin ball grid array (BGA) package

Table 4 shows the thermal characteristics for the MPC860.

**Table 4. MPC860 Thermal Resistance Data**

Rating	Environment		Symbol	ZP MPC860P	ZQ / VR MPC860P	Unit
Mold Compound Thickness				0.85	1.15	mm
Junction-to-ambient <sup>1</sup>	Natural convection	Single-layer board (1s)	R <sub>θJA</sub> <sup>2</sup>	34	34	°C/W
		Four-layer board (2s2p)	R <sub>θJMA</sub> <sup>3</sup>	22	22	
	Airflow (200 ft/min)	Single-layer board (1s)	R <sub>θJMA</sub> <sup>3</sup>	27	27	
		Four-layer board (2s2p)	R <sub>θJMA</sub> <sup>3</sup>	18	18	
Junction-to-board <sup>4</sup>			R <sub>θJB</sub>	14	13	
Junction-to-case <sup>5</sup>			R <sub>θJC</sub>	6	8	
Junction-to-package top <sup>6</sup>	Natural convection		Ψ <sub>JT</sub>	2	2	

<sup>1</sup> Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.

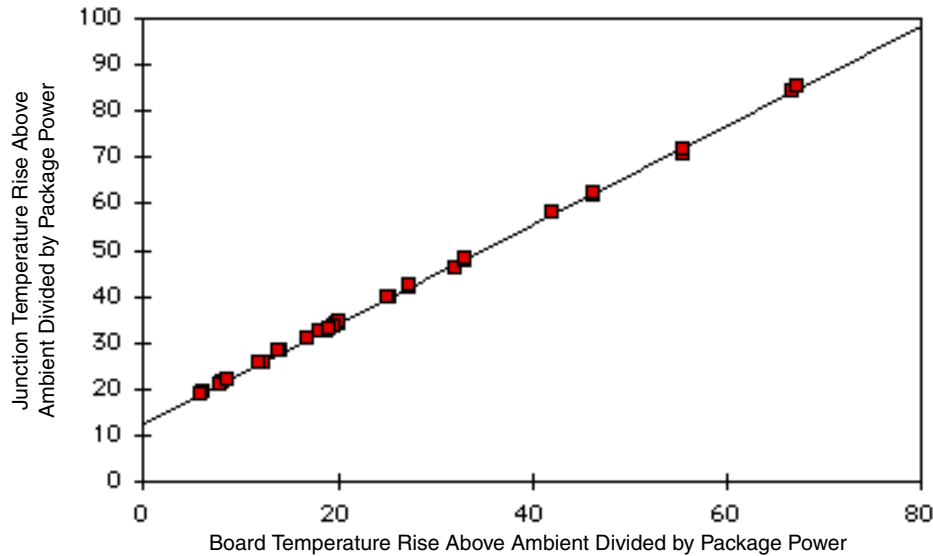
<sup>2</sup> Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.

<sup>3</sup> Per JEDEC JESD51-6 with the board horizontal.

<sup>4</sup> Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

<sup>5</sup> Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature. For exposed pad packages where the pad would be expected to be soldered, junction-to-case thermal resistance is a simulated value from the junction to the exposed pad without contact resistance.

<sup>6</sup> Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2.



**Figure 2. Effect of Board Temperature Rise on Thermal Behavior**

If the board temperature is known, an estimate of the junction temperature in the environment can be made using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

$R_{\theta JB}$  = junction-to-board thermal resistance ( $^{\circ}\text{C}/\text{W}$ )

$T_B$  = board temperature ( $^{\circ}\text{C}$ )

$P_D$  = power dissipation in package

If the board temperature is known and the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. For this method to work, the board and board mounting must be similar to the test board used to determine the junction-to-board thermal resistance, namely a 2s2p (board with a power and a ground plane) and by attaching the thermal balls to the ground plane.

## 7.4 Estimation Using Simulation

When the board temperature is not known, a thermal simulation of the application is needed. The simple two-resistor model can be used with the thermal simulation of the application [2], or a more accurate and complex model of the package can be used in the thermal simulation.

## 7.5 Experimental Determination

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter ( $\Psi_{JT}$ ) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

**Table 7. Bus Operation Timings (continued)**

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B35	A(0:31), BADDR(28:30) to $\overline{CS}$ valid—as requested by control bit BST4 in the corresponding word in UPM	5.58	—	4.25	—	3.00	—	1.79	—	ns
B35a	A(0:31), BADDR(28:30), and D(0:31) to $\overline{BS}$ valid—as requested by control bit BST1 in the corresponding word in UPM	13.15	—	10.50	—	8.00	—	5.58	—	ns
B35b	A(0:31), BADDR(28:30), and D(0:31) to $\overline{BS}$ valid—as requested by control bit BST2 in the corresponding word in UPM	20.73	—	16.75	—	13.00	—	9.36	—	ns
B36	A(0:31), BADDR(28:30), and D(0:31) to $\overline{GPL}$ valid—as requested by control bit GxT4 in the corresponding word in UPM	5.58	—	4.25	—	3.00	—	1.79	—	ns
B37	UPWAIT valid to CLKOUT falling edge <sup>9</sup>	6.00	—	6.00	—	6.00	—	6.00	—	ns
B38	CLKOUT falling edge to UPGATE valid <sup>9</sup>	1.00	—	1.00	—	1.00	—	1.00	—	ns
B39	$\overline{AS}$ valid to CLKOUT rising edge <sup>10</sup>	7.00	—	7.00	—	7.00	—	7.00	—	ns
B40	A(0:31), TSIZ(0:1), RD/ $\overline{WR}$ , $\overline{BURST}$ , valid to CLKOUT rising edge	7.00	—	7.00	—	7.00	—	7.00	—	ns
B41	$\overline{TS}$ valid to CLKOUT rising edge (setup time)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B42	CLKOUT rising edge to $\overline{TS}$ valid (hold time)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B43	$\overline{AS}$ negation to memory controller signals negation	—	TBD	—	TBD	—	TBD	—	TBD	ns

<sup>1</sup> Phase and frequency jitter performance results are only valid if the input jitter is less than the prescribed value.

<sup>2</sup> If the rate of change of the frequency of EXTAL is slow (that is, it does not jump between the minimum and maximum values in one cycle) or the frequency of the jitter is fast (that is, it does not stay at an extreme value for a long time) then the maximum allowed jitter on EXTAL can be up to 2%.

<sup>3</sup> The timings specified in B4 and B5 are based on full strength clock.

<sup>4</sup> The timing for  $\overline{BR}$  output is relevant when the MPC860 is selected to work with external bus arbiter. The timing for  $\overline{BG}$  output is relevant when the MPC860 is selected to work with internal bus arbiter.

<sup>5</sup> The timing required for  $\overline{BR}$  input is relevant when the MPC860 is selected to work with internal bus arbiter. The timing for  $\overline{BG}$  input is relevant when the MPC860 is selected to work with external bus arbiter.

<sup>6</sup> The D(0:31) and DP(0:3) input timings B18 and B19 refer to the rising edge of the CLKOUT in which the  $\overline{TA}$  input signal is asserted.

<sup>7</sup> The D(0:31) and DP(0:3) input timings B20 and B21 refer to the falling edge of the CLKOUT. This timing is valid only for read accesses controlled by chip-selects under control of the UPM in the memory controller, for data beats where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

<sup>8</sup> The timing B30 refers to  $\overline{CS}$  when ACS = 00 and to  $\overline{WE}$ (0:3) when CSNT = 0.

<sup>9</sup> The signal UPGATE is considered asynchronous to the CLKOUT and synchronized internally. The timings specified in B37 and B38 are specified to enable the freeze of the UPM output signals as described in [Figure 18](#).

<sup>10</sup> The  $\overline{AS}$  signal is considered asynchronous to the CLKOUT. The timing B39 is specified in order to allow the behavior specified in [Figure 21](#).

Figure 5 provides the timing for the synchronous output signals.

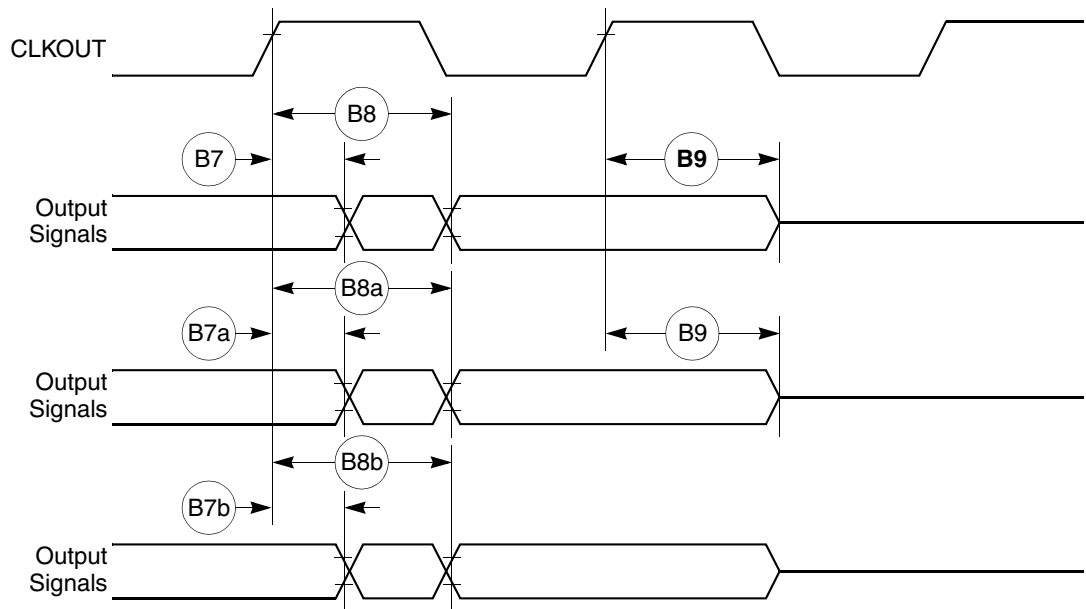


Figure 5. Synchronous Output Signals Timing

Figure 6 provides the timing for the synchronous active pull-up and open-drain output signals.

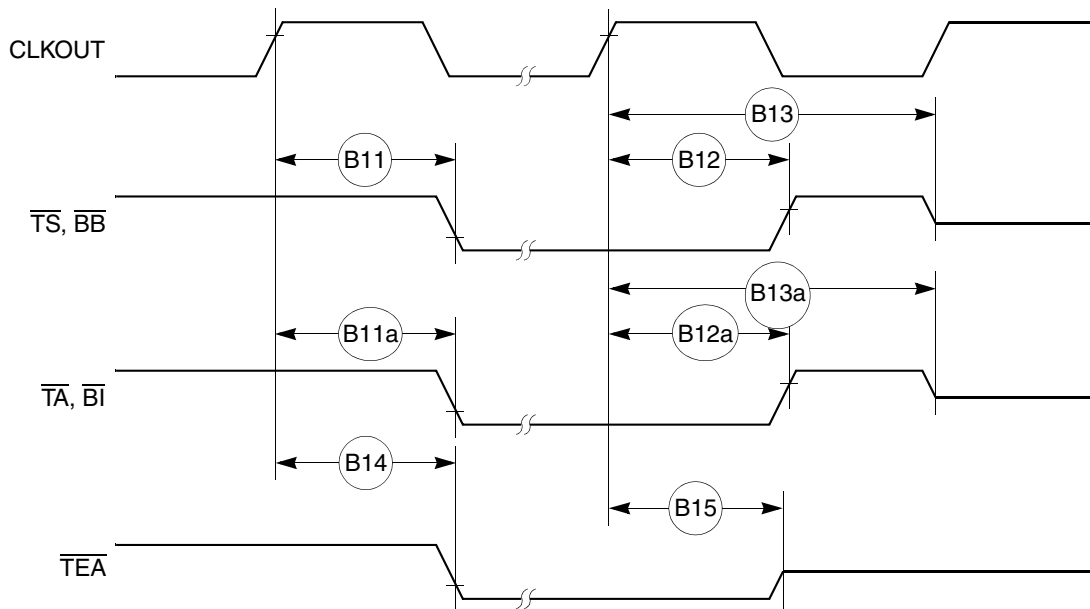


Figure 6. Synchronous Active Pull-Up Resistor and Open-Drain Outputs Signals Timing



Figure 9 provides the timing for the input data controlled by the UPM for data beats where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

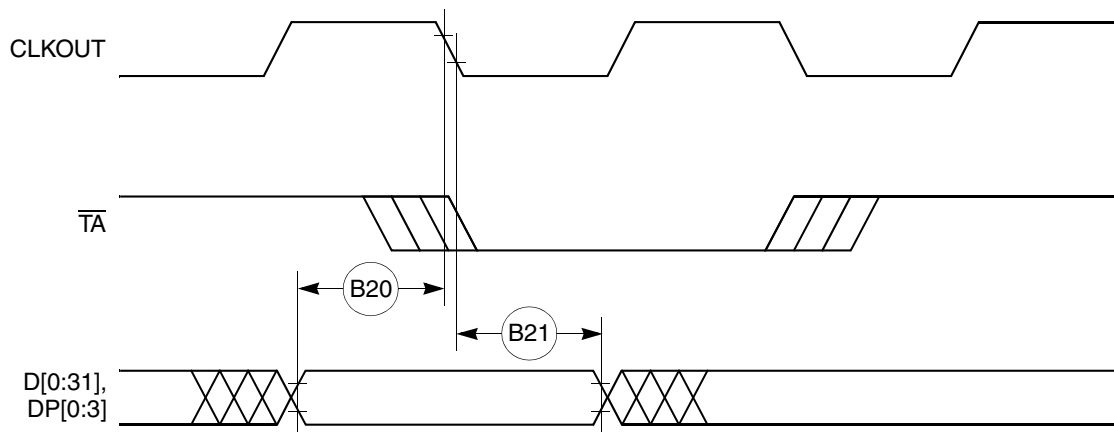


Figure 9. Input Data Timing when Controlled by UPM in the Memory Controller and DLT3 = 1

Figure 10 through Figure 13 provide the timing for the external bus read controlled by various GPCM factors.

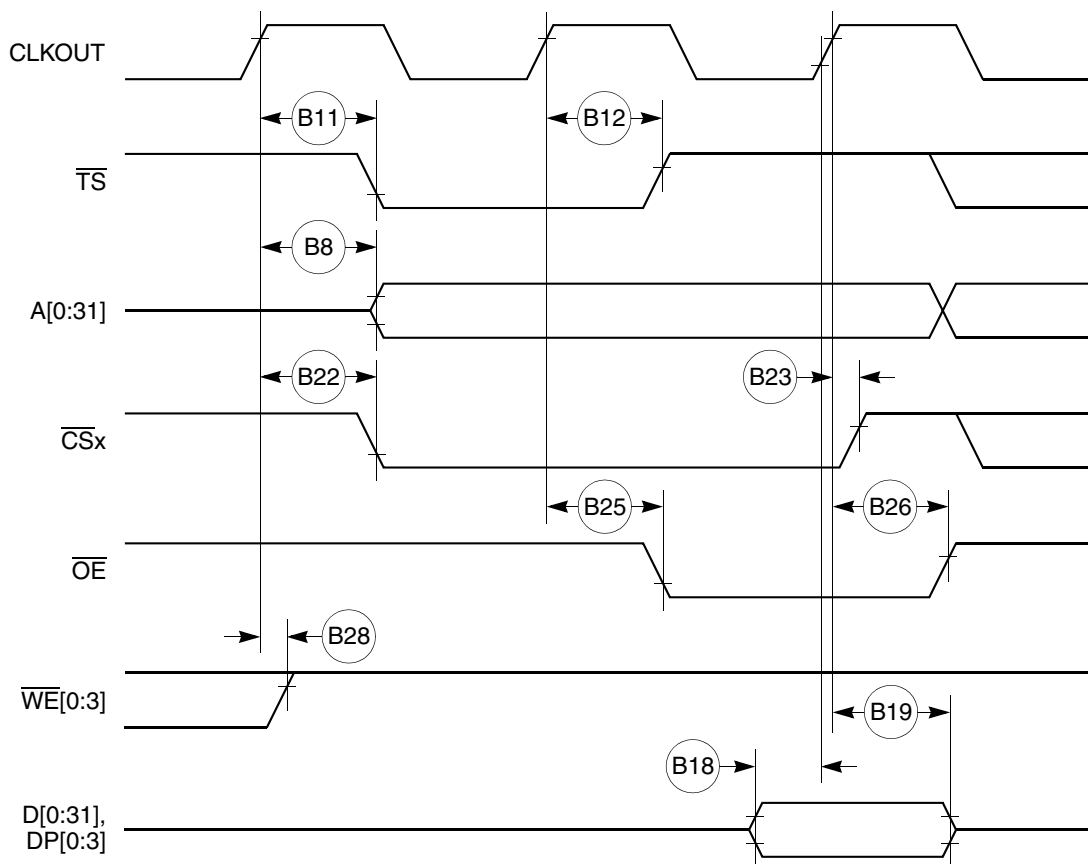


Figure 10. External Bus Read Timing (GPCM Controlled—ACS = 00)

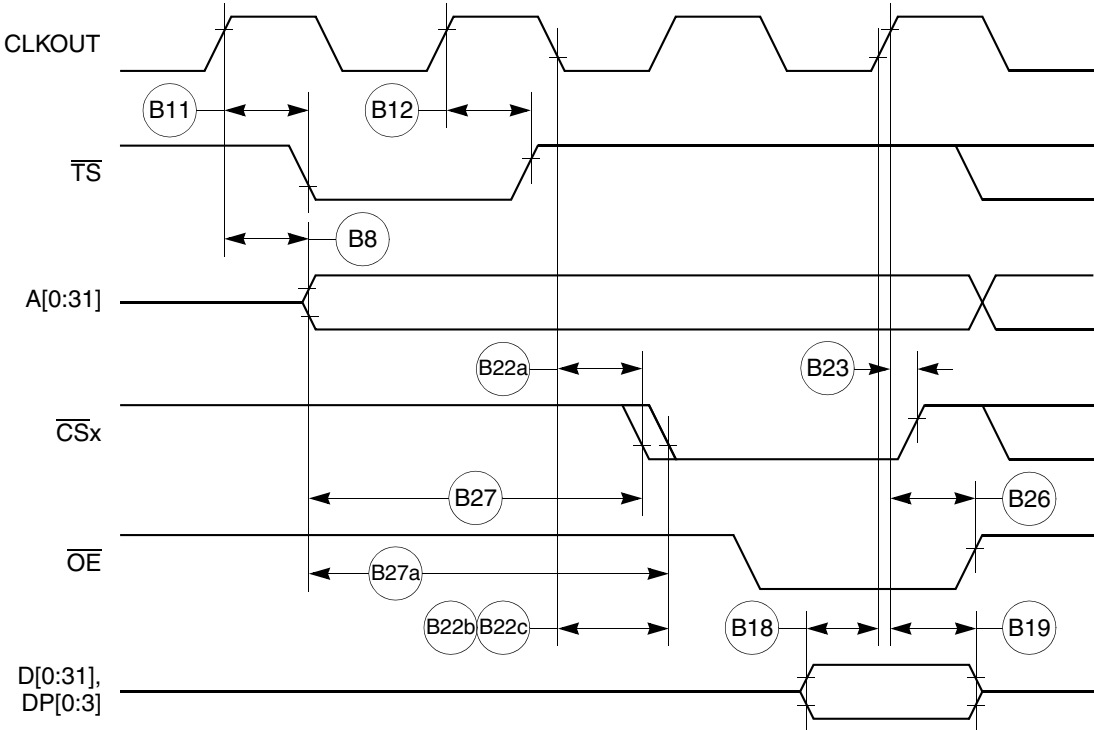


Figure 13. External Bus Read Timing (GPCM Controlled—TRLX = 0 or 1, ACS = 10, ACS = 11)

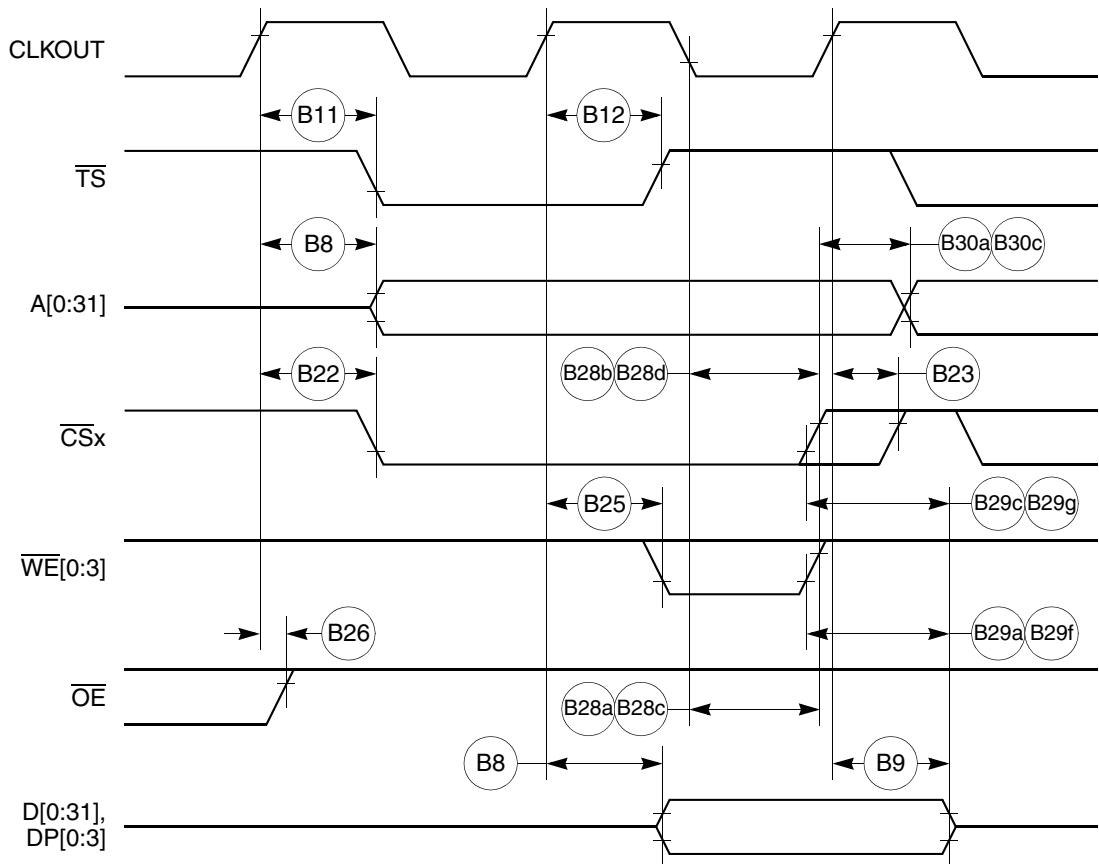


Figure 15. External Bus Write Timing (GPCM Controlled—TRLX = 0 or 1, CSNT = 1)

Figure 17 provides the timing for the external bus controlled by the UPM.

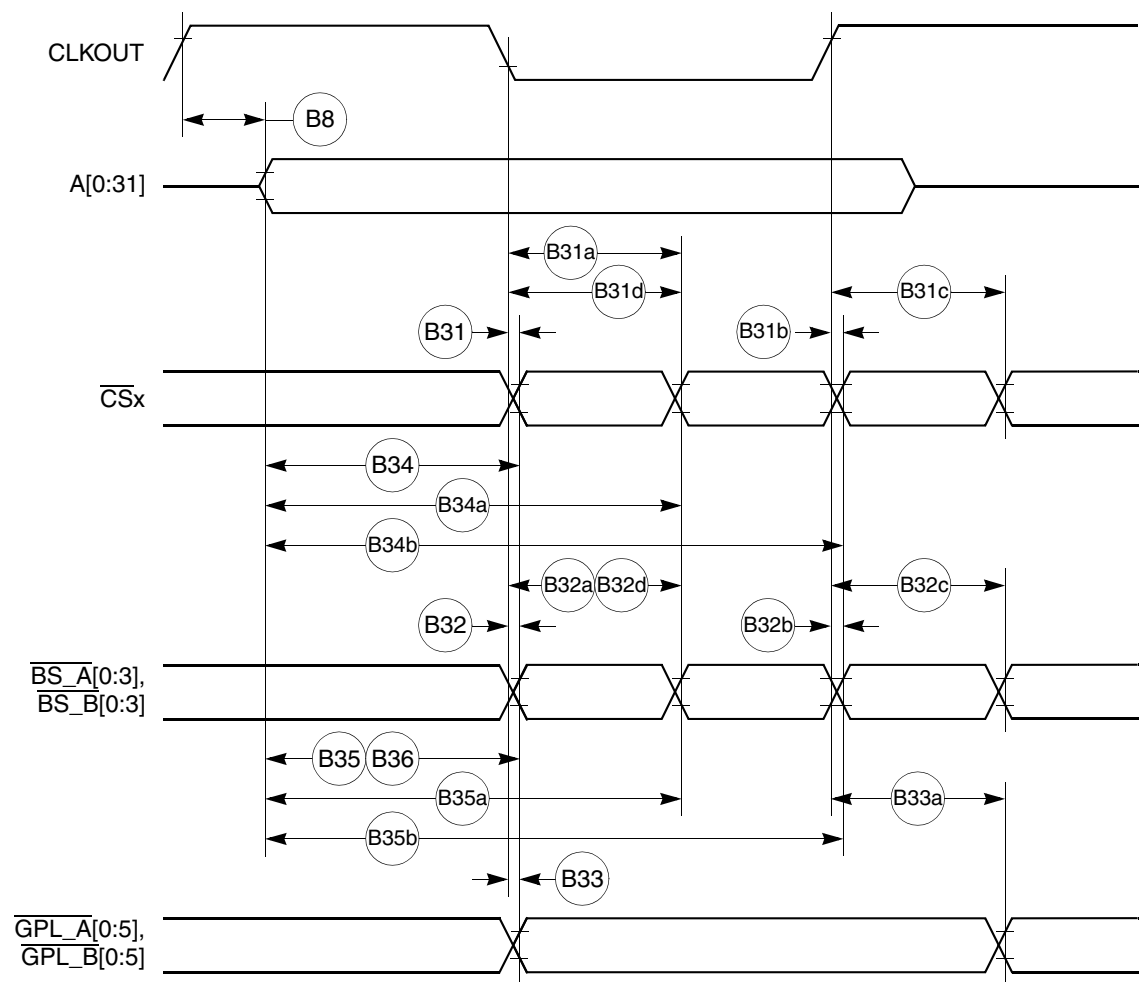


Figure 17. External Bus Timing (UPM Controlled Signals)

Table 9 shows the PCMCIA timing for the MPC860.

**Table 9. PCMCIA Timing**

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
P44	A(0:31), $\overline{\text{REG}}$ valid to PCMCIA Strobe asserted <sup>1</sup>	20.73	—	16.75	—	13.00	—	9.36	—	ns
P45	A(0:31), $\overline{\text{REG}}$ valid to ALE negation <sup>1</sup>	28.30	—	23.00	—	18.00	—	13.15	—	ns
P46	CLKOUT to $\overline{\text{REG}}$ valid	7.58	15.58	6.25	14.25	5.00	13.00	3.79	11.84	ns
P47	CLKOUT to $\overline{\text{REG}}$ invalid	8.58	—	7.25	—	6.00	—	4.84	—	ns
P48	CLKOUT to $\overline{\text{CE1}}$ , $\overline{\text{CE2}}$ asserted	7.58	15.58	6.25	14.25	5.00	13.00	3.79	11.84	ns
P49	CLKOUT to $\overline{\text{CE1}}$ , $\overline{\text{CE2}}$ negated	7.58	15.58	6.25	14.25	5.00	13.00	3.79	11.84	ns
P50	CLKOUT to $\overline{\text{PCOE}}$ , $\overline{\text{IORD}}$ , $\overline{\text{PCWE}}$ , $\overline{\text{IOWR}}$ assert time	—	11.00		11.00	—	11.00	—	11.00	ns
P51	CLKOUT to $\overline{\text{PCOE}}$ , $\overline{\text{IORD}}$ , $\overline{\text{PCWE}}$ , $\overline{\text{IOWR}}$ negate time	2.00	11.00	2.00	11.00	2.00	11.00	2.00	11.00	ns
P52	CLKOUT to ALE assert time	7.58	15.58	6.25	14.25	5.00	13.00	3.79	10.04	ns
P53	CLKOUT to ALE negate time	—	15.58		14.25	—	13.00	—	11.84	ns
P54	$\overline{\text{PCWE}}$ , $\overline{\text{IOWR}}$ negated to D(0:31) invalid <sup>1</sup>	5.58	—	4.25	—	3.00	—	1.79	—	ns
P55	$\overline{\text{WAITA}}$ and $\overline{\text{WAITB}}$ valid to CLKOUT rising edge <sup>1</sup>	8.00	—	8.00	—	8.00	—	8.00	—	ns
P56	CLKOUT rising edge to $\overline{\text{WAITA}}$ and $\overline{\text{WAITB}}$ invalid <sup>1</sup>	2.00	—	2.00	—	2.00	—	2.00	—	ns

<sup>1</sup> PSST = 1. Otherwise add PSST times cycle time.

PSHT = 0. Otherwise add PSHT times cycle time.

These synchronous timings define when the  $\overline{\text{WAITx}}$  signals are detected in order to freeze (or relieve) the PCMCIA current cycle. The  $\overline{\text{WAITx}}$  assertion will be effective only if it is detected 2 cycles before the PSL timer expiration. See Chapter 16, “PCMCIA Interface,” in the *MPC860 PowerQUICC™ Family User's Manual*.

Figure 25 provides the PCMCIA access cycle timing for the external bus read.

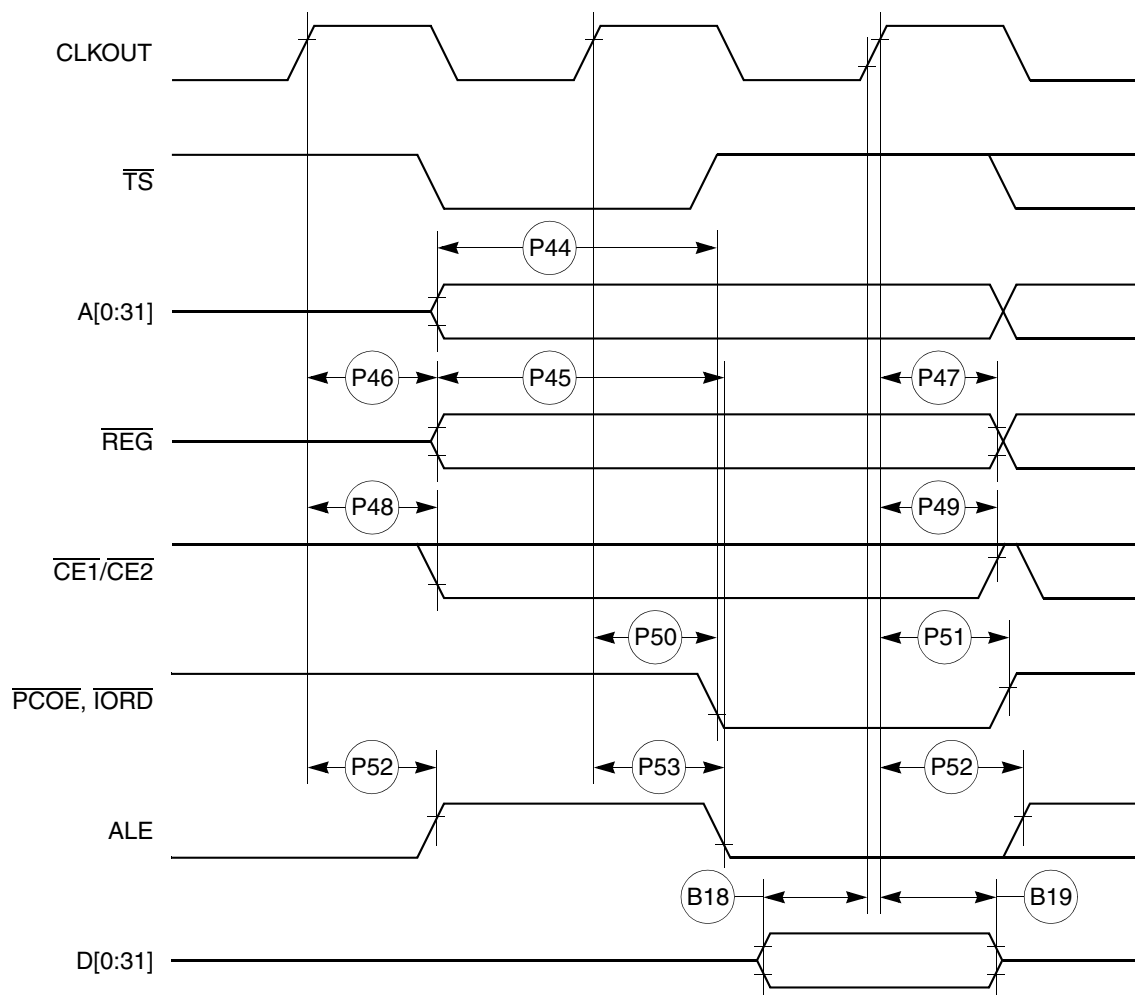


Figure 25. PCMCIA Access Cycle Timing External Bus Read

Table 12 shows the reset timing for the MPC860.

**Table 12. Reset Timing**

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
R69	CLKOUT to $\overline{\text{HRESET}}$ high impedance	—	20.00	—	20.00	—	20.00	—	20.00	ns
R70	CLKOUT to $\overline{\text{SRESET}}$ high impedance	—	20.00	—	20.00	—	20.00	—	20.00	ns
R71	$\overline{\text{RSTCONF}}$ pulse width	515.15	—	425.00	—	340.00	—	257.58	—	ns
R72	—	—	—	—	—	—	—	—	—	
R73	Configuration data to $\overline{\text{HRESET}}$ rising edge setup time	504.55	—	425.00	—	350.00	—	277.27	—	ns
R74	Configuration data to $\overline{\text{RSTCONF}}$ rising edge setup time	350.00	—	350.00	—	350.00	—	350.00	—	ns
R75	Configuration data hold time after $\overline{\text{RSTCONF}}$ negation	0.00	—	0.00	—	0.00	—	0.00	—	ns
R76	Configuration data hold time after $\overline{\text{HRESET}}$ negation	0.00	—	0.00	—	0.00	—	0.00	—	ns
R77	$\overline{\text{HRESET}}$ and $\overline{\text{RSTCONF}}$ asserted to data out drive	—	25.00	—	25.00	—	25.00	—	25.00	ns
R78	$\overline{\text{RSTCONF}}$ negated to data out high impedance	—	25.00	—	25.00	—	25.00	—	25.00	ns
R79	CLKOUT of last rising edge before chip three-state $\overline{\text{HRESET}}$ to data out high impedance	—	25.00	—	25.00	—	25.00	—	25.00	ns
R80	DSDI, DSCK setup	90.91	—	75.00	—	60.00	—	45.45	—	ns
R81	DSDI, DSCK hold time	0.00	—	0.00	—	0.00	—	0.00	—	ns
R82	$\overline{\text{SRESET}}$ negated to CLKOUT rising edge for DSDI and DSCK sample	242.42	—	200.00	—	160.00	—	121.21	—	ns

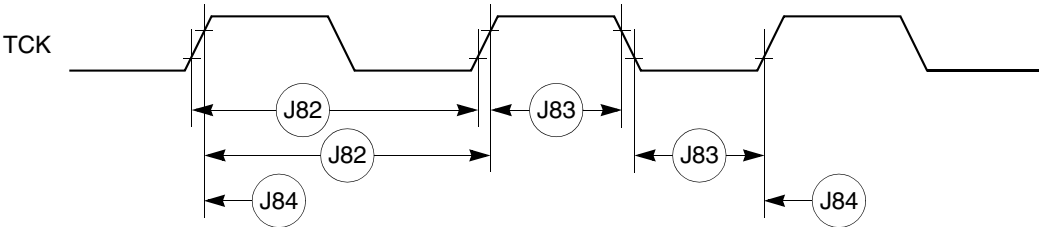


Figure 35. JTAG Test Clock Input Timing

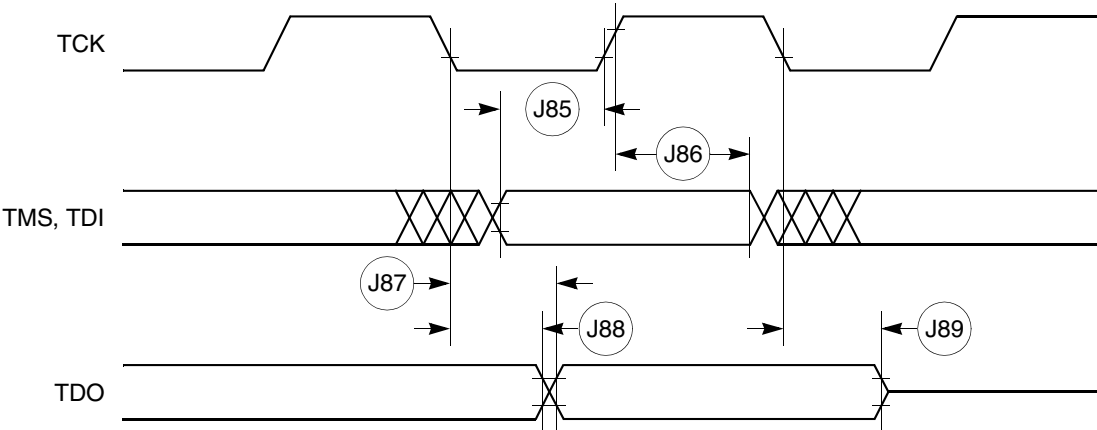


Figure 36. JTAG Test Access Port Timing Diagram

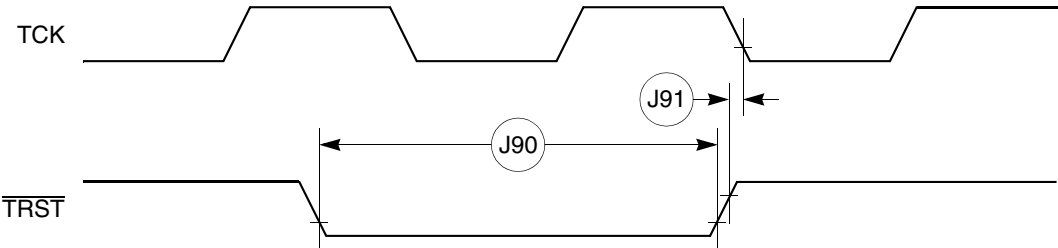


Figure 37. JTAG  $\overline{\text{TRST}}$  Timing Diagram

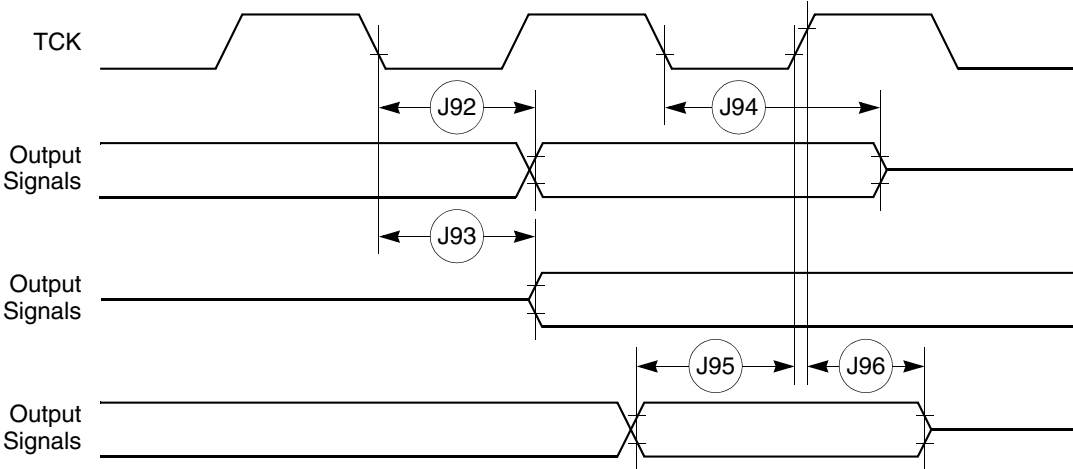


Figure 38. Boundary Scan (JTAG) Timing Diagram



## 11.4 Baud Rate Generator AC Electrical Specifications

Table 17 provides the baud rate generator timings as shown in Figure 49.

Table 17. Baud Rate Generator Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
50	BRGO rise and fall time	—	10	ns
51	BRGO duty cycle	40	60	%
52	BRGO cycle	40	—	ns

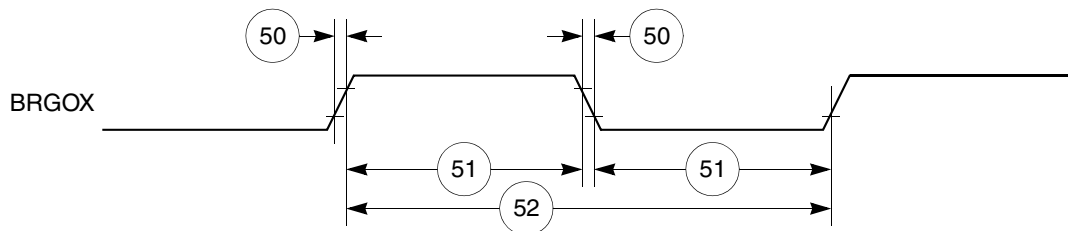


Figure 49. Baud Rate Generator Timing Diagram

## 11.5 Timer AC Electrical Specifications

Table 18 provides the general-purpose timer timings as shown in Figure 50.

Table 18. Timer Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
61	TIN/TGATE rise and fall time	10	—	ns
62	TIN/TGATE low time	1	—	CLK
63	TIN/TGATE high time	2	—	CLK
64	TIN/TGATE cycle time	3	—	CLK
65	CLKO low to TOUT valid	3	25	ns

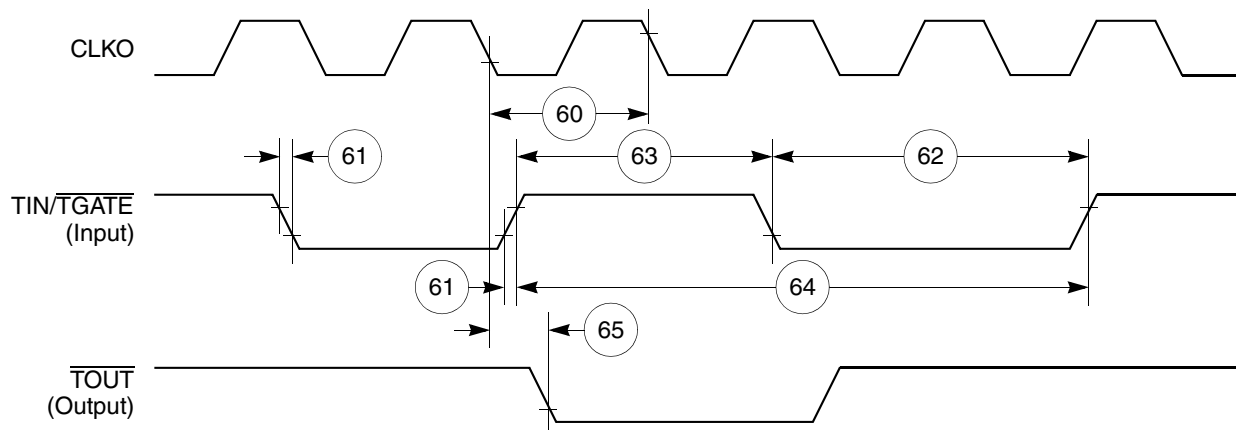


Figure 50. CPM General-Purpose Timers Timing Diagram

## 11.6 Serial Interface AC Electrical Specifications

Table 19 provides the serial interface timings as shown in Figure 51 through Figure 55.

Table 19. SI Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
70	L1RCLK, L1TCLK frequency (DSC = 0) <sup>1, 2</sup>	—	SYNCCCLK/2.5	MHz
71	L1RCLK, L1TCLK width low (DSC = 0) <sup>2</sup>	P + 10	—	ns
71a	L1RCLK, L1TCLK width high (DSC = 0) <sup>3</sup>	P + 10	—	ns
72	L1TXD, L1ST(1–4), $\overline{\text{L1RQ}}$ , L1CLKO rise/fall time	—	15.00	ns
73	L1RSYNC, L1TSYNC valid to L1CLK edge (SYNC setup time)	20.00	—	ns
74	L1CLK edge to L1RSYNC, L1TSYNC, invalid (SYNC hold time)	35.00	—	ns
75	L1RSYNC, L1TSYNC rise/fall time	—	15.00	ns
76	L1RXD valid to L1CLK edge (L1RXD setup time)	17.00	—	ns
77	L1CLK edge to L1RXD invalid (L1RXD hold time)	13.00	—	ns
78	L1CLK edge to L1ST(1–4) valid <sup>4</sup>	10.00	45.00	ns
78A	L1SYNC valid to L1ST(1–4) valid	10.00	45.00	ns
79	L1CLK edge to L1ST(1–4) invalid	10.00	45.00	ns
80	L1CLK edge to L1TXD valid	10.00	55.00	ns
80A	L1TSYNC valid to L1TXD valid <sup>4</sup>	10.00	55.00	ns
81	L1CLK edge to L1TXD high impedance	0.00	42.00	ns
82	L1RCLK, L1TCLK frequency (DSC = 1)	—	16.00 or SYNCCCLK/2	MHz
83	L1RCLK, L1TCLK width low (DSC = 1)	P + 10	—	ns
83a	L1RCLK, L1TCLK width high (DSC = 1) <sup>3</sup>	P + 10	—	ns

## 11.7 SCC in NMSI Mode Electrical Specifications

Table 20 provides the NMSI external clock timing.

**Table 20. NMSI External Clock Timing**

Num	Characteristic	All Frequencies		Unit
		Min	Max	
100	RCLK1 and TCLK1 width high <sup>1</sup>	1/SYNCCLK	—	ns
101	RCLK1 and TCLK1 width low	1/SYNCCLK + 5	—	ns
102	RCLK1 and TCLK1 rise/fall time	—	15.00	ns
103	TXD1 active delay (from TCLK1 falling edge)	0.00	50.00	ns
104	$\overline{\text{RTS1}}$ active/inactive delay (from TCLK1 falling edge)	0.00	50.00	ns
105	$\overline{\text{CTS1}}$ setup time to TCLK1 rising edge	5.00	—	ns
106	RXD1 setup time to RCLK1 rising edge	5.00	—	ns
107	RXD1 hold time from RCLK1 rising edge <sup>2</sup>	5.00	—	ns
108	$\overline{\text{CD1}}$ setup Time to RCLK1 rising edge	5.00	—	ns

<sup>1</sup> The ratios SYNCCLK/RCLK1 and SYNCCLK/TCLK1 must be greater than or equal to 2.25/1.

<sup>2</sup> Also applies to  $\overline{\text{CD}}$  and  $\overline{\text{CTS}}$  hold time when they are used as external sync signals.

Table 21 provides the NMSI internal clock timing.

**Table 21. NMSI Internal Clock Timing**

Num	Characteristic	All Frequencies		Unit
		Min	Max	
100	RCLK1 and TCLK1 frequency <sup>1</sup>	0.00	SYNCCLK/3	MHz
102	RCLK1 and TCLK1 rise/fall time	—	—	ns
103	TXD1 active delay (from TCLK1 falling edge)	0.00	30.00	ns
104	$\overline{\text{RTS1}}$ active/inactive delay (from TCLK1 falling edge)	0.00	30.00	ns
105	$\overline{\text{CTS1}}$ setup time to TCLK1 rising edge	40.00	—	ns
106	RXD1 setup time to RCLK1 rising edge	40.00	—	ns
107	RXD1 hold time from RCLK1 rising edge <sup>2</sup>	0.00	—	ns
108	$\overline{\text{CD1}}$ setup time to RCLK1 rising edge	40.00	—	ns

<sup>1</sup> The ratios SYNCCLK/RCLK1 and SYNCCLK/TCLK1 must be greater than or equal to 3/1.

<sup>2</sup> Also applies to  $\overline{\text{CD}}$  and  $\overline{\text{CTS}}$  hold time when they are used as external sync signals.

Figure 70 shows signal timings during UTOPIA receive operations.

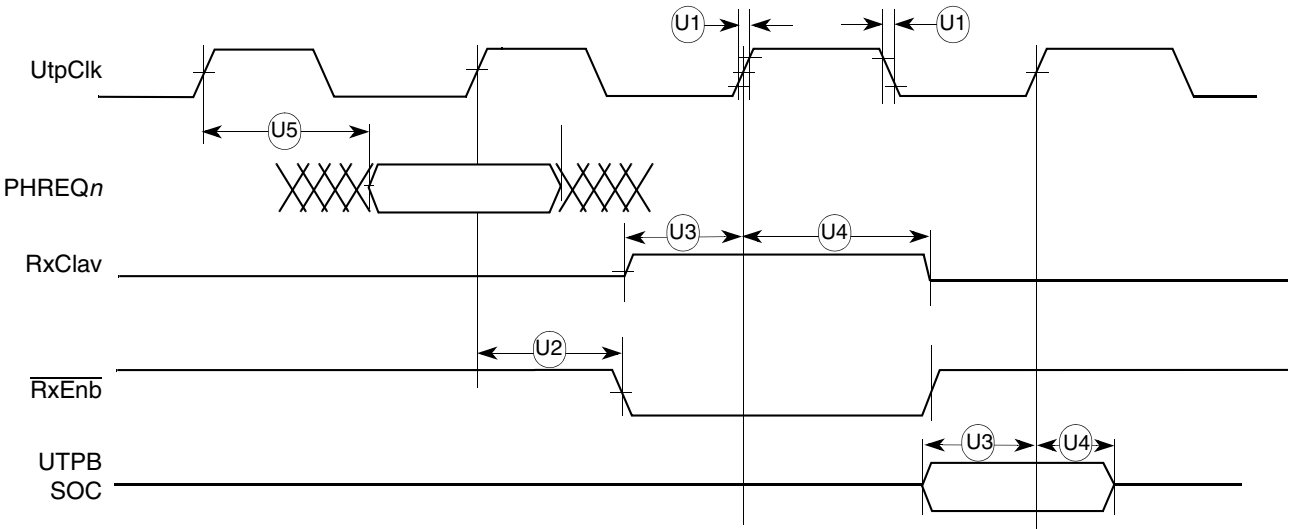


Figure 70. UTOPIA Receive Timing

Figure 71 shows signal timings during UTOPIA transmit operations.

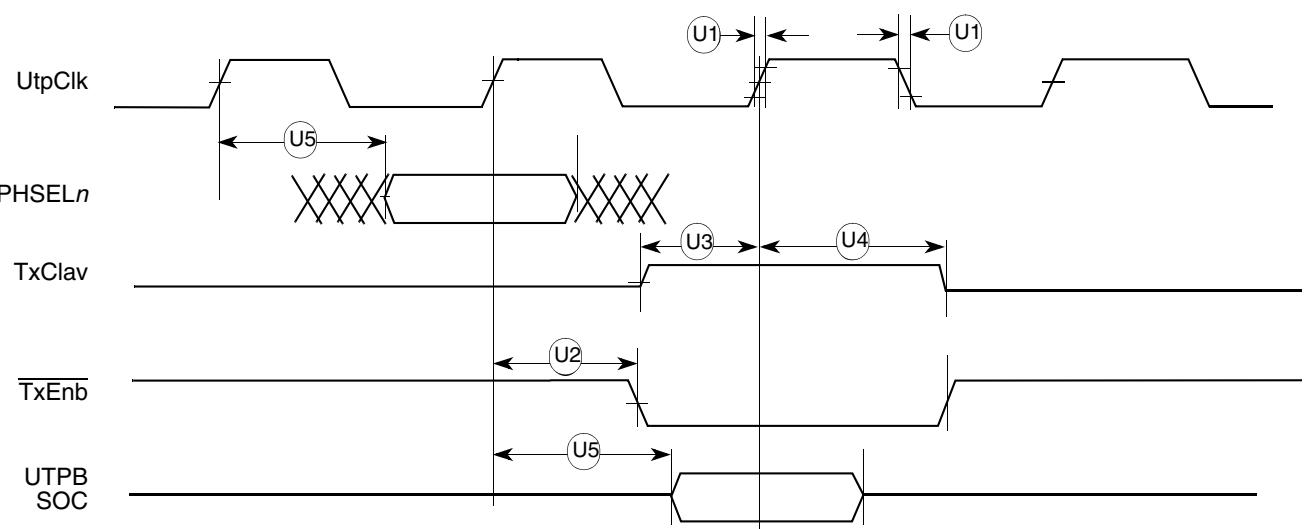


Figure 71. UTOPIA Transmit Timing

# 15 Document Revision History

Table 35 lists significant changes between revisions of this hardware specification.

**Table 35. Document Revision History**

Revision	Date	Changes
10	09/2015	In Table 34, moved MPC855TCVR50D4 and MPC855TCVR66D4 under the extended temperature (–40° to 95°C) and removed MC860ENCVR50D4R2 from the normal temperature Tape and Reel.
9	10/2011	Updated orderable part numbers in Table 34, “MPC860 Family Package/Frequency Availability.”
8	08/2007	<ul style="list-style-type: none"> <li>Updated template.</li> <li>On page 1, added a second paragraph.</li> <li>After Table 2, inserted a new figure showing the undershoot/overshoot voltage (Figure 1) and renumbered the rest of the figures.</li> <li>In Figure 3, changed all reference voltage measurement points from 0.2 and 0.8 V to 50% level.</li> <li>In Table 16, changed num 46 description to read, “<math>\overline{TA}</math> assertion to rising edge ...”</li> <li>In Figure 46, changed <math>\overline{TA}</math> to reflect the rising edge of the clock.</li> </ul>
7.0	9/2004	<ul style="list-style-type: none"> <li>Added a tablefootnote to Table 6 DC Electrical Specifications about meeting the VIL Max of the I2C Standard</li> <li>Replaced the thermal characteristics in Table 4 by the ZQ package</li> <li>Add the new parts to the Ordering and Availability Chart in Table 34</li> <li>Added the mechanical spec of the ZQ package in Figure 78</li> <li>Removed all of the old revisions from Table 5</li> </ul>
6.3	9/2003	<ul style="list-style-type: none"> <li>Added Section 11.2 on the Port C interrupt pins</li> <li>Nontechnical reformatting</li> </ul>
6.2	8/2003	<ul style="list-style-type: none"> <li>Changed B28a through B28d and B29d to show that TRLX can be 0 or 1</li> <li>Changed reference documentation to reflect the Rev 2 MPC860 PowerQUICC Family Users Manual</li> <li>Nontechnical reformatting</li> </ul>
6.1	11/2002	<ul style="list-style-type: none"> <li>Corrected UTOPIA RXenb* and TXenb* timing values</li> <li>Changed incorrect usage of Vcc to Vdd</li> <li>Corrected dual port RAM to 8 Kbytes</li> </ul>
6	10/2002	Added the MPC855T. Corrected Figure 26 on page -36.
5.1	11/2001	Revised template format, removed references to MAC functionality, changed Table 7 B23 max value @ 66 MHz from 2ns to 8ns, added this revision history table