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Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	50MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (2)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 95°C (TA)
Security Features	-
Package / Case	357-BBGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc860deczq50d4r2

Table 7. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B9	CLKOUT to A(0:31), BADDR(28:30), RD/WR, BURST, D(0:31), DP(0:3), TSIZ(0:1), REG, RSV, AT(0:3), PTR High-Z	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.04	ns
B11	CLKOUT to \overline{TS} , \overline{BB} assertion	7.58	13.58	6.25	12.25	5.00	11.00	3.80	11.29	ns
B11a	CLKOUT to \overline{TA} , \overline{BI} assertion (when driven by the memory controller or PCMCIA interface)	2.50	9.25	2.50	9.25	2.50	9.25	2.50	9.75	ns
B12	CLKOUT to \overline{TS} , \overline{BB} negation	7.58	14.33	6.25	13.00	5.00	11.75	3.80	8.54	ns
B12a	CLKOUT to \overline{TA} , \overline{BI} negation (when driven by the memory controller or PCMCIA interface)	2.50	11.00	2.50	11.00	2.50	11.00	2.50	9.00	ns
B13	CLKOUT to \overline{TS} , \overline{BB} High-Z	7.58	21.58	6.25	20.25	5.00	19.00	3.80	14.04	ns
B13a	CLKOUT to \overline{TA} , \overline{BI} High-Z (when driven by the memory controller or PCMCIA interface)	2.50	15.00	2.50	15.00	2.50	15.00	2.50	15.00	ns
B14	CLKOUT to \overline{TEA} assertion	2.50	10.00	2.50	10.00	2.50	10.00	2.50	9.00	ns
B15	CLKOUT to \overline{TEA} High-Z	2.50	15.00	2.50	15.00	2.50	15.00	2.50	15.00	ns
B16	\overline{TA} , \overline{BI} valid to CLKOUT (setup time)	9.75	—	9.75	—	9.75	—	6.00	—	ns
B16a	\overline{TEA} , \overline{KR} , \overline{RETRY} , \overline{CR} valid to CLKOUT (setup time)	10.00	—	10.00	—	10.00	—	4.50	—	ns
B16b	\overline{BB} , \overline{BG} , \overline{BR} , valid to CLKOUT (setup time) ⁵	8.50	—	8.50	—	8.50	—	4.00	—	ns
B17	CLKOUT to \overline{TA} , \overline{TEA} , \overline{BI} , \overline{BB} , \overline{BG} , \overline{BR} valid (hold time)	1.00	—	1.00	—	1.00	—	2.00	—	ns
B17a	CLKOUT to \overline{KR} , \overline{RETRY} , \overline{CR} valid (hold time)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B18	D(0:31), DP(0:3) valid to CLKOUT rising edge (setup time) ⁶	6.00	—	6.00	—	6.00	—	6.00	—	ns
B19	CLKOUT rising edge to D(0:31), DP(0:3) valid (hold time) ⁶	1.00	—	1.00	—	1.00	—	2.00	—	ns
B20	D(0:31), DP(0:3) valid to CLKOUT falling edge (setup time) ⁷	4.00	—	4.00	—	4.00	—	4.00	—	ns
B21	CLKOUT falling edge to D(0:31), DP(0:3) valid (hold time) ⁷	2.00	—	2.00	—	2.00	—	2.00	—	ns
B22	CLKOUT rising edge to \overline{CS} asserted GPCM ACS = 00	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.04	ns
B22a	CLKOUT falling edge to \overline{CS} asserted GPCM ACS = 10, TRLX = 0	—	8.00	—	8.00	—	8.00	—	8.00	ns
B22b	CLKOUT falling edge to \overline{CS} asserted GPCM ACS = 11, TRLX = 0, EBDF = 0	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.54	ns
B22c	CLKOUT falling edge to \overline{CS} asserted GPCM ACS = 11, TRLX = 0, EBDF = 1	10.86	17.99	8.88	16.00	7.00	14.13	5.18	12.31	ns

Table 7. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B35	A(0:31), BADDR(28:30) to \overline{CS} valid—as requested by control bit BST4 in the corresponding word in UPM	5.58	—	4.25	—	3.00	—	1.79	—	ns
B35a	A(0:31), BADDR(28:30), and D(0:31) to \overline{BS} valid—as requested by control bit BST1 in the corresponding word in UPM	13.15	—	10.50	—	8.00	—	5.58	—	ns
B35b	A(0:31), BADDR(28:30), and D(0:31) to \overline{BS} valid—as requested by control bit BST2 in the corresponding word in UPM	20.73	—	16.75	—	13.00	—	9.36	—	ns
B36	A(0:31), BADDR(28:30), and D(0:31) to \overline{GPL} valid—as requested by control bit GxT4 in the corresponding word in UPM	5.58	—	4.25	—	3.00	—	1.79	—	ns
B37	UPWAIT valid to CLKOUT falling edge ⁹	6.00	—	6.00	—	6.00	—	6.00	—	ns
B38	CLKOUT falling edge to UPWAIT valid ⁹	1.00	—	1.00	—	1.00	—	1.00	—	ns
B39	\overline{AS} valid to CLKOUT rising edge ¹⁰	7.00	—	7.00	—	7.00	—	7.00	—	ns
B40	A(0:31), TSIZ(0:1), RD/ \overline{WR} , \overline{BURST} , valid to CLKOUT rising edge	7.00	—	7.00	—	7.00	—	7.00	—	ns
B41	\overline{TS} valid to CLKOUT rising edge (setup time)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B42	CLKOUT rising edge to \overline{TS} valid (hold time)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B43	\overline{AS} negation to memory controller signals negation	—	TBD	—	TBD	—	TBD	—	TBD	ns

¹ Phase and frequency jitter performance results are only valid if the input jitter is less than the prescribed value.

² If the rate of change of the frequency of EXTAL is slow (that is, it does not jump between the minimum and maximum values in one cycle) or the frequency of the jitter is fast (that is, it does not stay at an extreme value for a long time) then the maximum allowed jitter on EXTAL can be up to 2%.

³ The timings specified in B4 and B5 are based on full strength clock.

⁴ The timing for \overline{BR} output is relevant when the MPC860 is selected to work with external bus arbiter. The timing for \overline{BG} output is relevant when the MPC860 is selected to work with internal bus arbiter.

⁵ The timing required for \overline{BR} input is relevant when the MPC860 is selected to work with internal bus arbiter. The timing for \overline{BG} input is relevant when the MPC860 is selected to work with external bus arbiter.

⁶ The D(0:31) and DP(0:3) input timings B18 and B19 refer to the rising edge of the CLKOUT in which the \overline{TA} input signal is asserted.

⁷ The D(0:31) and DP(0:3) input timings B20 and B21 refer to the falling edge of the CLKOUT. This timing is valid only for read accesses controlled by chip-selects under control of the UPM in the memory controller, for data beats where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

⁸ The timing B30 refers to \overline{CS} when ACS = 00 and to \overline{WE} (0:3) when CSNT = 0.

⁹ The signal UPWAIT is considered asynchronous to the CLKOUT and synchronized internally. The timings specified in B37 and B38 are specified to enable the freeze of the UPM output signals as described in [Figure 18](#).

¹⁰ The \overline{AS} signal is considered asynchronous to the CLKOUT. The timing B39 is specified in order to allow the behavior specified in [Figure 21](#).

Figure 5 provides the timing for the synchronous output signals.

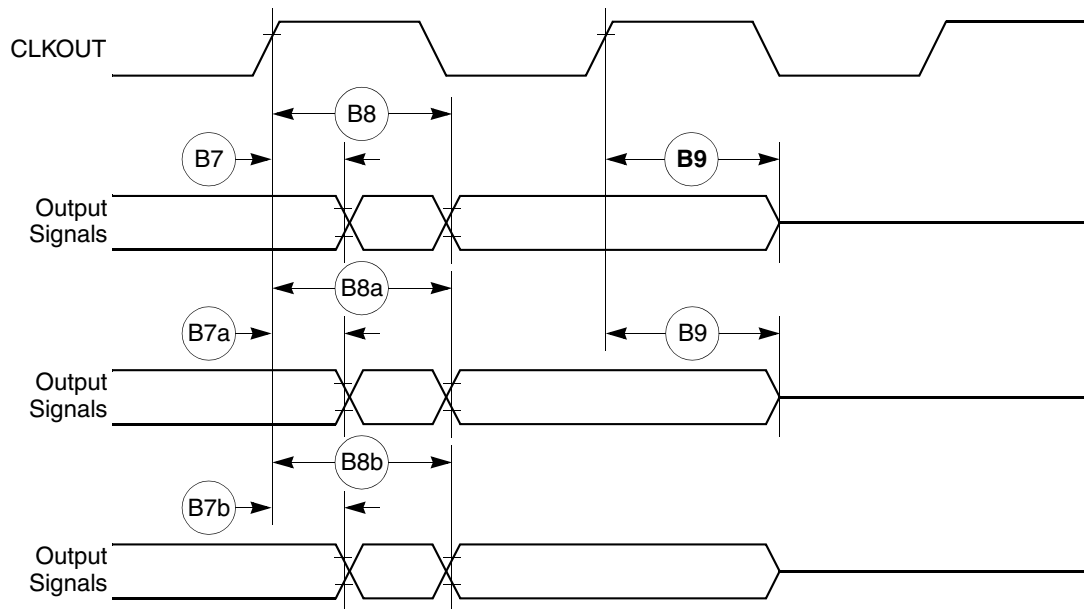


Figure 5. Synchronous Output Signals Timing

Figure 6 provides the timing for the synchronous active pull-up and open-drain output signals.

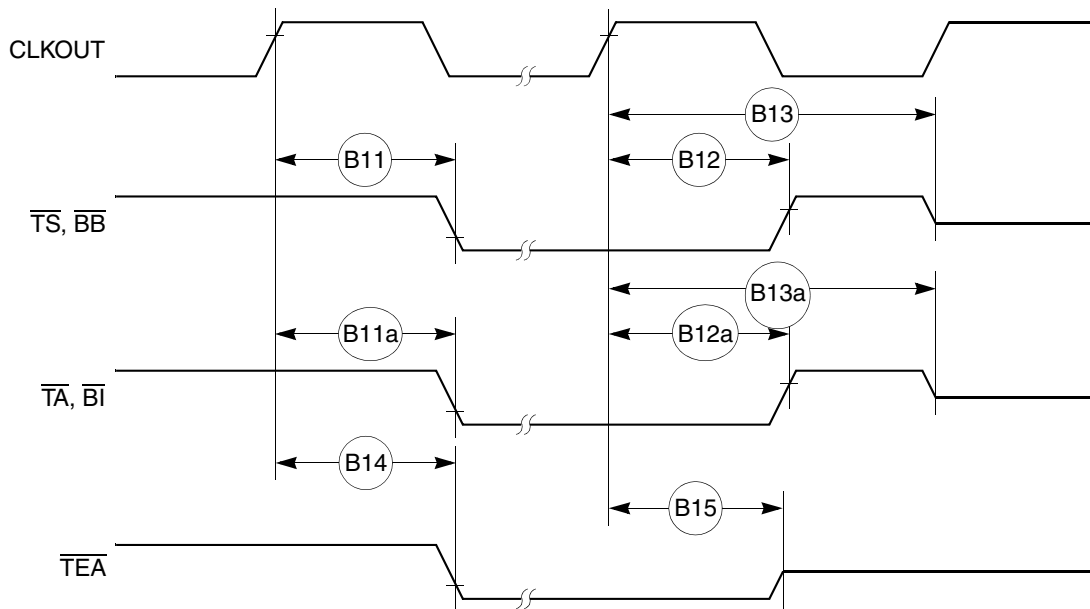


Figure 6. Synchronous Active Pull-Up Resistor and Open-Drain Outputs Signals Timing

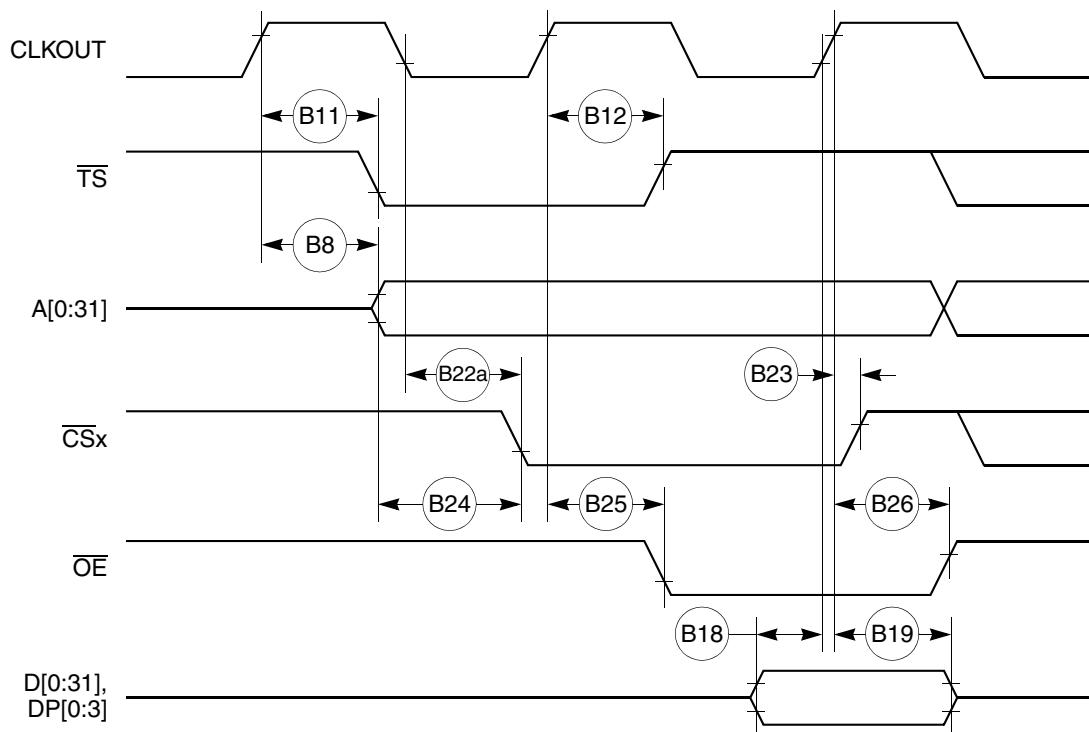


Figure 11. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 10)

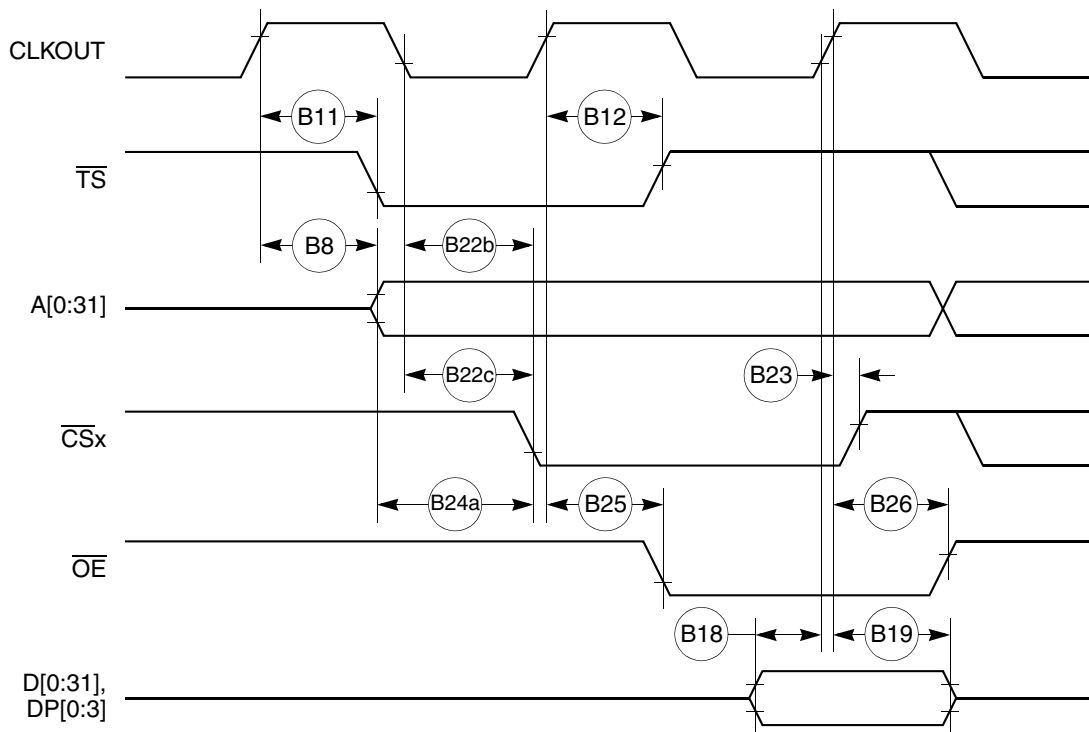


Figure 12. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 11)

Figure 14 through Figure 16 provide the timing for the external bus write controlled by various GPCM factors.

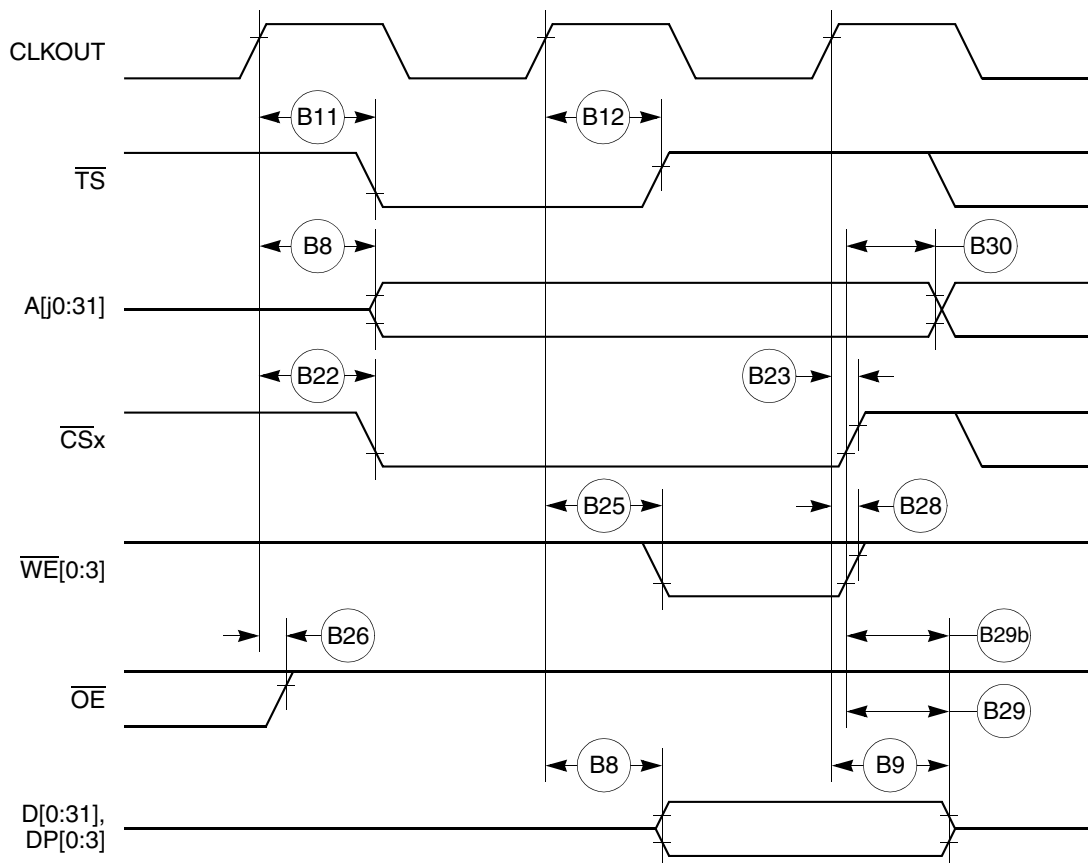


Figure 14. External Bus Write Timing (GPCM Controlled—TRLX = 0 or 1, CSNT = 0)

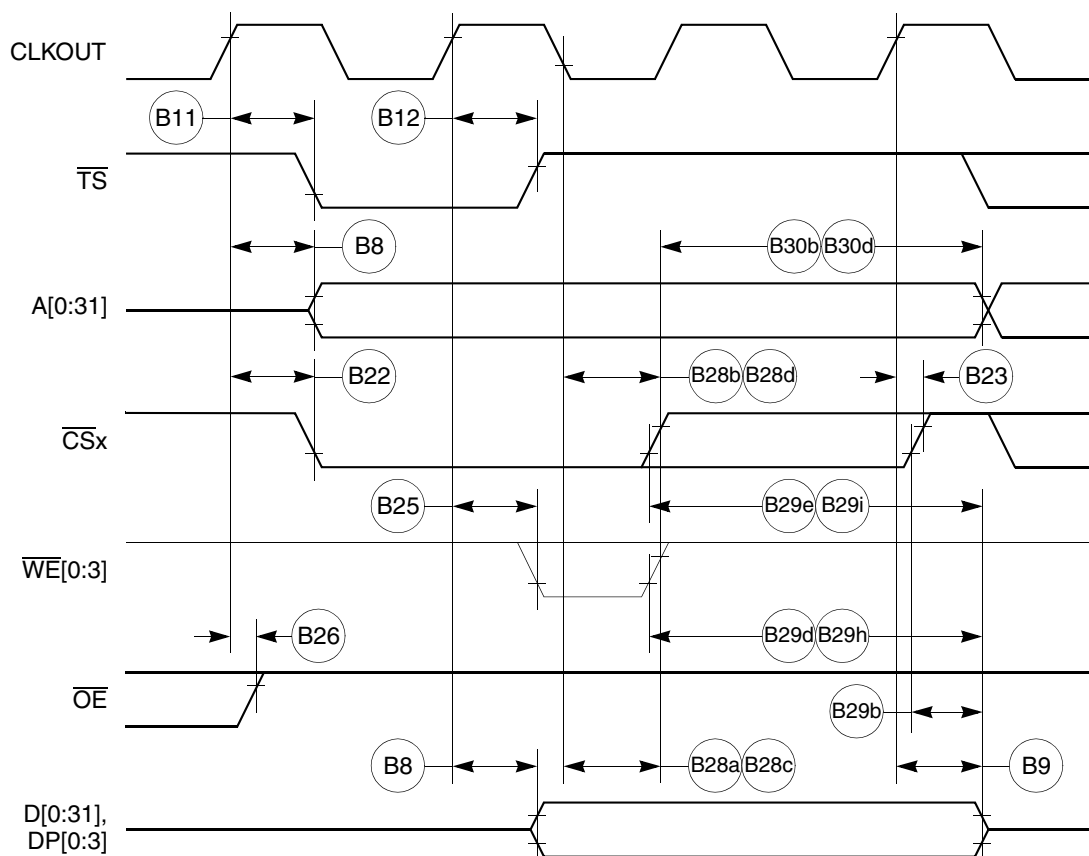


Figure 16. External Bus Write Timing (GPCM Controlled—TRLX = 0 or 1, CSNT = 1)

Figure 17 provides the timing for the external bus controlled by the UPM.

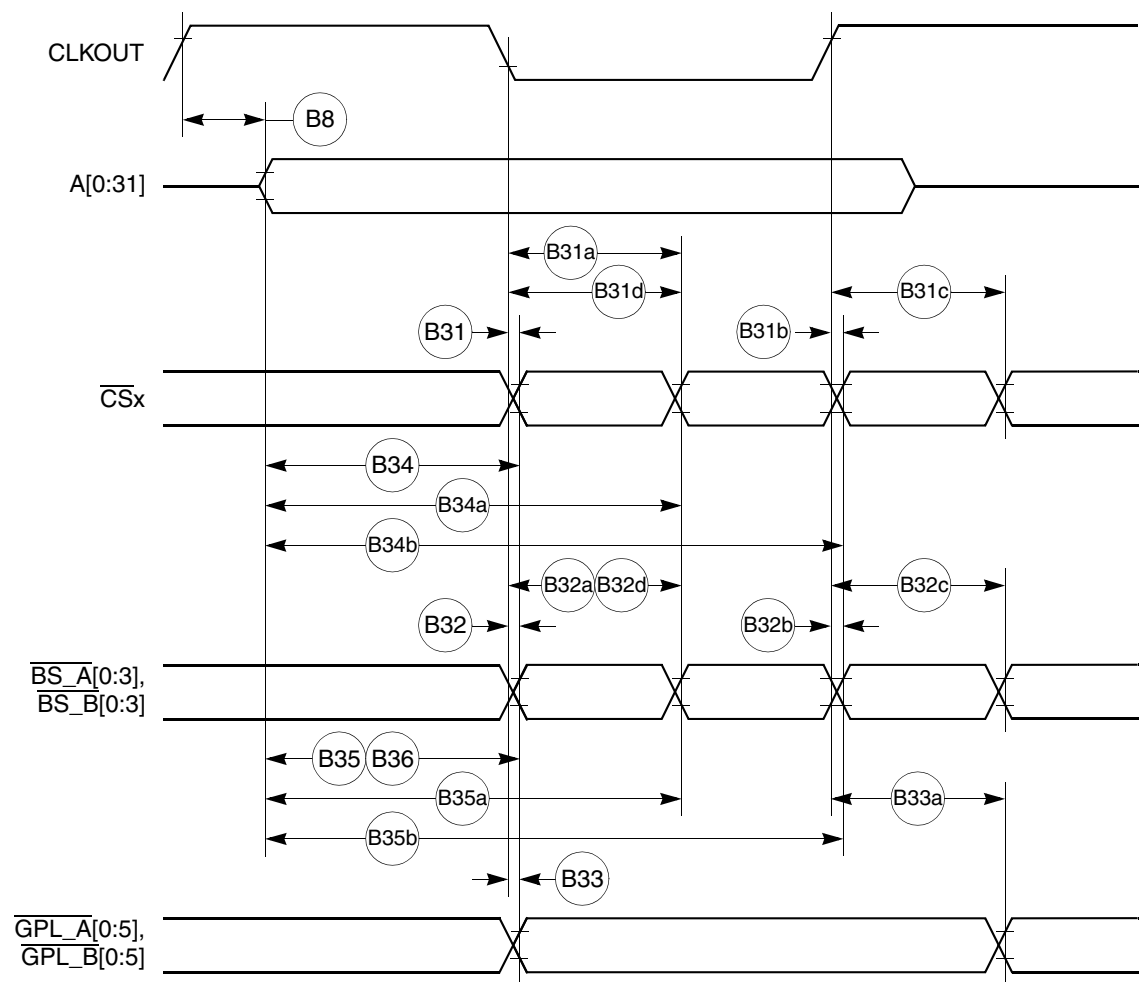


Figure 17. External Bus Timing (UPM Controlled Signals)

Figure 18 provides the timing for the asynchronous asserted UPWAIT signal controlled by the UPM.

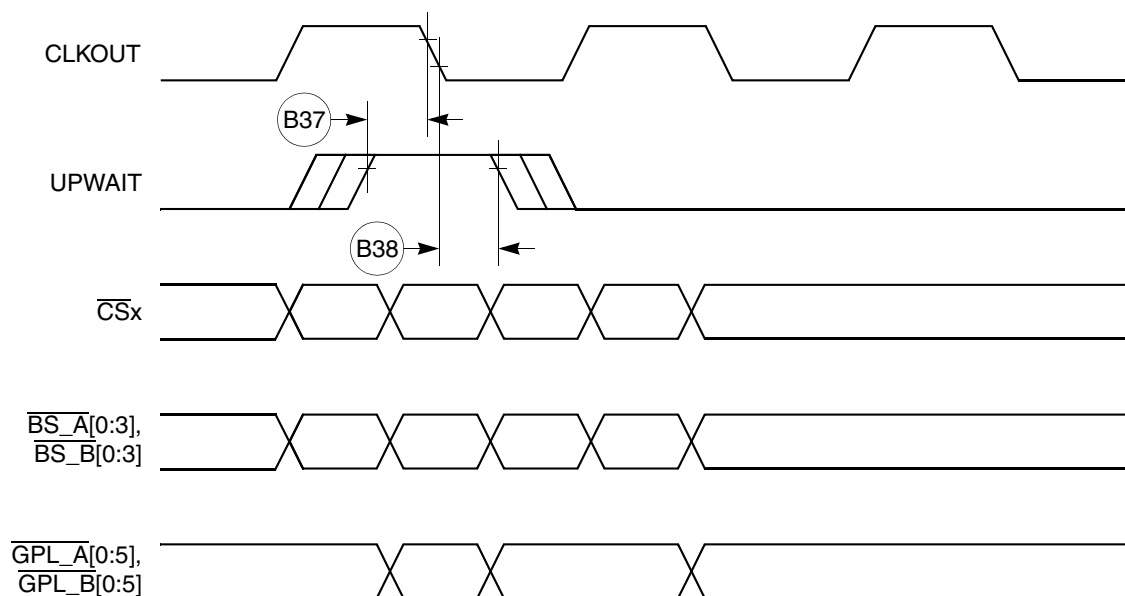


Figure 18. Asynchronous UPWAIT Asserted Detection in UPM Handled Cycles Timing

Figure 19 provides the timing for the asynchronous negated UPWAIT signal controlled by the UPM.

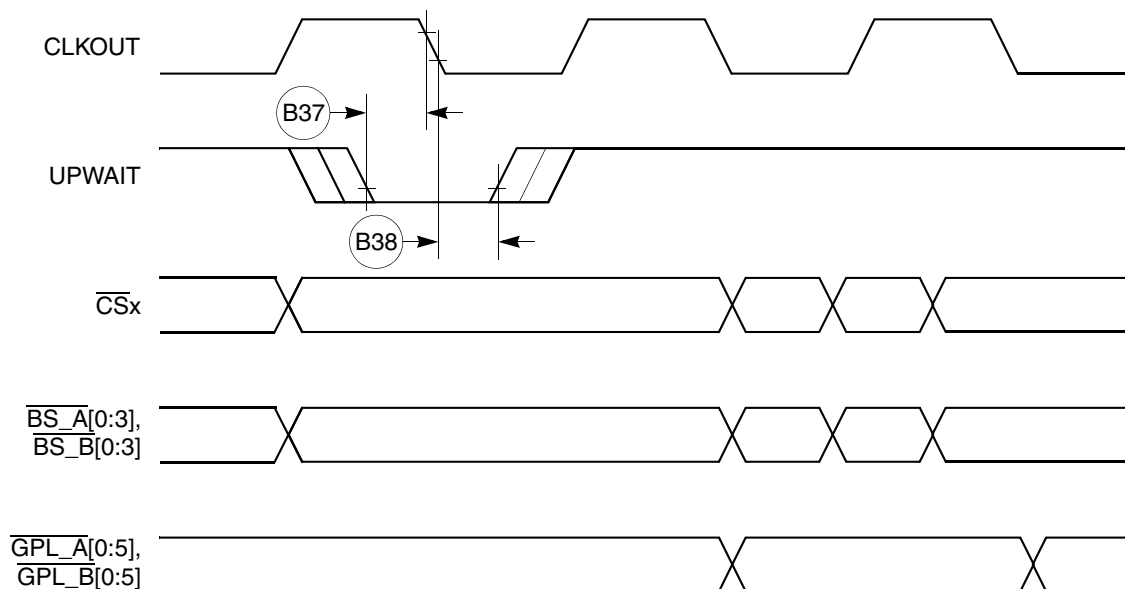


Figure 19. Asynchronous UPWAIT Negated Detection in UPM Handled Cycles Timing

Table 11 shows the debug port timing for the MPC860.

Table 11. Debug Port Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
P61	DSCK cycle time	$3 \times T_{\text{CLOCKOUT}}$	—	—
P62	DSCK clock pulse width	$1.25 \times T_{\text{CLOCKOUT}}$	—	—
P63	DSCK rise and fall times	0.00	3.00	ns
P64	DSDI input data setup time	8.00	—	ns
P65	DSDI data hold time	5.00	—	ns
P66	DSCK low to DSDO data valid	0.00	15.00	ns
P67	DSCK low to DSDO invalid	0.00	2.00	ns

Figure 30 provides the input timing for the debug port clock.

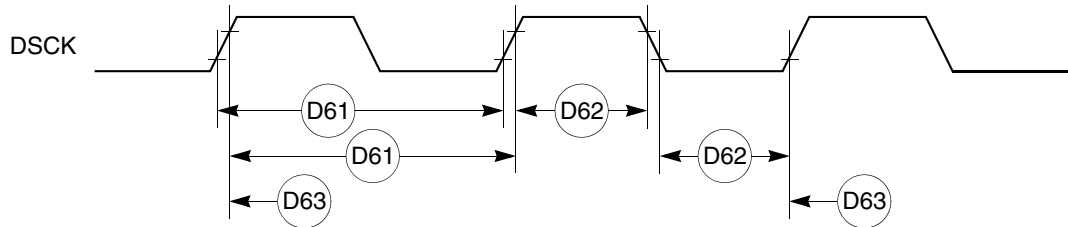


Figure 30. Debug Port Clock Input Timing

Figure 31 provides the timing for the debug port.

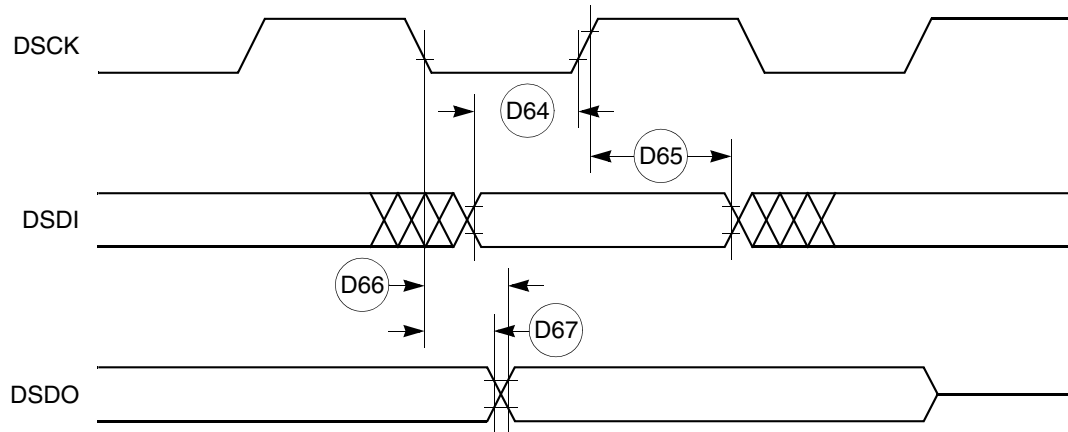


Figure 31. Debug Port Timings

Table 16. IDMA Controller Timing (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
42	$\overline{\text{SDACK}}$ assertion delay from clock high	—	12	ns
43	$\overline{\text{SDACK}}$ negation delay from clock low	—	12	ns
44	$\overline{\text{SDACK}}$ negation delay from $\overline{\text{TA}}$ low	—	20	ns
45	$\overline{\text{SDACK}}$ negation delay from clock high	—	15	ns
46	$\overline{\text{TA}}$ assertion to rising edge of the clock setup time (applies to external $\overline{\text{TA}}$)	7	—	ns

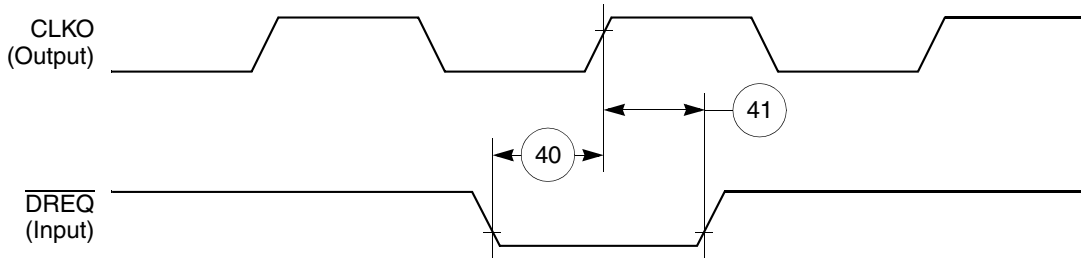


Figure 45. IDMA External Requests Timing Diagram

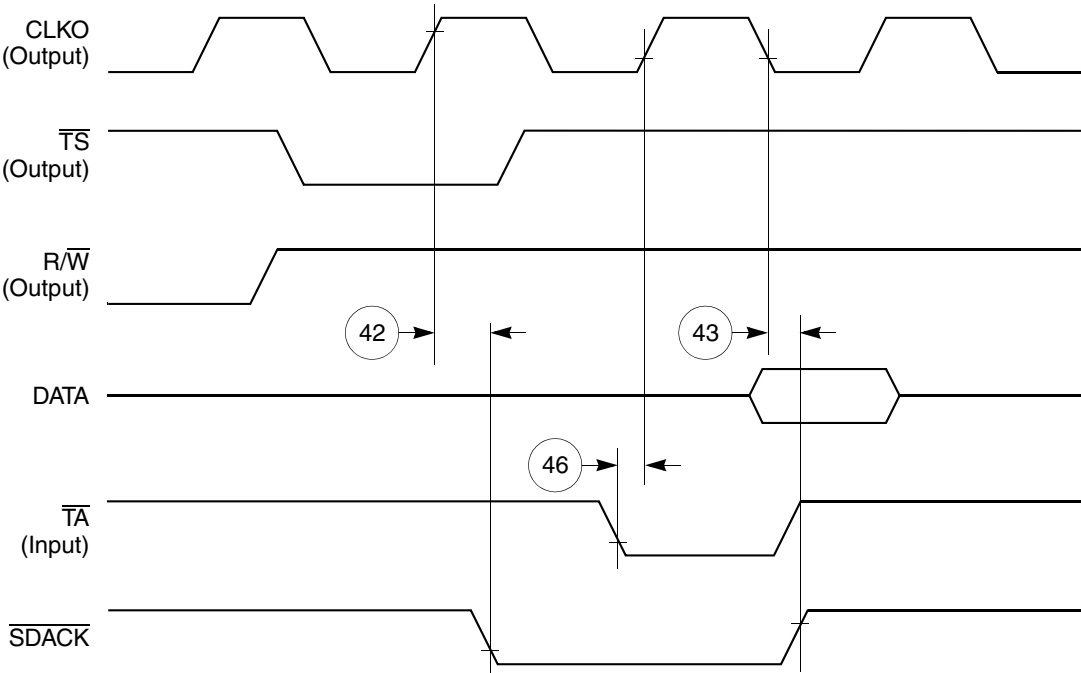


Figure 46. $\overline{\text{SDACK}}$ Timing Diagram—Peripheral Write, Externally-Generated $\overline{\text{TA}}$

11.4 Baud Rate Generator AC Electrical Specifications

Table 17 provides the baud rate generator timings as shown in Figure 49.

Table 17. Baud Rate Generator Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
50	BRGO rise and fall time	—	10	ns
51	BRGO duty cycle	40	60	%
52	BRGO cycle	40	—	ns

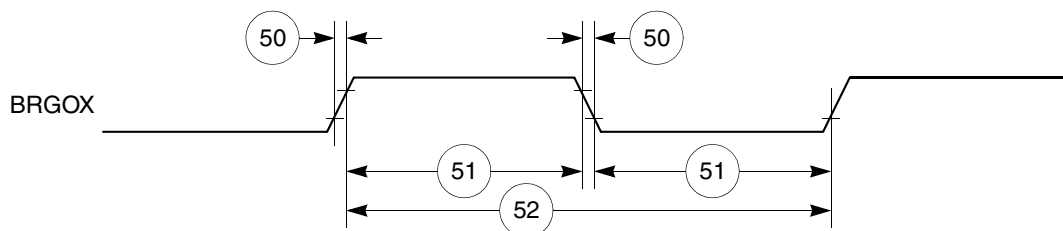


Figure 49. Baud Rate Generator Timing Diagram

11.5 Timer AC Electrical Specifications

Table 18 provides the general-purpose timer timings as shown in Figure 50.

Table 18. Timer Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
61	TIN/TGATE rise and fall time	10	—	ns
62	TIN/TGATE low time	1	—	CLK
63	TIN/TGATE high time	2	—	CLK
64	TIN/TGATE cycle time	3	—	CLK
65	CLKO low to TOUT valid	3	25	ns

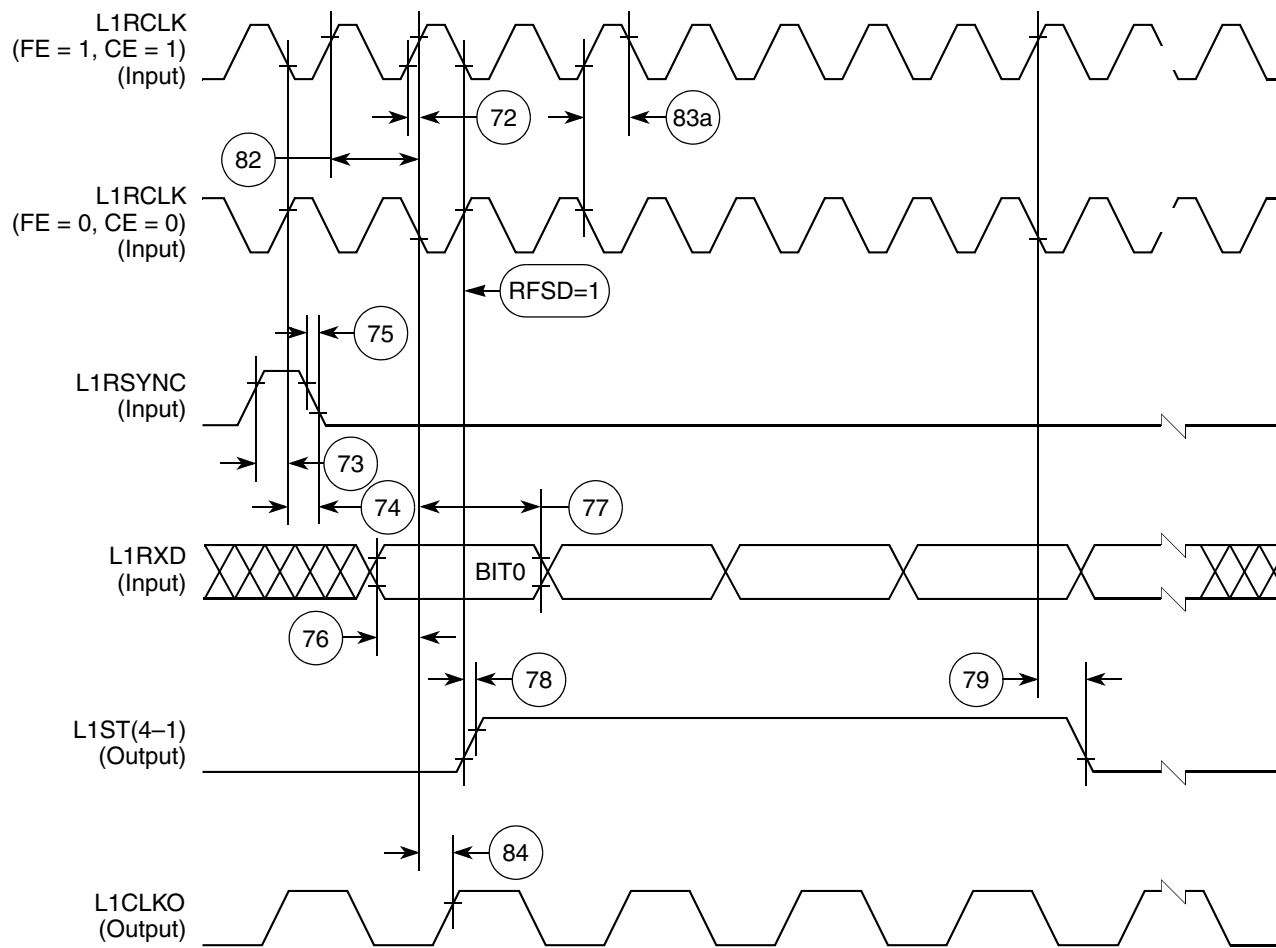


Figure 52. SI Receive Timing with Double-Speed Clocking (DSC = 1)

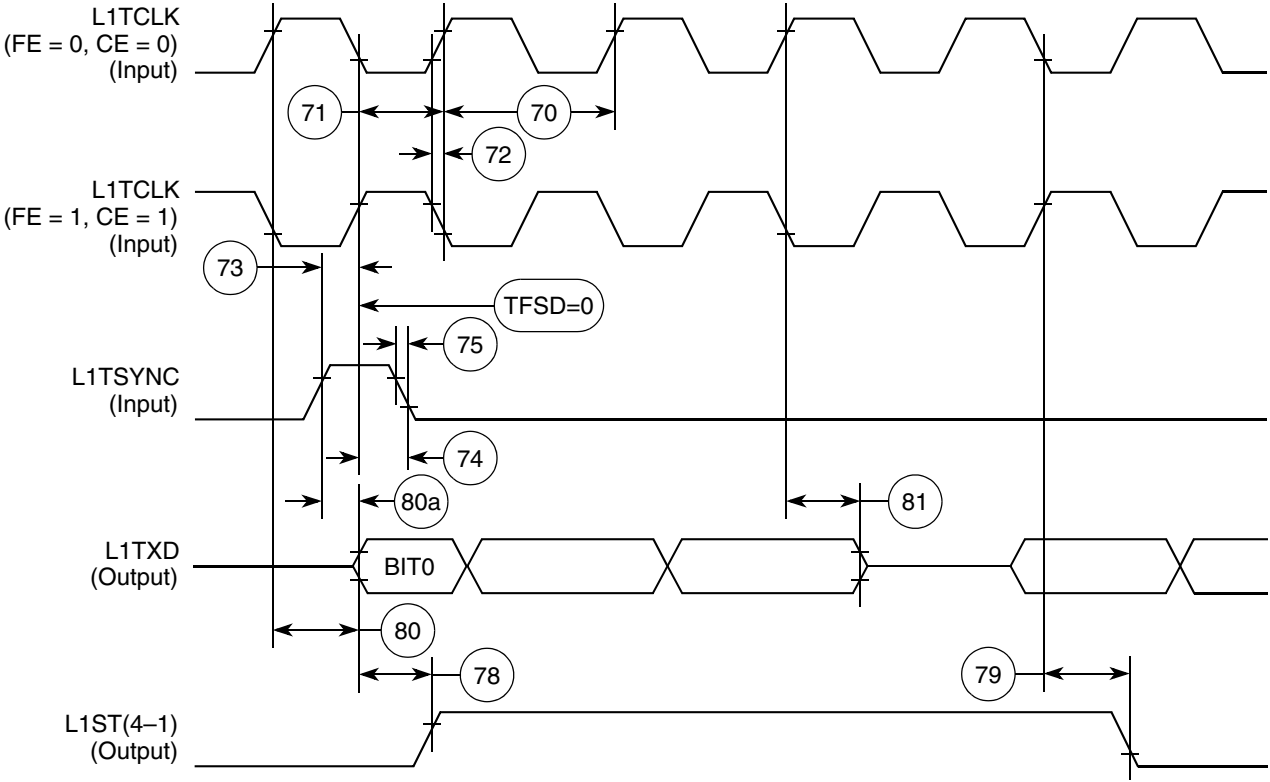


Figure 53. SI Transmit Timing Diagram (DSC = 0)

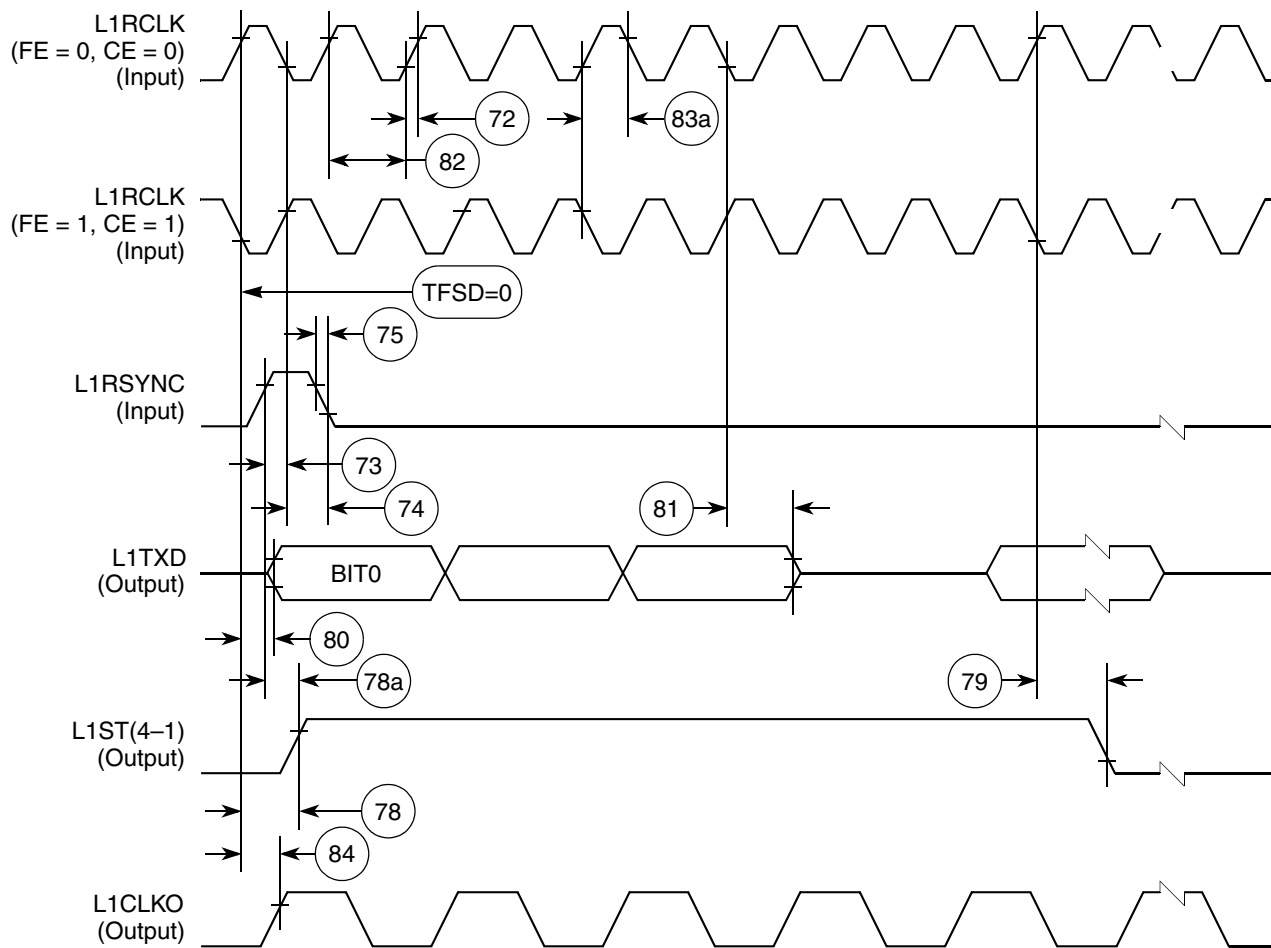


Figure 54. SI Transmit Timing with Double Speed Clocking (DSC = 1)

Figure 56 through Figure 58 show the NMSI timings.

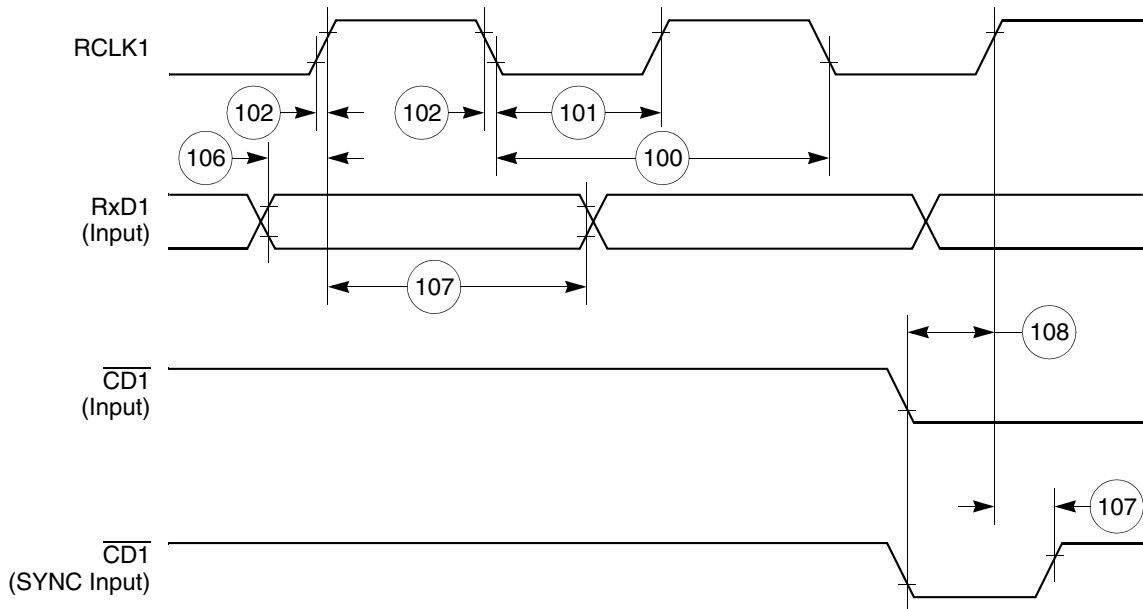


Figure 56. SCC NMSI Receive Timing Diagram

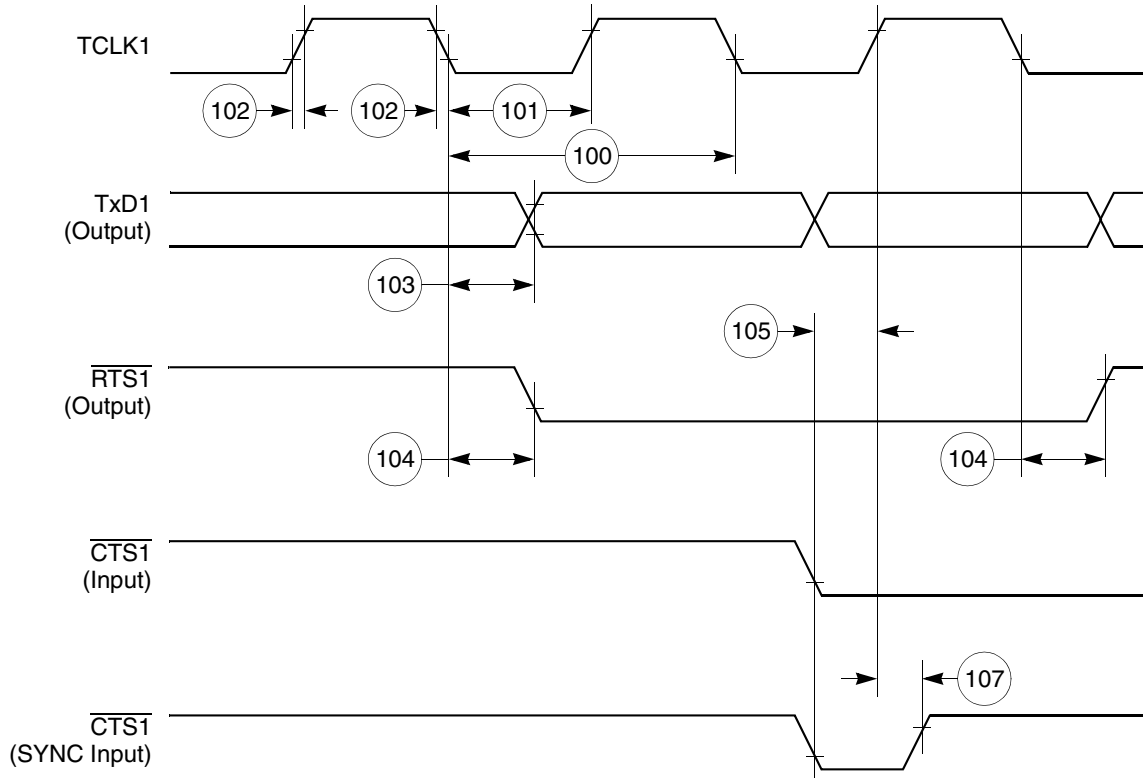


Figure 57. SCC NMSI Transmit Timing Diagram

Table 22. Ethernet Timing (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
135	$\overline{\text{RSTRT}}$ active delay (from TCLK1 falling edge)	10	50	ns
136	$\overline{\text{RSTRT}}$ inactive delay (from TCLK1 falling edge)	10	50	ns
137	$\overline{\text{REJECT}}$ width low	1	—	CLK
138	CLKO1 low to $\overline{\text{SDACK}}$ asserted ²	—	20	ns
139	CLKO1 low to $\overline{\text{SDACK}}$ negated ²	—	20	ns

¹ The ratios SYNCCLK/RCLK1 and SYNCCLK/TCLK1 must be greater than or equal to 2/1.

² $\overline{\text{SDACK}}$ is asserted whenever the SDMA writes the incoming frame DA into memory.

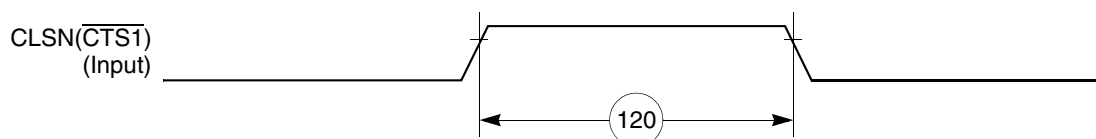


Figure 59. Ethernet Collision Timing Diagram

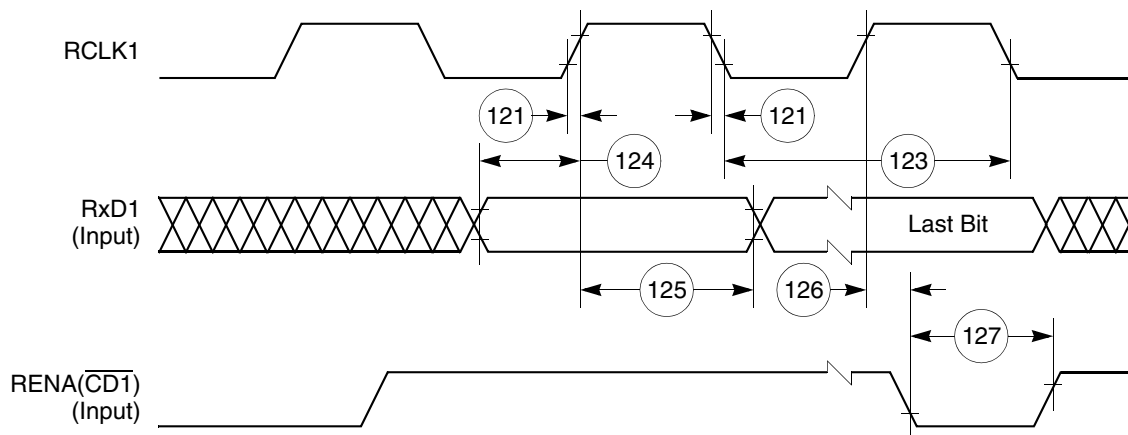


Figure 60. Ethernet Receive Timing Diagram

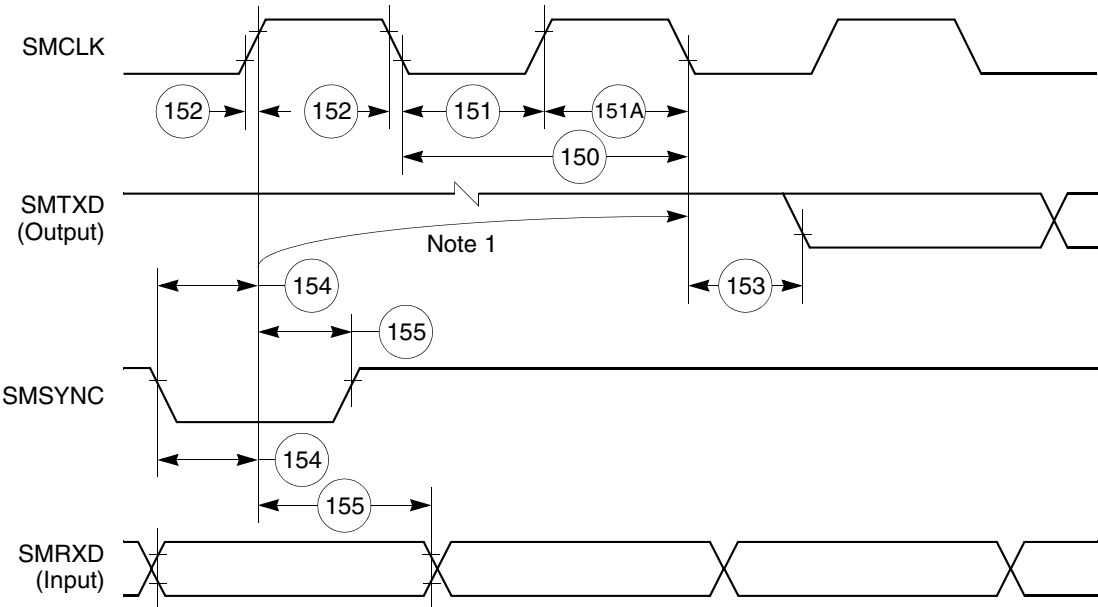
11.9 SMC Transparent AC Electrical Specifications

Table 23 provides the SMC transparent timings as shown in Figure 64.

Table 23. SMC Transparent Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
150	SMCLK clock period ¹	100	—	ns
151	SMCLK width low	50	—	ns
151A	SMCLK width high	50	—	ns
152	SMCLK rise/fall time	—	15	ns
153	SMTXD active delay (from SMCLK falling edge)	10	50	ns
154	SMRXD/SMSYNC setup time	20	—	ns
155	RXD1/SMSYNC hold time	5	—	ns

¹ SYNCCLK must be at least twice as fast as SMCLK.



Note:
1. This delay is equal to an integer number of character-length clocks.

Figure 64. SMC Transparent Timing Diagram

13.2 MII Transmit Signal Timing (MII_TXD[3:0], MII_TX_EN, MII_TX_ER, MII_TX_CLK)

The transmitter functions correctly up to a MII_TX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed the MII_TX_CLK frequency – 1%.

Table 30 provides information on the MII transmit signal timing.

Table 30. MII Transmit Signal Timing

Num	Characteristic	Min	Max	Unit
M5	MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER invalid	5	—	ns
M6	MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER valid	—	25	
M7	MII_TX_CLK pulse width high	35	65%	MII_TX_CLK period
M8	MII_TX_CLK pulse width low	35%	65%	MII_TX_CLK period

Figure 73 shows the MII transmit signal timing diagram.

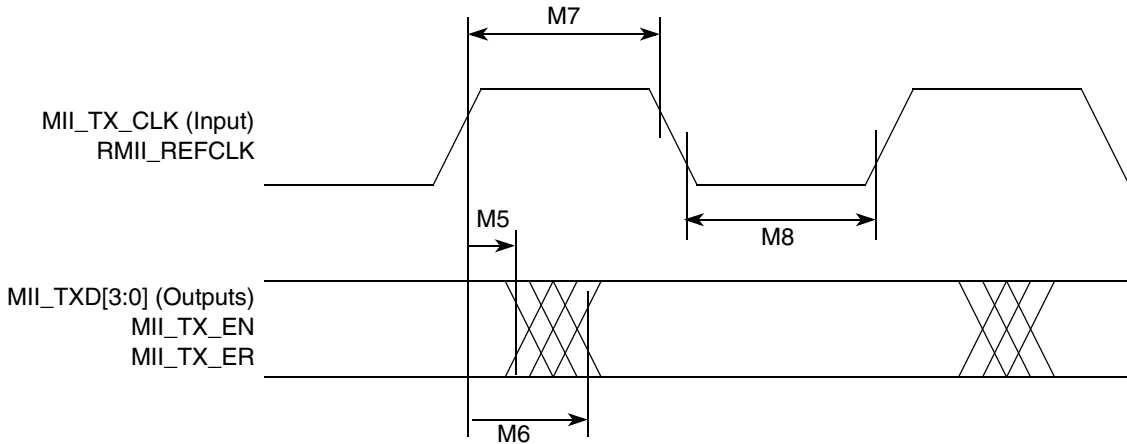


Figure 73. MII Transmit Signal Timing Diagram

14.3 Mechanical Dimensions of the PBGA Package

Figure 77 shows the mechanical dimensions of the ZP PBGA package.

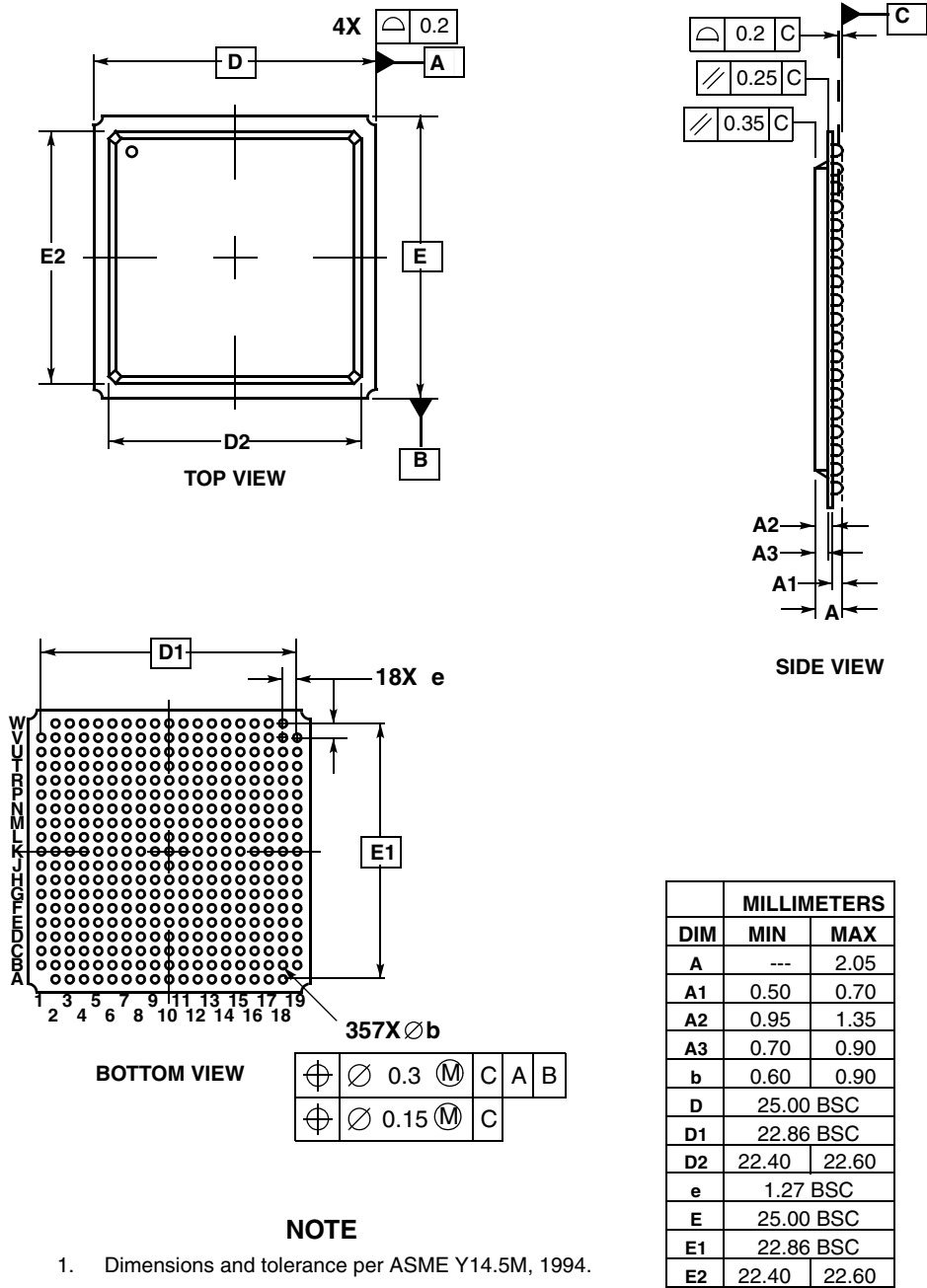


Figure 77. Mechanical Dimensions and Bottom Surface Nomenclature of the ZP PBGA Package

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Document Number: MPC860EC
Rev. 10
09/2015

