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### Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

### Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

#### Details

Product Status	Active
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	50MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (4)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 95°C (TA)
Security Features	-
Package / Case	357-BBGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	<a href="https://www.e-xfl.com/pro/item?MUrl=&amp;PartUrl=mc860encvr50d4r2">https://www.e-xfl.com/pro/item?MUrl=&amp;PartUrl=mc860encvr50d4r2</a>

## 2 Features

The following list summarizes the key MPC860 features:

- Embedded single-issue, 32-bit core (implementing the Power Architecture technology) with thirty-two 32-bit general-purpose registers (GPRs)
  - The core performs branch prediction with conditional prefetch without conditional execution.
  - 4- or 8-Kbyte data cache and 4- or 16-Kbyte instruction cache (see [Table 1](#))
    - 16-Kbyte instruction caches are four-way, set-associative with 256 sets; 4-Kbyte instruction caches are two-way, set-associative with 128 sets.
    - 8-Kbyte data caches are two-way, set-associative with 256 sets; 4-Kbyte data caches are two-way, set-associative with 128 sets.
    - Cache coherency for both instruction and data caches is maintained on 128-bit (4-word) cache blocks.
    - Caches are physically addressed, implement a least recently used (LRU) replacement algorithm, and are lockable on a cache block basis.
  - MMUs with 32-entry TLB, fully-associative instruction, and data TLBs
  - MMUs support multiple page sizes of 4-, 16-, and 512-Kbytes, and 8-Mbytes; 16 virtual address spaces and 16 protection groups
  - Advanced on-chip-emulation debug mode
- Up to 32-bit data bus (dynamic bus sizing for 8, 16, and 32 bits)
- 32 address lines
- Operates at up to 80 MHz
- Memory controller (eight banks)
  - Contains complete dynamic RAM (DRAM) controller
  - Each bank can be a chip select or  $\overline{\text{RAS}}$  to support a DRAM bank.
  - Up to 15 wait states programmable per memory bank
  - Glueless interface to DRAM, SIMMS, SRAM, EPROM, Flash EPROM, and other memory devices
  - DRAM controller programmable to support most size and speed memory interfaces
  - Four  $\overline{\text{CAS}}$  lines, four  $\overline{\text{WE}}$  lines, and one  $\overline{\text{OE}}$  line
  - Boot chip-select available at reset (options for 8-, 16-, or 32-bit memory)
  - Variable block sizes (32 Kbytes to 256 Mbytes)
  - Selectable write protection
  - On-chip bus arbitration logic
- General-purpose timers
  - Four 16-bit timers or two 32-bit timers
  - Gate mode can enable/disable counting
  - Interrupt can be masked on reference match and event capture.

- System integration unit (SIU)
  - Bus monitor
  - Software watchdog
  - Periodic interrupt timer (PIT)
  - Low-power stop mode
  - Clock synthesizer
  - Decrementer, time base, and real-time clock (RTC)
  - Reset controller
  - IEEE 1149.1™ Std. test access port (JTAG)
- Interrupts
  - Seven external interrupt request (IRQ) lines
  - 12 port pins with interrupt capability
  - 23 internal interrupt sources
  - Programmable priority between SCCs
  - Programmable highest priority request
- 10/100 Mbps Ethernet support, fully compliant with the IEEE 802.3u® Standard (not available when using ATM over UTOPIA interface)
- ATM support compliant with ATM forum UNI 4.0 specification
  - Cell processing up to 50–70 Mbps at 50-MHz system clock
  - Cell multiplexing/demultiplexing
  - Support of AAL5 and AAL0 protocols on a per-VC basis. AAL0 support enables OAM and software implementation of other protocols.
  - ATM pace control (APC) scheduler, providing direct support for constant bit rate (CBR) and unspecified bit rate (UBR) and providing control mechanisms enabling software support of available bit rate (ABR)
  - Physical interface support for UTOPIA (10/100-Mbps is not supported with this interface) and byte-aligned serial (for example, T1/E1/ADSL)
  - UTOPIA-mode ATM supports level-1 master with cell-level handshake, multi-PHY (up to four physical layer devices), connection to 25-, 51-, or 155-Mbps framers, and UTOPIA/system clock ratios of 1/2 or 1/3.
  - Serial-mode ATM connection supports transmission convergence (TC) function for T1/E1/ADSL lines, cell delineation, cell payload scrambling/descrambling, automatic idle/unassigned cell insertion/stripping, header error control (HEC) generation, checking, and statistics.
- Communications processor module (CPM)
  - RISC communications processor (CP)
  - Communication-specific commands (for example, GRACEFUL STOP TRANSMIT, ENTER HUNT MODE, and RESTART TRANSMIT)
  - Supports continuous mode transmission and reception on all serial channels

- Up to 8 Kbytes of dual-port RAM
- 16 serial DMA (SDMA) channels
- Three parallel I/O registers with open-drain capability
- Four baud-rate generators (BRGs)
  - Independent (can be tied to any SCC or SMC)
  - Allows changes during operation
  - Autobaud support option
- Four serial communications controllers (SCCs)
  - Ethernet/IEEE 802.3® standard optional on SCC1–4, supporting full 10-Mbps operation (available only on specially programmed devices)
  - HDLC/SDLC (all channels supported at 2 Mbps)
  - HDLC bus (implements an HDLC-based local area network (LAN))
  - Asynchronous HDLC to support point-to-point protocol (PPP)
  - AppleTalk
  - Universal asynchronous receiver transmitter (UART)
  - Synchronous UART
  - Serial infrared (IrDA)
  - Binary synchronous communication (BISYNC)
  - Totally transparent (bit streams)
  - Totally transparent (frame-based with optional cyclic redundancy check (CRC))
- Two SMCs (serial management channels)
  - UART
  - Transparent
  - General circuit interface (GCI) controller
  - Can be connected to the time-division multiplexed (TDM) channels
- One SPI (serial peripheral interface)
  - Supports master and slave modes
  - Supports multimaster operation on the same bus
- One I<sup>2</sup>C (inter-integrated circuit) port
  - Supports master and slave modes
  - Multiple-master environment support
- Time-slot assigner (TSA)
  - Allows SCCs and SMCs to run in multiplexed and/or non-multiplexed operation
  - Supports T1, CEPT, PCM highway, ISDN basic rate, ISDN primary rate, user defined
  - 1- or 8-bit resolution
  - Allows independent transmit and receive routing, frame synchronization, and clocking

Table 4 shows the thermal characteristics for the MPC860.

**Table 4. MPC860 Thermal Resistance Data**

Rating	Environment		Symbol	ZP MPC860P	ZQ / VR MPC860P	Unit
Mold Compound Thickness				0.85	1.15	mm
Junction-to-ambient <sup>1</sup>	Natural convection	Single-layer board (1s)	$R_{\theta JA}^2$	34	34	°C/W
		Four-layer board (2s2p)	$R_{\theta JMA}^3$	22	22	
	Airflow (200 ft/min)	Single-layer board (1s)	$R_{\theta JMA}^3$	27	27	
		Four-layer board (2s2p)	$R_{\theta JMA}^3$	18	18	
Junction-to-board <sup>4</sup>			$R_{\theta JB}$	14	13	
Junction-to-case <sup>5</sup>			$R_{\theta JC}$	6	8	
Junction-to-package top <sup>6</sup>	Natural convection		$\Psi_{JT}$	2	2	

<sup>1</sup> Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.

<sup>2</sup> Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.

<sup>3</sup> Per JEDEC JESD51-6 with the board horizontal.

<sup>4</sup> Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

<sup>5</sup> Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature. For exposed pad packages where the pad would be expected to be soldered, junction-to-case thermal resistance is a simulated value from the junction to the exposed pad without contact resistance.

<sup>6</sup> Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2.

## 7 Thermal Calculation and Measurement

For the following discussions,  $P_D = (V_{DD} \times I_{DD}) + PI/O$ , where PI/O is the power dissipation of the I/O drivers.

### 7.1 Estimation with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature,  $T_J$ , in °C can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

$T_A$  = ambient temperature (°C)

$R_{\theta JA}$  = package junction-to-ambient thermal resistance (°C/W)

$P_D$  = power dissipation in package

The junction-to-ambient thermal resistance is an industry standard value which provides a quick and easy estimation of thermal performance. However, the answer is only an estimate; test cases have demonstrated that errors of a factor of two (in the quantity  $T_J - T_A$ ) are possible.

### 7.2 Estimation with Junction-to-Case Thermal Resistance

Historically, the thermal resistance has frequently been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$  = junction-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$  = junction-to-case thermal resistance (°C/W)

$R_{\theta CA}$  = case-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$  is device related and cannot be influenced by the user. The user adjusts the thermal environment to affect the case-to-ambient thermal resistance,  $R_{\theta CA}$ . For instance, the user can change the airflow around the device, add a heat sink, change the mounting arrangement on the printed-circuit board, or change the thermal dissipation on the printed-circuit board surrounding the device. This thermal model is most useful for ceramic packages with heat sinks where some 90% of the heat flows through the case and the heat sink to the ambient environment. For most packages, a better model is required.

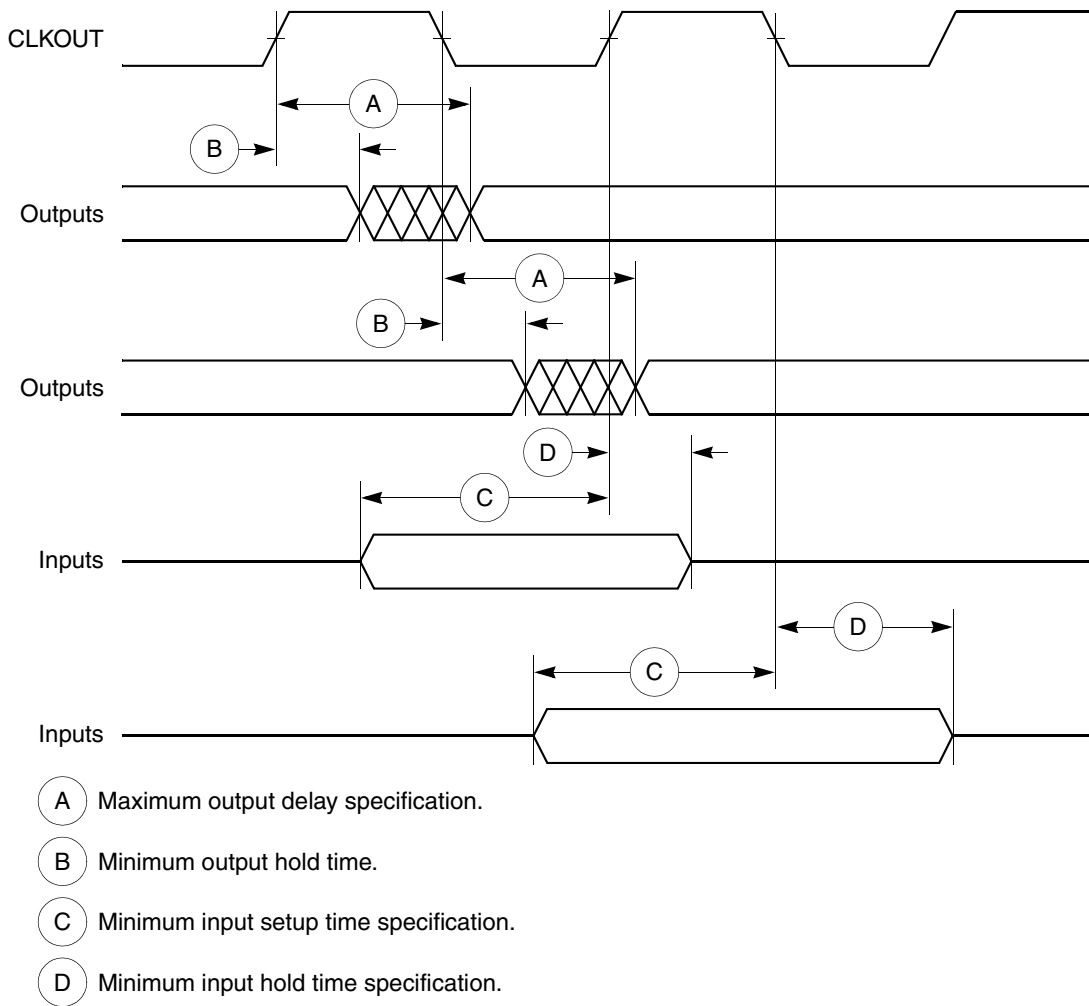
### 7.3 Estimation with Junction-to-Board Thermal Resistance

A simple package thermal model which has demonstrated reasonable accuracy (about 20%) is a two-resistor model consisting of a junction-to-board and a junction-to-case thermal resistance. The junction-to-case thermal resistance covers the situation where a heat sink is used or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed-circuit board. It has been observed that the thermal performance of most plastic packages, especially PBGA packages, is strongly dependent on the board temperature; see [Figure 2](#).

Table 7. Bus Operation Timings (continued)

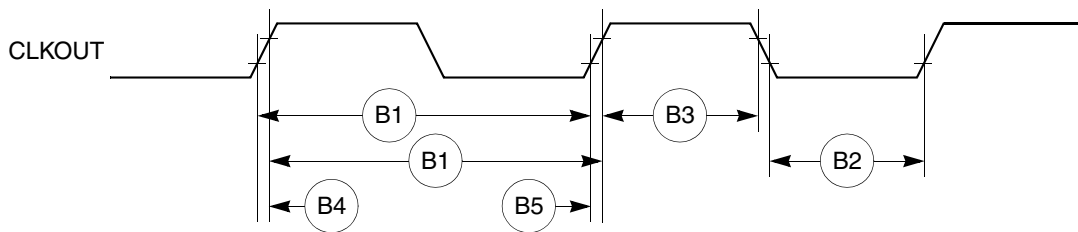
Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B31a	CLKOUT falling edge to $\overline{CS}$ valid—as requested by control bit CST1 in the corresponding word in UPM	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.54	ns
B31b	CLKOUT rising edge to $\overline{CS}$ valid—as requested by control bit CST2 in the corresponding word in UPM	1.50	8.00	1.50	8.00	1.50	8.00	1.50	8.00	ns
B31c	CLKOUT rising edge to $\overline{CS}$ valid—as requested by control bit CST3 in the corresponding word in UPM	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.04	ns
B31d	CLKOUT falling edge to $\overline{CS}$ valid—as requested by control bit CST1 in the corresponding word in UPM, EBDF = 1	13.26	17.99	11.28	16.00	9.40	14.13	7.58	12.31	ns
B32	CLKOUT falling edge to $\overline{BS}$ valid—as requested by control bit BST4 in the corresponding word in UPM	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns
B32a	CLKOUT falling edge to $\overline{BS}$ valid—as requested by control bit BST1 in the corresponding word in UPM, EBDF = 0	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.54	ns
B32b	CLKOUT rising edge to $\overline{BS}$ valid—as requested by control bit BST2 in the corresponding word in UPM	1.50	8.00	1.50	8.00	1.50	8.00	1.50	8.00	ns
B32c	CLKOUT rising edge to $\overline{BS}$ valid—as requested by control bit BST3 in the corresponding word in UPM	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.54	ns
B32d	CLKOUT falling edge to $\overline{BS}$ valid—as requested by control bit BST1 in the corresponding word in UPM, EBDF = 1	13.26	17.99	11.28	16.00	9.40	14.13	7.58	12.31	ns
B33	CLKOUT falling edge to $\overline{GPL}$ valid—as requested by control bit GxT4 in the corresponding word in UPM	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns
B33a	CLKOUT rising edge to $\overline{GPL}$ valid—as requested by control bit GxT3 in the corresponding word in UPM	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.54	ns
B34	A(0:31), BADDR(28:30), and D(0:31) to $\overline{CS}$ valid—as requested by control bit CST4 in the corresponding word in UPM	5.58	—	4.25	—	3.00	—	1.79	—	ns
B34a	A(0:31), BADDR(28:30), and D(0:31) to $\overline{CS}$ valid—as requested by control bit CST1 in the corresponding word in UPM	13.15	—	10.50	—	8.00	—	5.58	—	ns
B34b	A(0:31), BADDR(28:30), and D(0:31) to $\overline{CS}$ valid—as requested by control bit CST2 in the corresponding word in UPM	20.73	—	16.75	—	13.00	—	9.36	—	ns

Figure 3 is the control timing diagram.



**Figure 3. Control Timing**

Figure 4 provides the timing for the external clock.



**Figure 4. External Clock Timing**



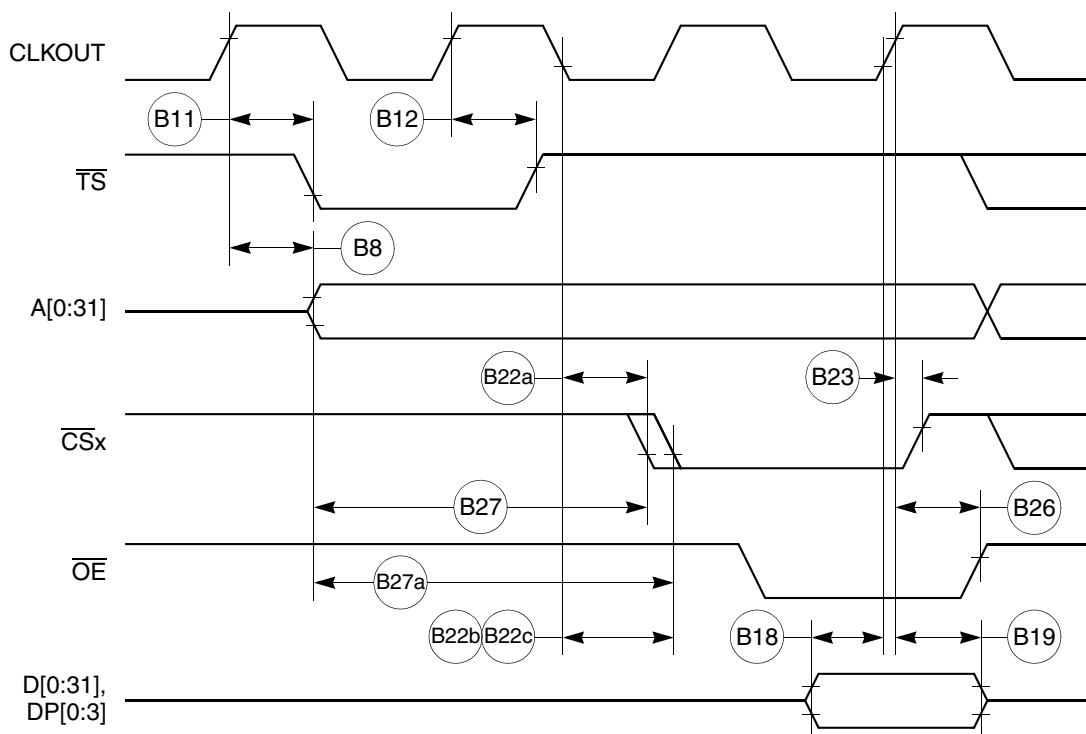


Figure 13. External Bus Read Timing (GPCM Controlled—TRLX = 0 or 1, ACS = 10, ACS = 11)

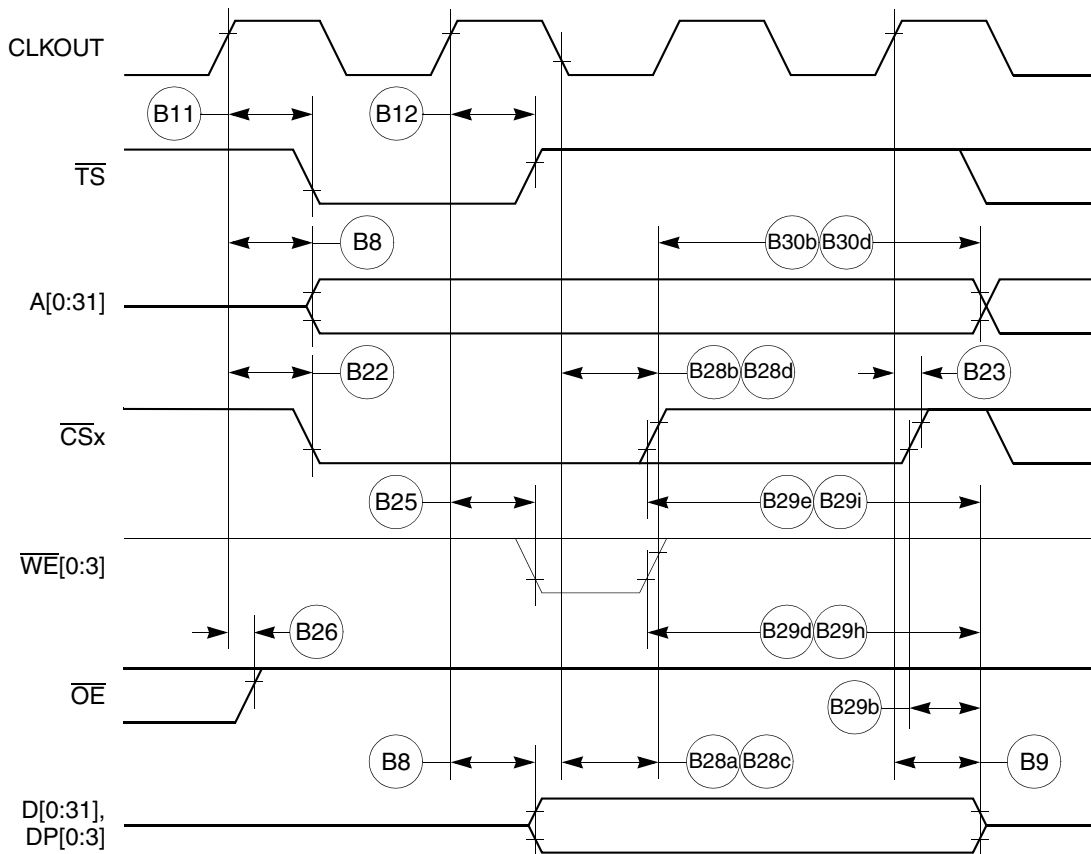


Figure 16. External Bus Write Timing (GPCM Controlled—TRLX = 0 or 1, CSNT = 1)

Figure 20 provides the timing for the synchronous external master access controlled by the GPCM.

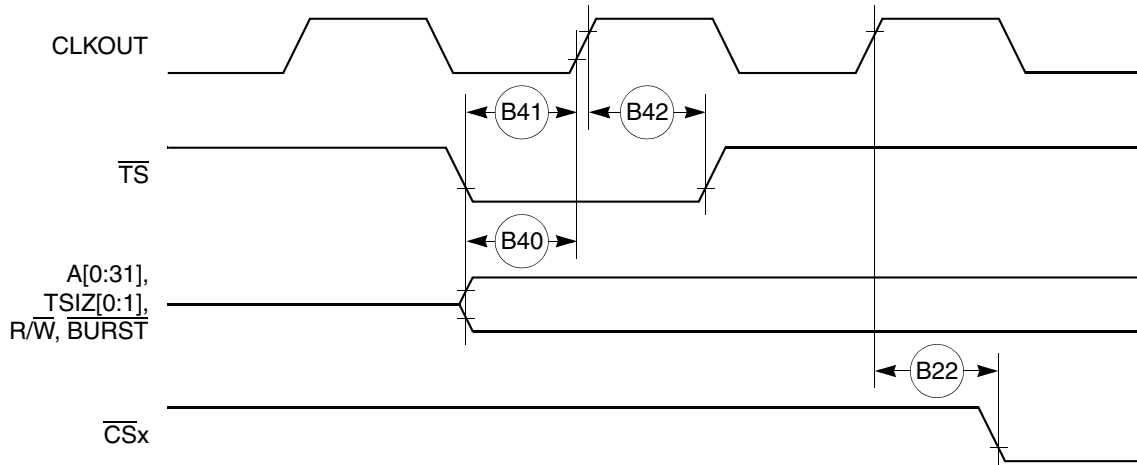


Figure 20. Synchronous External Master Access Timing (GPCM Handled ACS = 00)

Figure 21 provides the timing for the asynchronous external master memory access controlled by the GPCM.

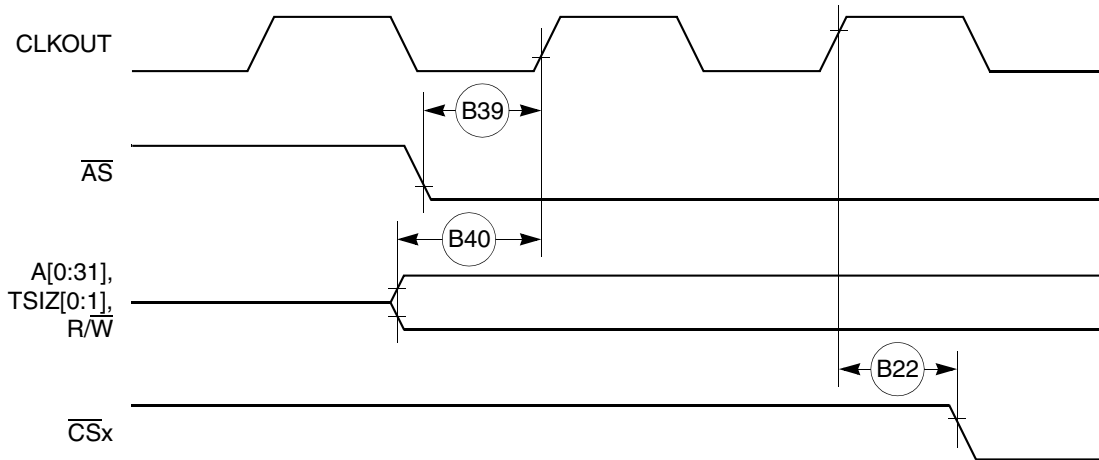


Figure 21. Asynchronous External Master Memory Access Timing (GPCM Controlled—ACS = 00)

Figure 22 provides the timing for the asynchronous external master control signals negation.

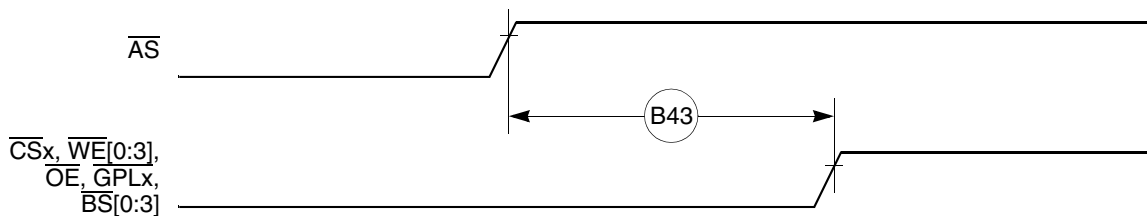


Figure 22. Asynchronous External Master—Control Signals Negation Timing

Figure 25 provides the PCMCIA access cycle timing for the external bus read.

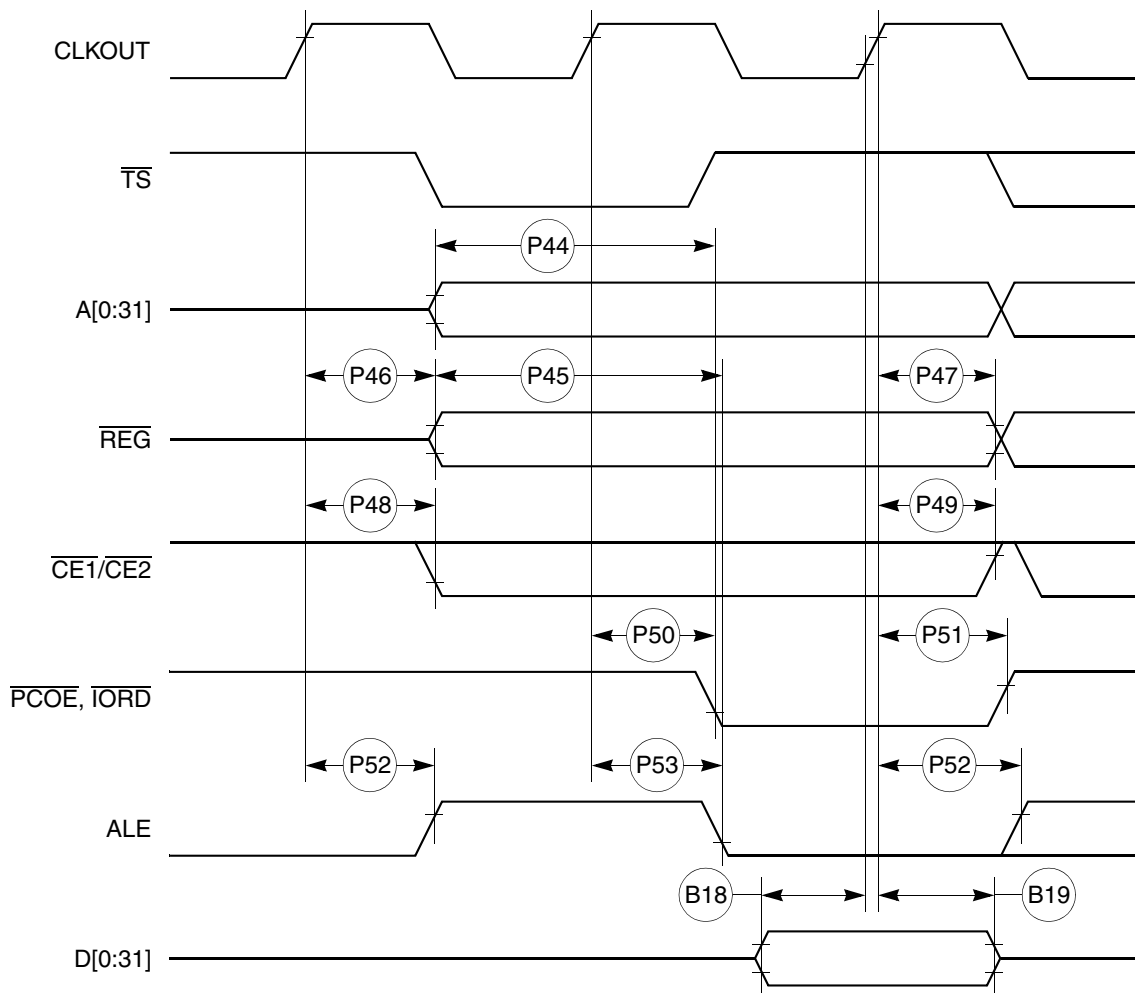
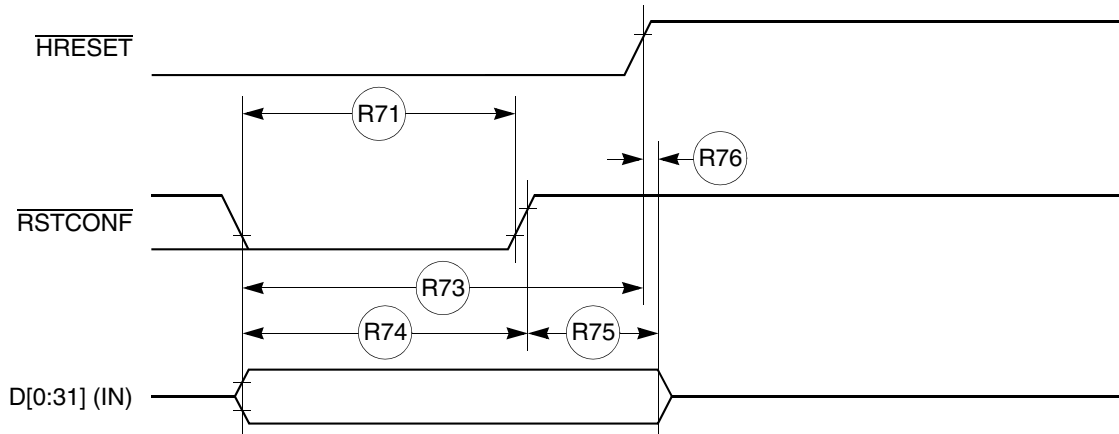


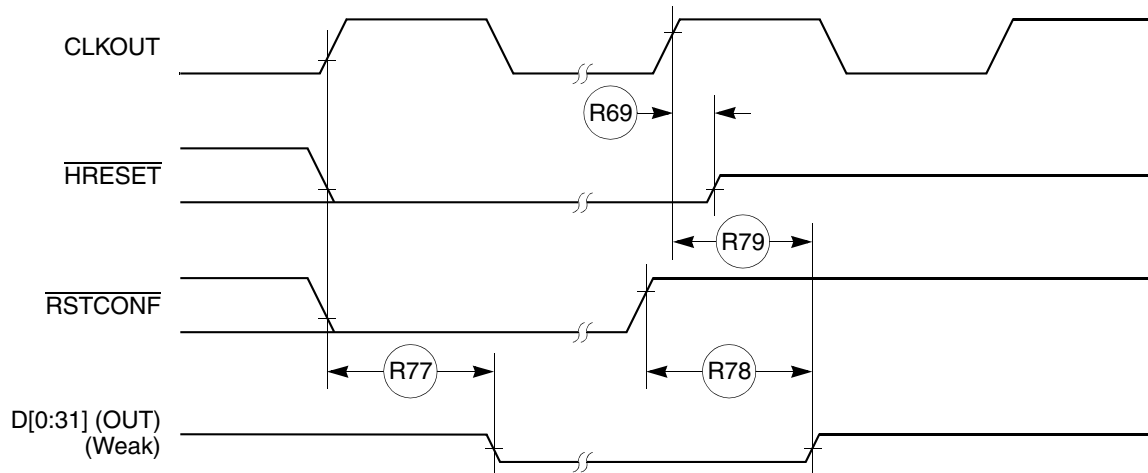
Figure 25. PCMCIA Access Cycle Timing External Bus Read

Figure 32 shows the reset timing for the data bus configuration.



**Figure 32. Reset Timing—Configuration from Data Bus**

Figure 33 provides the reset timing for the data bus weak drive during configuration.



**Figure 33. Reset Timing—Data Bus Weak Drive During Configuration**

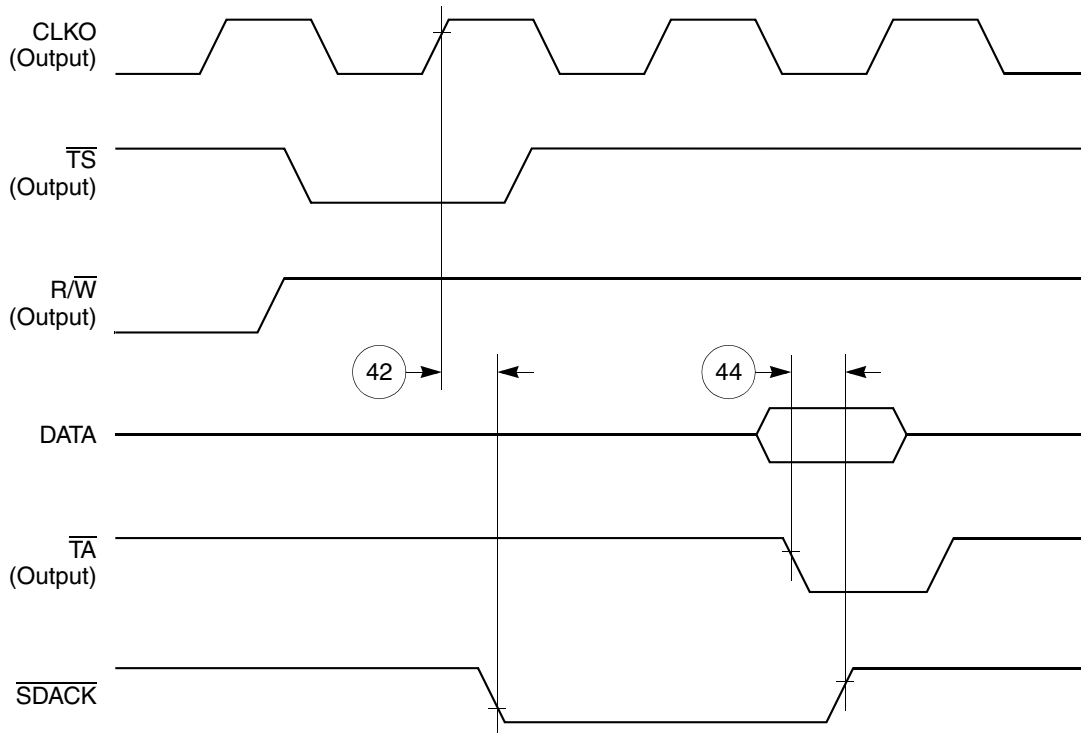


Figure 47.  $\overline{\text{SDACK}}$  Timing Diagram—Peripheral Write, Internally-Generated  $\overline{\text{TA}}$

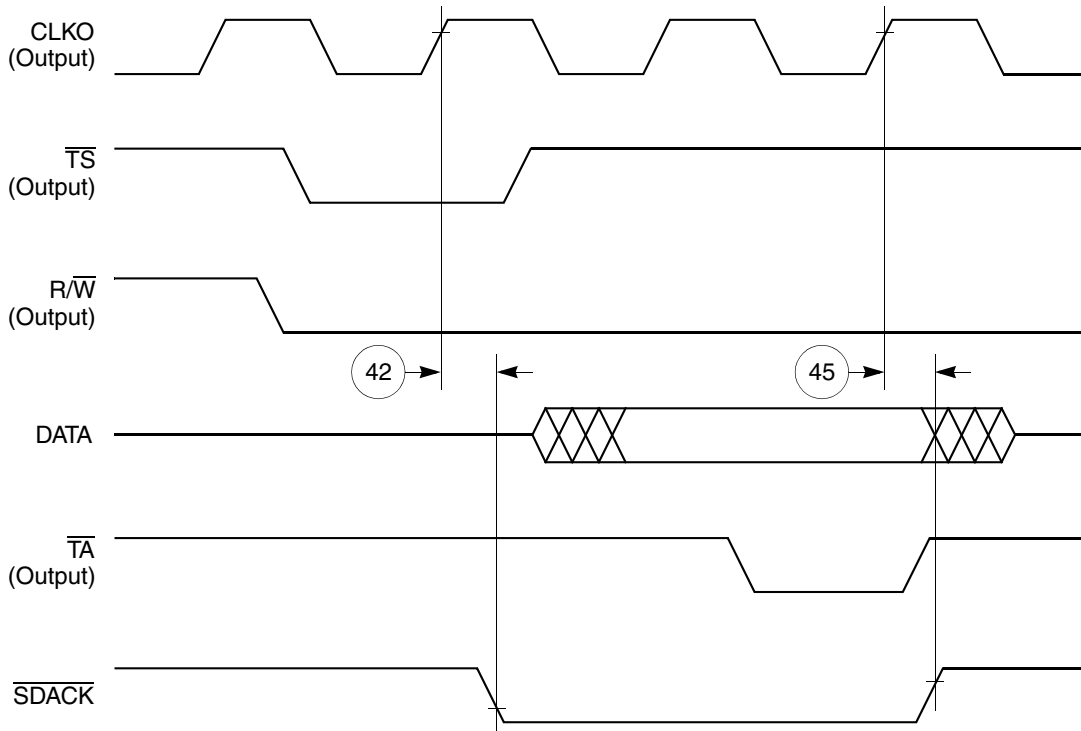


Figure 48.  $\overline{\text{SDACK}}$  Timing Diagram—Peripheral Read, Internally-Generated  $\overline{\text{TA}}$

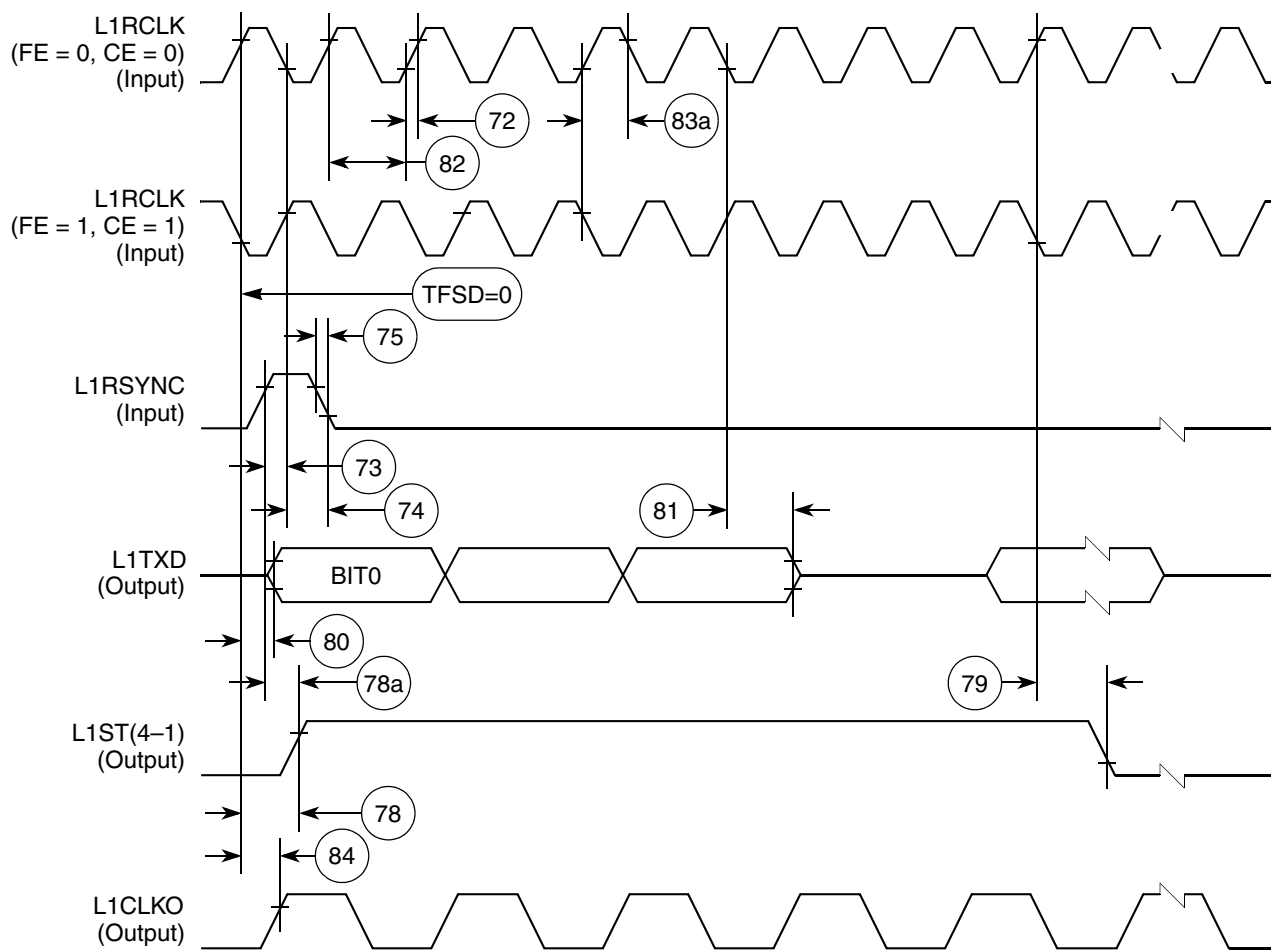


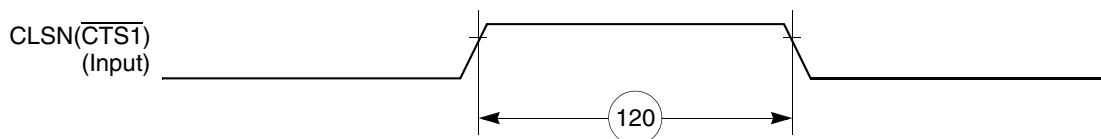
Figure 54. SI Transmit Timing with Double Speed Clocking (DSC = 1)

**Table 22. Ethernet Timing (continued)**

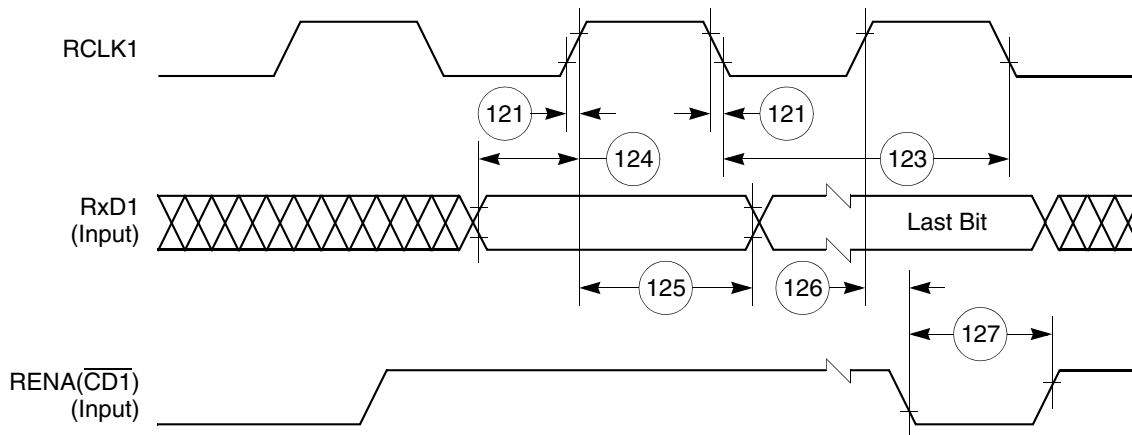
Num	Characteristic	All Frequencies		Unit
		Min	Max	
135	$\overline{\text{RSTRT}}$ active delay (from TCLK1 falling edge)	10	50	ns
136	$\overline{\text{RSTRT}}$ inactive delay (from TCLK1 falling edge)	10	50	ns
137	$\overline{\text{REJECT}}$ width low	1	—	CLK
138	CLKO1 low to $\overline{\text{SDACK}}$ asserted <sup>2</sup>	—	20	ns
139	CLKO1 low to $\overline{\text{SDACK}}$ negated <sup>2</sup>	—	20	ns

<sup>1</sup> The ratios SYNCCLK/RCLK1 and SYNCCLK/TCLK1 must be greater than or equal to 2/1.

<sup>2</sup>  $\overline{\text{SDACK}}$  is asserted whenever the SDMA writes the incoming frame DA into memory.

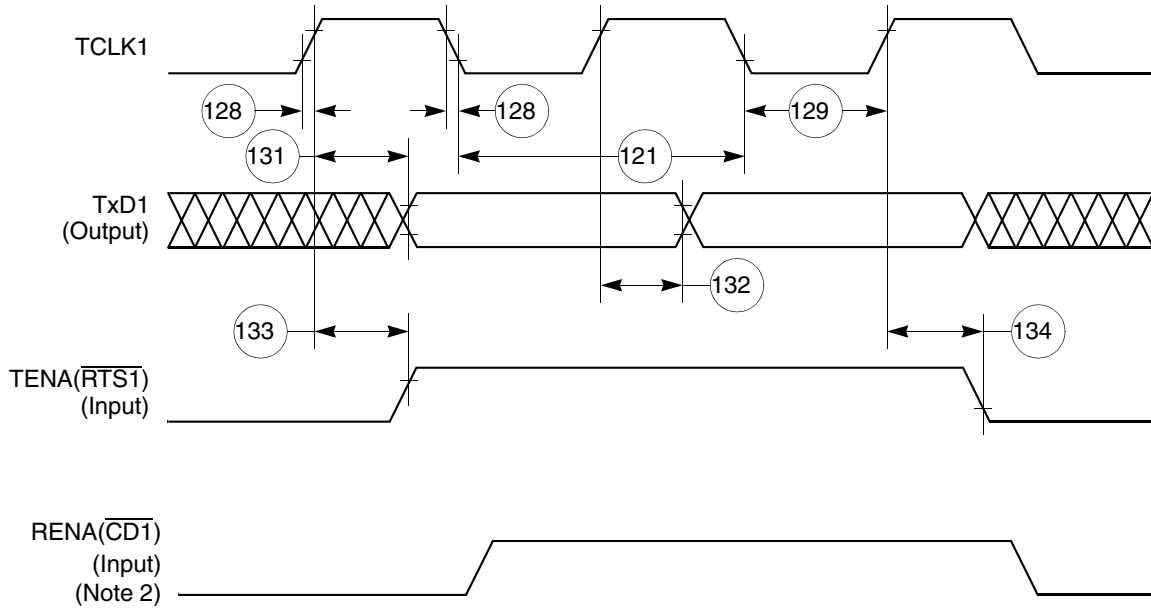


**Figure 59. Ethernet Collision Timing Diagram**



**Figure 60. Ethernet Receive Timing Diagram**

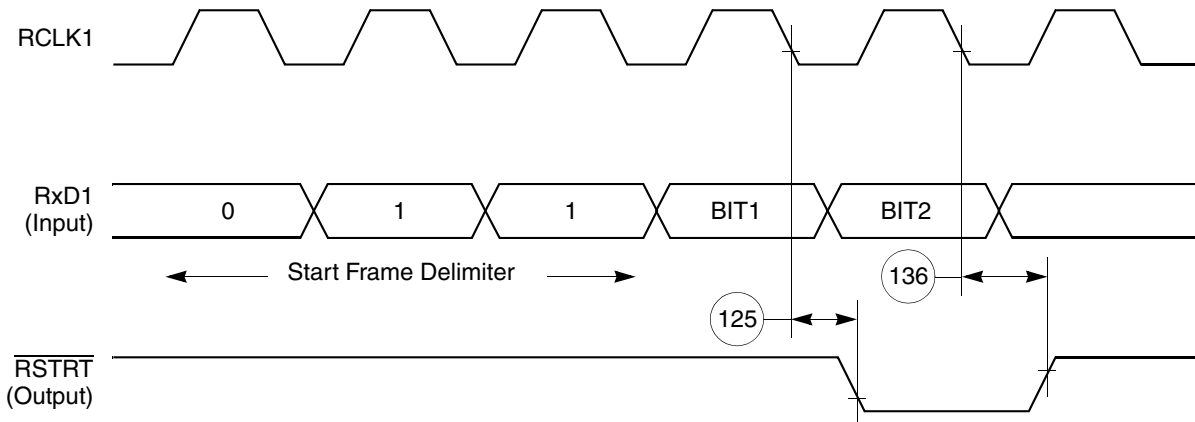




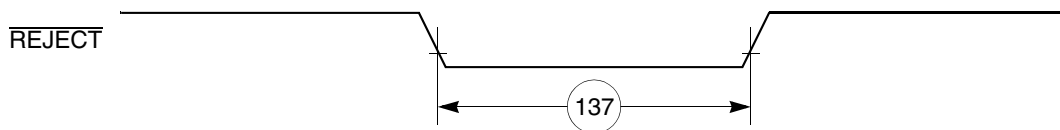
**Notes:**

1. Transmit clock invert (TCI) bit in GSMR is set.
2. If RENA is deasserted before TENA, or RENA is not asserted at all during transmit, then the CSL bit is set in the buffer descriptor at the end of the frame transmission.

**Figure 61. Ethernet Transmit Timing Diagram**



**Figure 62. CAM Interface Receive Start Timing Diagram**



**Figure 63. CAM Interface  $\overline{\text{REJECT}}$  Timing Diagram**

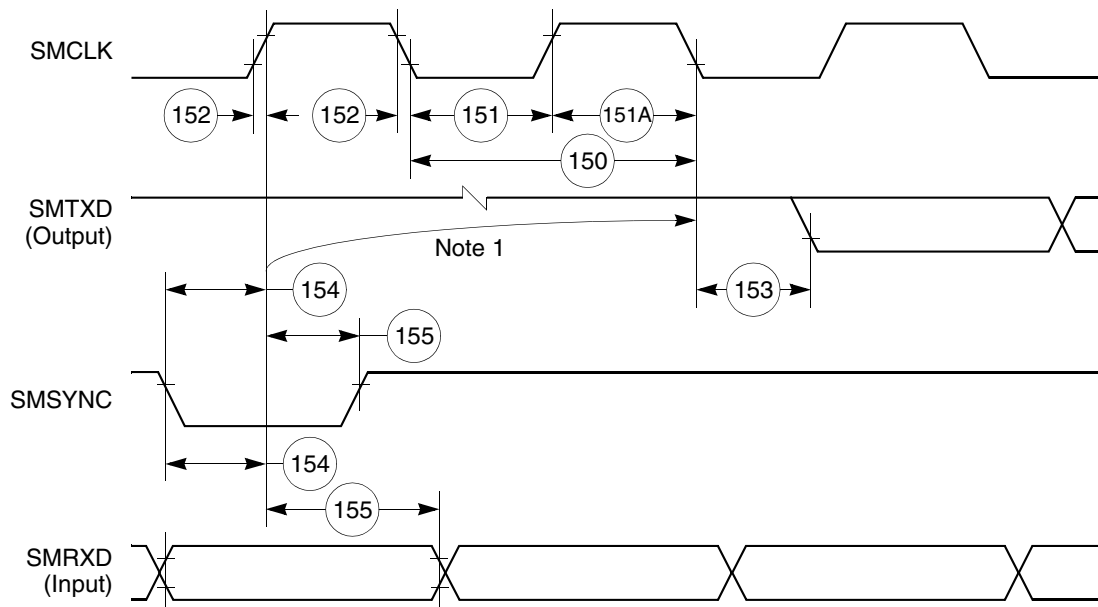
## 11.9 SMC Transparent AC Electrical Specifications

Table 23 provides the SMC transparent timings as shown in Figure 64.

Table 23. SMC Transparent Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
150	SMCLK clock period <sup>1</sup>	100	—	ns
151	SMCLK width low	50	—	ns
151A	SMCLK width high	50	—	ns
152	SMCLK rise/fall time	—	15	ns
153	SMTXD active delay (from SMCLK falling edge)	10	50	ns
154	SMRXD/SMSYNC setup time	20	—	ns
155	RXD1/SMSYNC hold time	5	—	ns

<sup>1</sup> SYNCCLK must be at least twice as fast as SMCLK.



**Note:**

1. This delay is equal to an integer number of character-length clocks.

Figure 64. SMC Transparent Timing Diagram

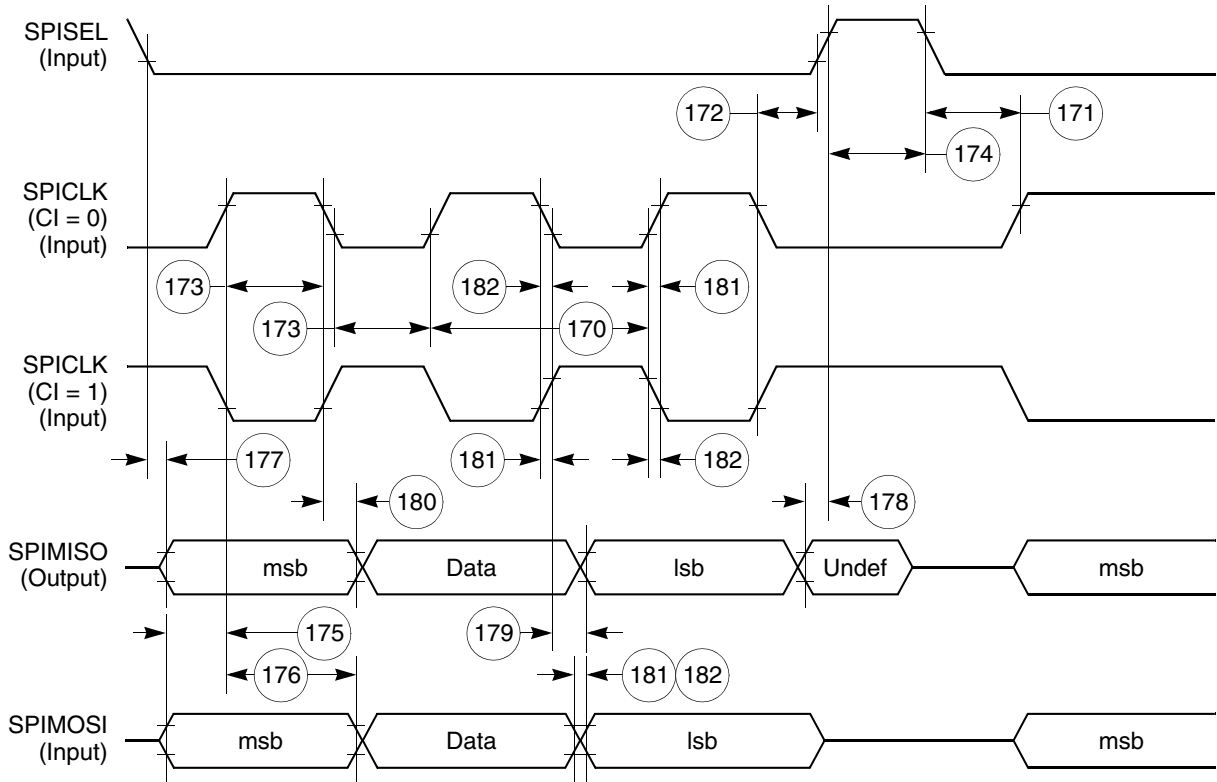


Figure 67. SPI Slave (CP = 0) Timing Diagram

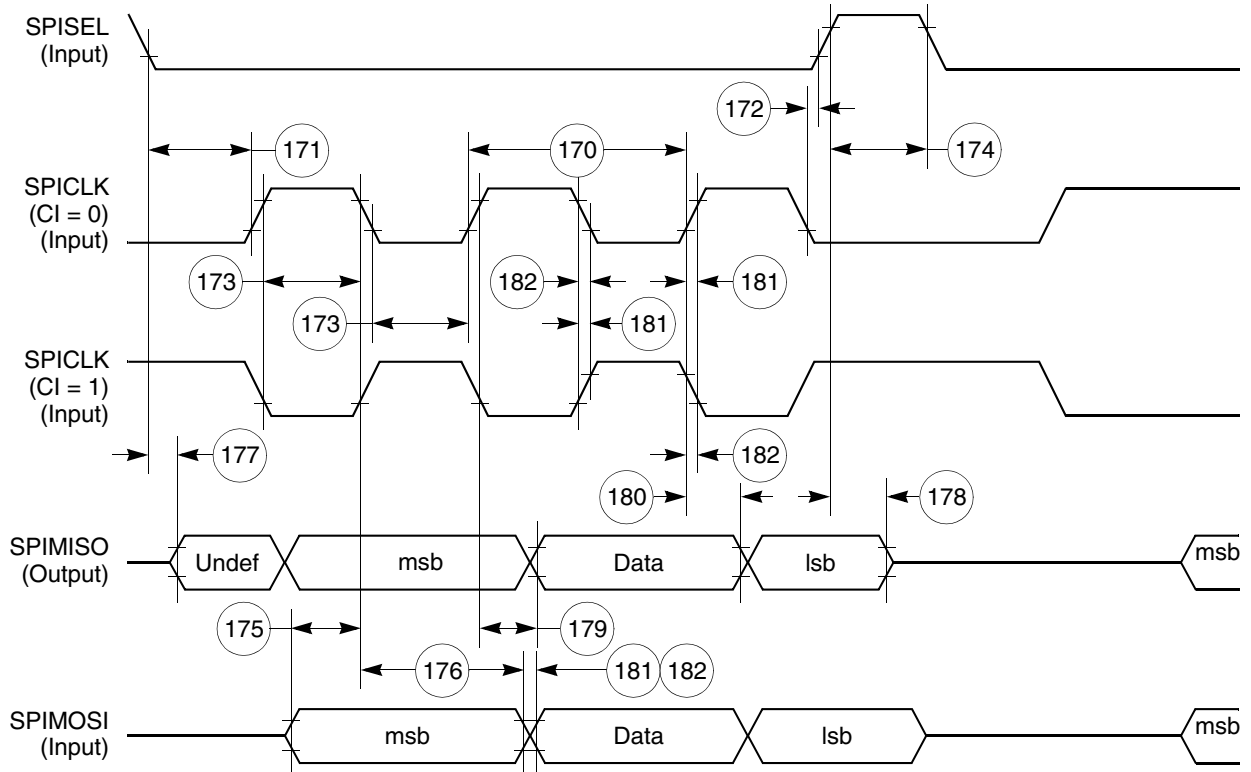


Figure 68. SPI Slave (CP = 1) Timing Diagram

Figure 70 shows signal timings during UTOPIA receive operations.

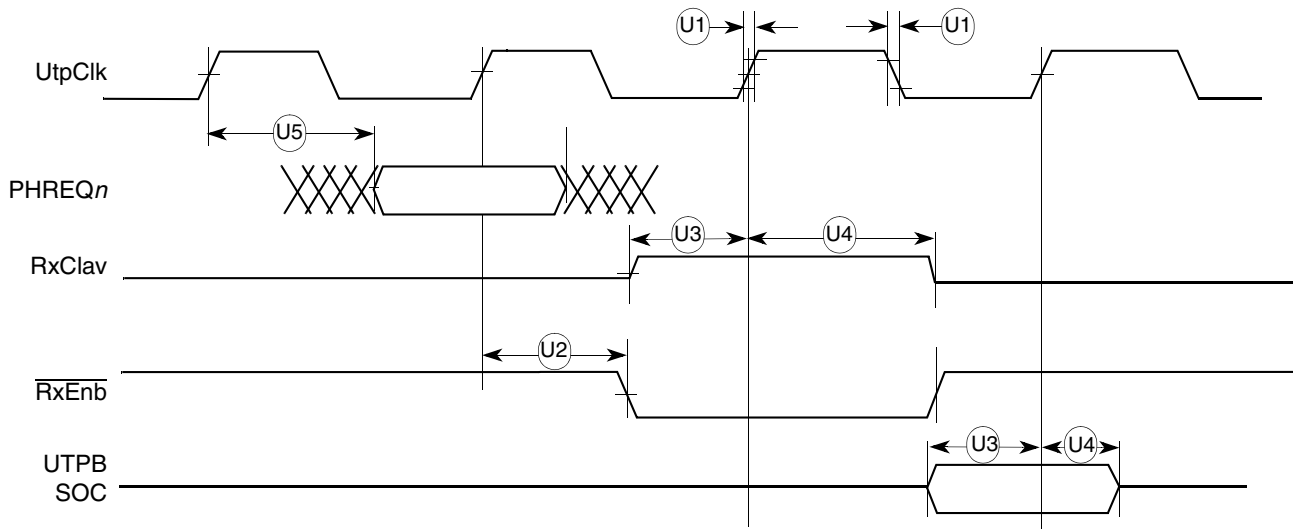


Figure 70. UTOPIA Receive Timing

Figure 71 shows signal timings during UTOPIA transmit operations.

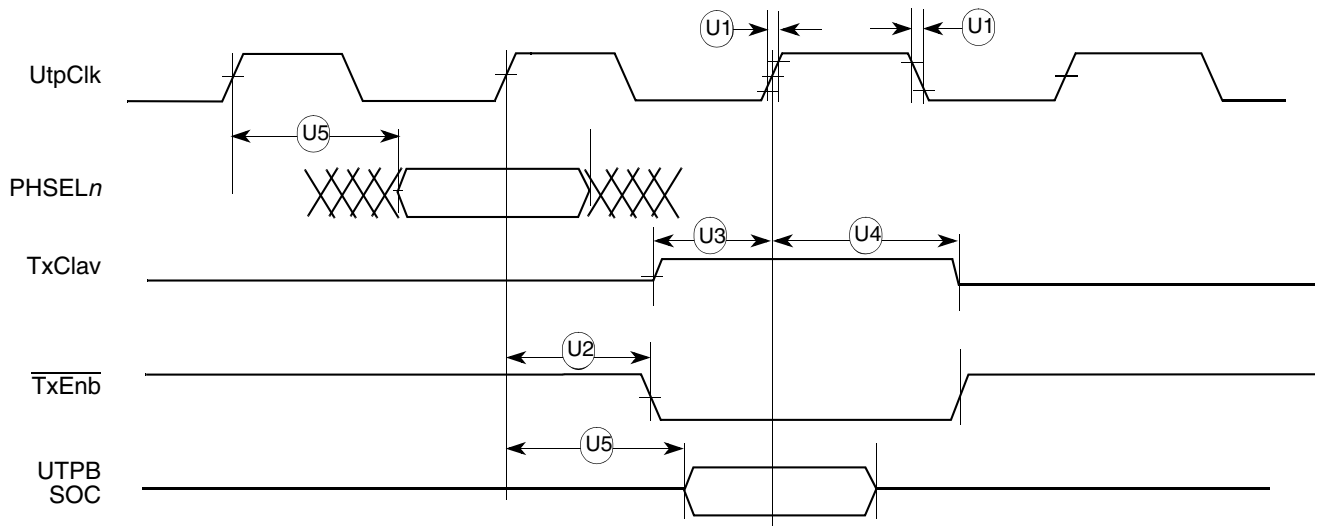


Figure 71. UTOPIA Transmit Timing

# 15 Document Revision History

Table 35 lists significant changes between revisions of this hardware specification.

**Table 35. Document Revision History**

Revision	Date	Changes
10	09/2015	In <a href="#">Table 34</a> , moved MPC855TCVR50D4 and MPC855TCVR66D4 under the extended temperature (–40° to 95°C) and removed MC860ENCVR50D4R2 from the normal temperature Tape and Reel.
9	10/2011	Updated orderable part numbers in <a href="#">Table 34</a> , “MPC860 Family Package/Frequency Availability.”
8	08/2007	<ul style="list-style-type: none"> <li>• Updated template.</li> <li>• On page 1, added a second paragraph.</li> <li>• After <a href="#">Table 2</a>, inserted a new figure showing the undershoot/overshoot voltage (<a href="#">Figure 1</a>) and renumbered the rest of the figures.</li> <li>• In <a href="#">Figure 3</a>, changed all reference voltage measurement points from 0.2 and 0.8 V to 50% level.</li> <li>• In <a href="#">Table 16</a>, changed num 46 description to read, “<math>\overline{TA}</math> assertion to rising edge ...”</li> <li>• In <a href="#">Figure 46</a>, changed <math>\overline{TA}</math> to reflect the rising edge of the clock.</li> </ul>
7.0	9/2004	<ul style="list-style-type: none"> <li>• Added a tablefootnote to <a href="#">Table 6</a> DC Electrical Specifications about meeting the VIL Max of the I2C Standard</li> <li>• Replaced the thermal characteristics in <a href="#">Table 4</a> by the ZQ package</li> <li>• Add the new parts to the Ordering and Availability Chart in <a href="#">Table 34</a></li> <li>• Added the mechanical spec of the ZQ package in <a href="#">Figure 78</a></li> <li>• Removed all of the old revisions from <a href="#">Table 5</a></li> </ul>
6.3	9/2003	<ul style="list-style-type: none"> <li>• Added Section 11.2 on the Port C interrupt pins</li> <li>• Nontechnical reformatting</li> </ul>
6.2	8/2003	<ul style="list-style-type: none"> <li>• Changed B28a through B28d and B29d to show that TRLX can be 0 or 1</li> <li>• Changed reference documentation to reflect the Rev 2 MPC860 PowerQUICC Family Users Manual</li> <li>• Nontechnical reformatting</li> </ul>
6.1	11/2002	<ul style="list-style-type: none"> <li>• Corrected UTOPIA RXenb* and TXenb* timing values</li> <li>• Changed incorrect usage of Vcc to Vdd</li> <li>• Corrected dual port RAM to 8 Kbytes</li> </ul>
6	10/2002	<ul style="list-style-type: none"> <li>• Added the MPC855T. Corrected <a href="#">Figure 26 on page -36</a>.</li> </ul>
5.1	11/2001	<ul style="list-style-type: none"> <li>• Revised template format, removed references to MAC functionality, changed <a href="#">Table 7</a> B23 max value @ 66 MHz from 2ns to 8ns, added this revision history table</li> </ul>