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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	66MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (2)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 95°C (TA)
Security Features	-
Package / Case	357-BBGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc860decvr66d4

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



2 Features

The following list summarizes the key MPC860 features:

- Embedded single-issue, 32-bit core (implementing the Power Architecture technology) with thirty-two 32-bit general-purpose registers (GPRs)
 - The core performs branch prediction with conditional prefetch without conditional execution.
 - 4- or 8-Kbyte data cache and 4- or 16-Kbyte instruction cache (see Table 1)
 - 16-Kbyte instruction caches are four-way, set-associative with 256 sets; 4-Kbyte instruction caches are two-way, set-associative with 128 sets.
 - 8-Kbyte data caches are two-way, set-associative with 256 sets; 4-Kbyte data caches are two-way, set-associative with 128 sets.
 - Cache coherency for both instruction and data caches is maintained on 128-bit (4-word) cache blocks.
 - Caches are physically addressed, implement a least recently used (LRU) replacement algorithm, and are lockable on a cache block basis.
 - MMUs with 32-entry TLB, fully-associative instruction, and data TLBs
 - MMUs support multiple page sizes of 4-, 16-, and 512-Kbytes, and 8-Mbytes; 16 virtual address spaces and 16 protection groups
 - Advanced on-chip-emulation debug mode
- Up to 32-bit data bus (dynamic bus sizing for 8, 16, and 32 bits)
- 32 address lines
- Operates at up to 80 MHz
- Memory controller (eight banks)
 - Contains complete dynamic RAM (DRAM) controller
 - Each bank can be a chip select or \overline{RAS} to support a DRAM bank.
 - Up to 15 wait states programmable per memory bank
 - Glueless interface to DRAM, SIMMS, SRAM, EPROM, Flash EPROM, and other memory devices
 - DRAM controller programmable to support most size and speed memory interfaces
 - Four $\overline{\text{CAS}}$ lines, four $\overline{\text{WE}}$ lines, and one $\overline{\text{OE}}$ line
 - Boot chip-select available at reset (options for 8-, 16-, or 32-bit memory)
 - Variable block sizes (32 Kbytes to 256 Mbytes)
 - Selectable write protection
 - On-chip bus arbitration logic
- General-purpose timers
 - Four 16-bit timers or two 32-bit timers
 - Gate mode can enable/disable counting
 - Interrupt can be masked on reference match and event capture.



- Up to 8 Kbytes of dual-port RAM
- 16 serial DMA (SDMA) channels
- Three parallel I/O registers with open-drain capability
- Four baud-rate generators (BRGs)
 - Independent (can be tied to any SCC or SMC)
 - Allows changes during operation
 - Autobaud support option
- Four serial communications controllers (SCCs)
 - Ethernet/IEEE 802.3[®] standard optional on SCC1–4, supporting full 10-Mbps operation (available only on specially programmed devices)
 - HDLC/SDLC (all channels supported at 2 Mbps)
 - HDLC bus (implements an HDLC-based local area network (LAN))
 - Asynchronous HDLC to support point-to-point protocol (PPP)
 - AppleTalk
 - Universal asynchronous receiver transmitter (UART)
 - Synchronous UART
 - Serial infrared (IrDA)
 - Binary synchronous communication (BISYNC)
 - Totally transparent (bit streams)
 - Totally transparent (frame-based with optional cyclic redundancy check (CRC))
- Two SMCs (serial management channels)
 - UART
 - Transparent
 - General circuit interface (GCI) controller
 - Can be connected to the time-division multiplexed (TDM) channels
- One SPI (serial peripheral interface)
 - Supports master and slave modes
 - Supports multimaster operation on the same bus
- One I²C (inter-integrated circuit) port
 - Supports master and slave modes
 - Multiple-master environment support
- Time-slot assigner (TSA)
 - Allows SCCs and SMCs to run in multiplexed and/or non-multiplexed operation
 - Supports T1, CEPT, PCM highway, ISDN basic rate, ISDN primary rate, user defined
 - 1- or 8-bit resolution
 - Allows independent transmit and receive routing, frame synchronization, and clocking



Table 4 shows the thermal characteristics for the MPC860.

Table 4. MPC860 Thermal Resistance Data

Rating	Env	Symbol	ZP MPC860P	ZQ / VR MPC860P	Unit	
Mold Compound Thicknes		0.85	1.15	mm		
Junction-to-ambient ¹	Natural convection	Single-layer board (1s)	$R_{\theta JA}^2$	34	34	°C/W
		Four-layer board (2s2p)	$R_{\theta JMA}^{3}$	22	22	
	Airflow (200 ft/min)	Single-layer board (1s)	$R_{\theta JMA}^{3}$	27	27	
		Four-layer board (2s2p)	$R_{\theta JMA}^{3}$	18	18	
Junction-to-board ⁴			$R_{\theta JB}$	14	13	
Junction-to-case ⁵			R_{\thetaJC}	6	8	
Junction-to-package top ⁶	Natural convection		Ψ_{JT}	2	2	

¹ Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.

² Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.

³ Per JEDEC JESD51-6 with the board horizontal.

⁴ Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

- ⁵ Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature. For exposed pad packages where the pad would be expected to be soldered, junction-to-case thermal resistance is a simulated value from the junction to the exposed pad without contact resistance.
- ⁶ Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2.



Power Dissipation

5 **Power Dissipation**

Table 5 provides power dissipation information. The modes are 1:1, where CPU and bus speeds are equal, and 2:1, where CPU frequency is twice the bus speed.

Die Revision	Frequency (MHz)	Typical ¹	Maximum ²	Unit
D.4	50	656	735	mW
(1:1 mode)	66	TBD	TBD	mW
D.4	66	722	762	mW
(2:1 mode)	80	851	909	mW

Table 5. Power Dissipation (PD)

¹ Typical power dissipation is measured at 3.3 V.

² Maximum power dissipation is measured at 3.5 V.

NOTE

Values in Table 5 represent V_{DDL} -based power dissipation and do not include I/O power dissipation over V_{DDH} . I/O power dissipation varies widely by application due to buffer current, depending on external circuitry.

6 DC Characteristics

Table 6 provides the DC electrical characteristics for the MPC860.

 Table 6. DC Electrical Specifications

Characteristic	Symbol	Min	Мах	Unit
Operating voltage at 40 MHz or less	V _{DDH} , V _{DDL} , V _{DDSYN}	3.0	3.6	V
	KAPWR (power-down mode)	2.0	3.6	V
	KAPWR (all other operating modes)	V _{DDH} – 0.4	V _{DDH}	V
Operating voltage greater than 40 MHz	V _{DDH} , V _{DDL} , KAPWR, V _{DDSYN}	3.135	3.465	V
	KAPWR (power-down mode)	2.0	3.6	V
	KAPWR (all other operating modes)	V _{DDH} – 0.4	V _{DDH}	V
Input high voltage (all inputs except EXTAL and EXTCLK)	V _{IH}	2.0	5.5	V
Input low voltage ¹	V _{IL}	GND	0.8	V
EXTAL, EXTCLK input high voltage	V _{IHC}	$0.7 imes (V_{DDH})$	V _{DDH} + 0.3	V
Input leakage current, $V_{in} = 5.5 \text{ V}$ (except TMS, TRST, DSCK, and DSDI pins)	l _{in}	—	100	μA



Thermal Calculation and Measurement

7 Thermal Calculation and Measurement

For the following discussions, $P_D = (V_{DD} \times I_{DD}) + PI/O$, where PI/O is the power dissipation of the I/O drivers.

7.1 Estimation with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J, in °C can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

 T_A = ambient temperature (°C)

 $R_{\theta JA}$ = package junction-to-ambient thermal resistance (°C/W)

 P_D = power dissipation in package

The junction-to-ambient thermal resistance is an industry standard value which provides a quick and easy estimation of thermal performance. However, the answer is only an estimate; test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

7.2 Estimation with Junction-to-Case Thermal Resistance

Historically, the thermal resistance has frequently been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

 $R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

where:

 $R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

 $R_{\theta IC}$ = junction-to-case thermal resistance (°C/W)

 $R_{\theta CA}$ = case-to-ambient thermal resistance (°C/W)

 $R_{\theta JC}$ is device related and cannot be influenced by the user. The user adjusts the thermal environment to affect the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the airflow around the device, add a heat sink, change the mounting arrangement on the printed-circuit board, or change the thermal dissipation on the printed-circuit board surrounding the device. This thermal model is most useful for ceramic packages with heat sinks where some 90% of the heat flows through the case and the heat sink to the ambient environment. For most packages, a better model is required.

7.3 Estimation with Junction-to-Board Thermal Resistance

A simple package thermal model which has demonstrated reasonable accuracy (about 20%) is a two-resistor model consisting of a junction-to-board and a junction-to-case thermal resistance. The junction-to-case thermal resistance covers the situation where a heat sink is used or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed-circuit board. It has been observed that the thermal performance of most plastic packages, especially PBGA packages, is strongly dependent on the board temperature; see Figure 2.



Thermal Calculation and Measurement



Figure 2. Effect of Board Temperature Rise on Thermal Behavior

If the board temperature is known, an estimate of the junction temperature in the environment can be made using the following equation:

$$T_{J} = T_{B} + (R_{\theta JB} \times P_{D})$$

where:

 $R_{\theta JB}$ = junction-to-board thermal resistance (°C/W)

 $T_B = board temperature (°C)$

 P_D = power dissipation in package

If the board temperature is known and the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. For this method to work, the board and board mounting must be similar to the test board used to determine the junction-to-board thermal resistance, namely a 2s2p (board with a power and a ground plane) and by attaching the thermal balls to the ground plane.

7.4 Estimation Using Simulation

When the board temperature is not known, a thermal simulation of the application is needed. The simple two-resistor model can be used with the thermal simulation of the application [2], or a more accurate and complex model of the package can be used in the thermal simulation.

7.5 Experimental Determination

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$



Layout Practices

where:

 Ψ_{JT} = thermal characterization parameter

 T_T = thermocouple temperature on top of package

 P_D = power dissipation in package

The thermal characterization parameter is measured per JEDEC JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

7.6 References

Semiconductor Equipment and Materials International	(415) 964-5111
805 East Middlefield Rd.	
Mountain View, CA 94043	
MIL-SPEC and EIA/JESD (JEDEC) Specifications	800-854-7179 or
(Available from Global Engineering Documents)	303-397-7956
JEDEC Specifications	http://www.jedec.org

- 1. C.E. Triplett and B. Joiner, "An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module," Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.
- B. Joiner and V. Adams, "Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling," Proceedings of SemiTherm, San Diego, 1999, pp. 212–220.

8 Layout Practices

Each V_{DD} pin on the MPC860 should be provided with a low-impedance path to the board's supply. Each GND pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on the chip. The V_{DD} power supply should be bypassed to ground using at least four 0.1 µF-bypass capacitors located as close as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to chip V_{DD} and GND should be kept to less than half an inch per capacitor lead. A four-layer board employing two inner layers as V_{CC} and GND planes is recommended.

All output pins on the MPC860 have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized in order to minimize undershoot and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data buses. Maximum PC trace lengths of 6 inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the V_{CC} and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.



		33 MHz		40 MHz		50 MHz		66 MHz		
Num	Characteristic	Min	Max	Min	Max	Min	Max	Min	Max	Unit
B31a	CLKOUT falling edge to CS valid—as requested by control bit CST1 in the corresponding word in UPM	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.54	ns
B31b	CLKOUT rising edge to \overline{CS} valid—as requested by control bit CST2 in the corresponding word in UPM	1.50	8.00	1.50	8.00	1.50	8.00	1.50	8.00	ns
B31c	CLKOUT rising edge to $\overline{\text{CS}}$ valid—as requested by control bit CST3 in the corresponding word in UPM	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.04	ns
B31d	CLKOUT falling edge to \overline{CS} valid—as requested by control bit CST1 in the corresponding word in UPM, EBDF = 1	13.26	17.99	11.28	16.00	9.40	14.13	7.58	12.31	ns
B32	CLKOUT falling edge to BS valid—as requested by control bit BST4 in the corresponding word in UPM	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns
B32a	CLKOUT falling edge to \overline{BS} valid—as requested by control bit BST1 in the corresponding word in UPM, EBDF = 0	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.54	ns
B32b	CLKOUT rising edge to $\overline{\text{BS}}$ valid—as requested by control bit BST2 in the corresponding word in UPM	1.50	8.00	1.50	8.00	1.50	8.00	1.50	8.00	ns
B32c	CLKOUT rising edge to $\overline{\text{BS}}$ valid—as requested by control bit BST3 in the corresponding word in UPM	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.54	ns
B32d	CLKOUT falling edge to \overline{BS} valid—as requested by control bit BST1 in the corresponding word in UPM, EBDF = 1	13.26	17.99	11.28	16.00	9.40	14.13	7.58	12.31	ns
B33	CLKOUT falling edge to GPL valid—as requested by control bit GxT4 in the corresponding word in UPM	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns
B33a	CLKOUT rising edge to GPL valid—as requested by control bit GxT3 in the corresponding word in UPM	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.54	ns
B34	A(0:31), BADDR(28:30), and D(0:31) to \overline{CS} valid—as requested by control bit CST4 in the corresponding word in UPM	5.58	—	4.25	—	3.00	—	1.79	—	ns
B34a	A(0:31), BADDR(28:30), and D(0:31) to \overline{CS} valid—as requested by control bit CST1 in the corresponding word in UPM	13.15		10.50		8.00		5.58	_	ns
B34b	A(0:31), BADDR(28:30), and D(0:31) to \overline{CS} valid—as requested by control bit CST2 in the corresponding word in UPM	20.73	_	16.75		13.00		9.36	_	ns

Table 7. Bus Operation Timings (continued)



Bus Signal Timing

	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
NUM	Characteristic	Min	Max	Min	Max	Min	Max	Min	Max	Unit
B35	A(0:31), BADDR(28:30) to \overline{CS} valid—as requested by control bit BST4 in the corresponding word in UPM	5.58	_	4.25	_	3.00	_	1.79	_	ns
B35a	A(0:31), BADDR(28:30), and D(0:31) to $\overline{\text{BS}}$ valid—as requested by control bit BST1 in the corresponding word in UPM	13.15	—	10.50	—	8.00	—	5.58	_	ns
B35b	A(0:31), BADDR(28:30), and D(0:31) to $\overline{\text{BS}}$ valid—as requested by control bit BST2 in the corresponding word in UPM	20.73	—	16.75	—	13.00	—	9.36		ns
B36	A(0:31), BADDR(28:30), and D(0:31) to GPL valid—as requested by control bit GxT4 in the corresponding word in UPM	5.58	—	4.25	—	3.00	—	1.79	_	ns
B37	UPWAIT valid to CLKOUT falling edge ⁹	6.00	—	6.00	—	6.00	—	6.00		ns
B38	CLKOUT falling edge to UPWAIT valid ⁹	1.00	—	1.00	_	1.00	_	1.00	_	ns
B39	AS valid to CLKOUT rising edge ¹⁰	7.00	_	7.00	_	7.00	_	7.00	_	ns
B40	A(0:31), TSIZ(0:1), RD/WR, BURST, valid to CLKOUT rising edge	7.00	—	7.00	—	7.00	—	7.00	_	ns
B41	$\overline{\text{TS}}$ valid to CLKOUT rising edge (setup time)	7.00	—	7.00	_	7.00	_	7.00	_	ns
B42	CLKOUT rising edge to \overline{TS} valid (hold time)	2.00	—	2.00	—	2.00	—	2.00	_	ns
B43	AS negation to memory controller signals negation	_	TBD	_	TBD	_	TBD	_	TBD	ns

¹ Phase and frequency jitter performance results are only valid if the input jitter is less than the prescribed value.

² If the rate of change of the frequency of EXTAL is slow (that is, it does not jump between the minimum and maximum values in one cycle) or the frequency of the jitter is fast (that is, it does not stay at an extreme value for a long time) then the maximum allowed jitter on EXTAL can be up to 2%.

³ The timings specified in B4 and B5 are based on full strength clock.

⁴ The timing for BR output is relevant when the MPC860 is selected to work with external bus arbiter. The timing for BG output is relevant when the MPC860 is selected to work with internal bus arbiter.

⁵ The timing required for BR input is relevant when the MPC860 is selected to work with internal bus arbiter. The timing for BG input is relevant when the MPC860 is selected to work with external bus arbiter.

⁶ The D(0:31) and DP(0:3) input timings B18 and B19 refer to the rising edge of the CLKOUT in which the TA input signal is asserted.

⁷ The D(0:31) and DP(0:3) input timings B20 and B21 refer to the falling edge of the CLKOUT. This timing is valid only for read accesses controlled by chip-selects under control of the UPM in the memory controller, for data beats where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

⁸ The timing B30 refers to \overline{CS} when ACS = 00 and to $\overline{WE}(0:3)$ when CSNT = 0.

⁹ The signal UPWAIT is considered asynchronous to the CLKOUT and synchronized internally. The timings specified in B37 and B38 are specified to enable the freeze of the UPM output signals as described in Figure 18.

¹⁰ The AS signal is considered asynchronous to the CLKOUT. The timing B39 is specified in order to allow the behavior specified in Figure 21.







Figure 16. External Bus Write Timing (GPCM Controlled—TRLX = 0 or 1, CSNT = 1)



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Table 8 provides interrupt timing for the MPC860.

Table 8. Interrupt Timing

Num	Characteristic1	All Freq	Unit	
	Characteristic	Min	Мах	Onit
139	IRQx valid to CLKOUT rising edge (setup time)	6.00	_	ns
140	IRQx hold time after CLKOUT	2.00	_	ns
141	IRQx pulse width low	3.00	—	ns
142	IRQx pulse width high	3.00	_	ns
143	IRQx edge-to-edge time	$4 \times T_{CLOCKOUT}$	—	—

The timings I39 and I40 describe the testing conditions under which the IRQ lines are tested when being defined as level-sensitive. The IRQ lines are synchronized internally and do not have to be asserted or negated with reference to the CLKOUT.

The timings I41, I42, and I43 are specified to allow the correct function of the IRQ lines detection circuitry and have no direct relation with the total system interrupt latency that the MPC860 is able to support.

Figure 23 provides the interrupt detection timing for the external level-sensitive lines.



Figure 23. Interrupt Detection Timing for External Level Sensitive Lines

Figure 24 provides the interrupt detection timing for the external edge-sensitive lines.



Figure 24. Interrupt Detection Timing for External Edge Sensitive Lines



Table 10 shows the PCMCIA port timing for the MPC860.

Table 10. PCMCIA Port Timing

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Unit
P57	CLKOUT to OPx valid	—	19.00	—	19.00	_	19.00	_	19.00	ns
P58	HRESET negated to OPx drive ¹	25.73	—	21.75	—	18.00	—	14.36	—	ns
P59	IP_Xx valid to CLKOUT rising edge	5.00	—	5.00	—	5.00	—	5.00	—	ns
P60	CLKOUT rising edge to IP_Xx invalid	1.00	—	1.00	—	1.00	—	1.00	—	ns

¹ OP2 and OP3 only.

Figure 28 provides the PCMCIA output port timing for the MPC860.



Figure 28. PCMCIA Output Port Timing

Figure 29 provides the PCMCIA output port timing for the MPC860.



Figure 29. PCMCIA Input Port Timing





Figure 42. PIP TX (Pulse Mode) Timing Diagram



11.4 Baud Rate Generator AC Electrical Specifications

Table 17 provides the baud rate generator timings as shown in Figure 49.

Table 17. Baud Rate Generator Timing

Num	Charactariatia	All Freq	Unit	
	Characteristic	Min	Мах	Unit
50	BRGO rise and fall time	—	10	ns
51	BRGO duty cycle	40	60	%
52	BRGO cycle	40	—	ns



Figure 49. Baud Rate Generator Timing Diagram

11.5 Timer AC Electrical Specifications

Table 18 provides the general-purpose timer timings as shown in Figure 50.

Table 18. Timer Timing

Num	Characteristic	All Freq	Unit	
	Characteristic	Min	Мах	Unit
61	TIN/TGATE rise and fall time	10	—	ns
62	TIN/TGATE low time	1	—	CLK
63	TIN/TGATE high time	2	—	CLK
64	TIN/TGATE cycle time	3	—	CLK
65	CLKO low to TOUT valid	3	25	ns





Figure 50. CPM General-Purpose Timers Timing Diagram

11.6 Serial Interface AC Electrical Specifications

Table 19 provides the serial interface timings as shown in Figure 51 through Figure 55.

Num	Ohana sharia ta	All Frequencies		11
	Characteristic	Min Ma	Max	
70	L1RCLK, L1TCLK frequency (DSC = 0) ^{1, 2}		SYNCCLK/2.5	MHz
71	L1RCLK, L1TCLK width low $(DSC = 0)^2$	P + 10	—	ns
71a	L1RCLK, L1TCLK width high $(DSC = 0)^3$	P + 10	—	ns
72	L1TXD, L1ST(1–4), L1RQ, L1CLKO rise/fall time	—	15.00	ns
73	L1RSYNC, L1TSYNC valid to L1CLK edge (SYNC setup time)	20.00	—	ns
74	L1CLK edge to L1RSYNC, L1TSYNC, invalid (SYNC hold time)	35.00	—	ns
75	L1RSYNC, L1TSYNC rise/fall time	—	15.00	ns
76	L1RXD valid to L1CLK edge (L1RXD setup time)	17.00	—	ns
77	L1CLK edge to L1RXD invalid (L1RXD hold time)	13.00	—	ns
78	L1CLK edge to L1ST(1-4) valid ⁴	10.00	45.00	ns
78A	L1SYNC valid to L1ST(1-4) valid	10.00	45.00	ns
79	L1CLK edge to L1ST(1-4) invalid	10.00	45.00	ns
80	L1CLK edge to L1TXD valid	10.00	55.00	ns
80A	L1TSYNC valid to L1TXD valid ⁴	10.00	55.00	ns
81	L1CLK edge to L1TXD high impedance	0.00	42.00	ns
82	L1RCLK, L1TCLK frequency (DSC =1)	—	16.00 or SYNCCLK/2	MHz
83	L1RCLK, L1TCLK width low (DSC = 1)	P + 10	_	ns
83a	L1RCLK, L1TCLK width high $(DSC = 1)^3$	P + 10	—	ns

Table 19. SI Timing



CPM Electrical Characteristics





CPM Electrical Characteristics





11.10 SPI Master AC Electrical Specifications

Table 24 provides the SPI master timings as shown in Figure 65 and Figure 66.

Table 24. SPI Master Timing

Num	Characteristic	All Frequencies		11
		Min	Мах	
160	MASTER cycle time	4	1024	t _{cyc}
161	MASTER clock (SCK) high or low time	2	512	t _{cyc}
162	MASTER data setup time (inputs)	50	_	ns
163	Master data hold time (inputs)	0	—	ns
164	Master data valid (after SCK edge)	—	20	ns
165	Master data hold time (outputs)	0	_	ns
166	Rise time output	—	15	ns
167	Fall time output	—	15	ns





11.12 I²C AC Electrical Specifications

Table 26 provides the I^2C (SCL < 100 kHz) timings.

Table 26. I²C Timing (SCL < 100 kHz)

Num	Characteristic	All Frequencies		Unit
		Min	Мах	Unit
200	SCL clock frequency (slave)	0	100	kHz
200	SCL clock frequency (master) ¹	1.5	100	kHz
202	Bus free time between transmissions	4.7	—	μS
203	Low period of SCL	4.7	—	μS
204	High period of SCL	4.0	—	μS
205	Start condition setup time	4.7	—	μS
206	Start condition hold time	4.0	—	μS
207	Data hold time	0	—	μS
208	Data setup time	250	—	ns
209	SDL/SCL rise time	—	1	μS
210	SDL/SCL fall time	—	300	ns
211	Stop condition setup time	4.7	—	μS

SCL frequency is given by SCL = BRGCLK_frequency / ((BRG register + 3 × pre_scaler × 2). The ratio SYNCCLK/(BRGCLK/pre_scaler) must be greater than or equal to 4/1.

Table 27 provides the I^2C (SCL > 100 kHz) timings.

Table 27. . I²C Timing (SCL > 100 kHz)

Num	Characteristic	Expression	All Frequencies		Unit
			Min	Мах	Unit
200	SCL clock frequency (slave)	fSCL	0	BRGCLK/48	Hz
200	SCL clock frequency (master) ¹	fSCL	BRGCLK/16512	BRGCLK/48	Hz
202	Bus free time between transmissions		1/(2.2 * fSCL)	—	S
203	Low period of SCL		1/(2.2 * fSCL)	—	S
204	High period of SCL		1/(2.2 * fSCL)	—	S
205	Start condition setup time		1/(2.2 * fSCL)	—	S
206	Start condition hold time		1/(2.2 * fSCL)	—	S
207	Data hold time		0	—	S
208	Data setup time		1/(40 * fSCL)	—	S
209	SDL/SCL rise time		—	1/(10 * fSCL)	S
210	SDL/SCL fall time		—	1/(33 * fSCL)	S
211	Stop condition setup time		1/2(2.2 * fSCL)	—	s

SCL frequency is given by SCL = BRGCLK_frequency / ((BRG register + 3) × pre_scaler × 2). The ratio SYNCCLK/(BRGCLK / pre_scaler) must be greater than or equal to 4/1.



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