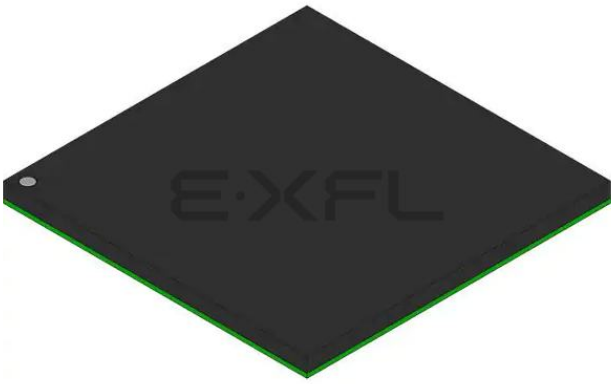

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	50MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (2)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 95°C (TA)
Security Features	-
Package / Case	357-BBGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc860deczq50d4

- System integration unit (SIU)
  - Bus monitor
  - Software watchdog
  - Periodic interrupt timer (PIT)
  - Low-power stop mode
  - Clock synthesizer
  - Decrementer, time base, and real-time clock (RTC)
  - Reset controller
  - IEEE 1149.1™ Std. test access port (JTAG)
- Interrupts
  - Seven external interrupt request (IRQ) lines
  - 12 port pins with interrupt capability
  - 23 internal interrupt sources
  - Programmable priority between SCCs
  - Programmable highest priority request
- 10/100 Mbps Ethernet support, fully compliant with the IEEE 802.3u® Standard (not available when using ATM over UTOPIA interface)
- ATM support compliant with ATM forum UNI 4.0 specification
  - Cell processing up to 50–70 Mbps at 50-MHz system clock
  - Cell multiplexing/demultiplexing
  - Support of AAL5 and AAL0 protocols on a per-VC basis. AAL0 support enables OAM and software implementation of other protocols.
  - ATM pace control (APC) scheduler, providing direct support for constant bit rate (CBR) and unspecified bit rate (UBR) and providing control mechanisms enabling software support of available bit rate (ABR)
  - Physical interface support for UTOPIA (10/100-Mbps is not supported with this interface) and byte-aligned serial (for example, T1/E1/ADSL)
  - UTOPIA-mode ATM supports level-1 master with cell-level handshake, multi-PHY (up to four physical layer devices), connection to 25-, 51-, or 155-Mbps framers, and UTOPIA/system clock ratios of 1/2 or 1/3.
  - Serial-mode ATM connection supports transmission convergence (TC) function for T1/E1/ADSL lines, cell delineation, cell payload scrambling/descrambling, automatic idle/unassigned cell insertion/stripping, header error control (HEC) generation, checking, and statistics.
- Communications processor module (CPM)
  - RISC communications processor (CP)
  - Communication-specific commands (for example, GRACEFUL STOP TRANSMIT, ENTER HUNT MODE, and RESTART TRANSMIT)
  - Supports continuous mode transmission and reception on all serial channels

- — Up to 8 Kbytes of dual-port RAM
- — 16 serial DMA (SDMA) channels
- — Three parallel I/O registers with open-drain capability
- Four baud-rate generators (BRGs)
  - — Independent (can be tied to any SCC or SMC)
  - — Allows changes during operation
  - — Autobaud support option
- Four serial communications controllers (SCCs)
  - — Ethernet/IEEE 802.3® standard optional on SCC1–4, supporting full 10-Mbps operation (available only on specially programmed devices)
  - — HDLC/SDLC (all channels supported at 2 Mbps)
  - — HDLC bus (implements an HDLC-based local area network (LAN))
  - — Asynchronous HDLC to support point-to-point protocol (PPP)
  - — AppleTalk
  - — Universal asynchronous receiver transmitter (UART)
  - — Synchronous UART
  - — Serial infrared (IrDA)
  - — Binary synchronous communication (BISYNC)
  - — Totally transparent (bit streams)
  - — Totally transparent (frame-based with optional cyclic redundancy check (CRC))
- Two SMCs (serial management channels)
  - — UART
  - — Transparent
  - — General circuit interface (GCI) controller
  - — Can be connected to the time-division multiplexed (TDM) channels
- One SPI (serial peripheral interface)
  - — Supports master and slave modes
  - — Supports multimaster operation on the same bus
- One I^2C (inter-integrated circuit) port
  - — Supports master and slave modes
  - — Multiple-master environment support
- Time-slot assigner (TSA)
  - — Allows SCCs and SMCs to run in multiplexed and/or non-multiplexed operation
  - — Supports T1, CEPT, PCM highway, ISDN basic rate, ISDN primary rate, user defined
  - — 1- or 8-bit resolution
  - — Allows independent transmit and receive routing, frame synchronization, and clocking

Table 7. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B31a	CLKOUT falling edge to $\overline{CS}$ valid—as requested by control bit CST1 in the corresponding word in UPM	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.54	ns
B31b	CLKOUT rising edge to $\overline{CS}$ valid—as requested by control bit CST2 in the corresponding word in UPM	1.50	8.00	1.50	8.00	1.50	8.00	1.50	8.00	ns
B31c	CLKOUT rising edge to $\overline{CS}$ valid—as requested by control bit CST3 in the corresponding word in UPM	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.04	ns
B31d	CLKOUT falling edge to $\overline{CS}$ valid—as requested by control bit CST1 in the corresponding word in UPM, EBDF = 1	13.26	17.99	11.28	16.00	9.40	14.13	7.58	12.31	ns
B32	CLKOUT falling edge to $\overline{BS}$ valid—as requested by control bit BST4 in the corresponding word in UPM	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns
B32a	CLKOUT falling edge to $\overline{BS}$ valid—as requested by control bit BST1 in the corresponding word in UPM, EBDF = 0	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.54	ns
B32b	CLKOUT rising edge to $\overline{BS}$ valid—as requested by control bit BST2 in the corresponding word in UPM	1.50	8.00	1.50	8.00	1.50	8.00	1.50	8.00	ns
B32c	CLKOUT rising edge to $\overline{BS}$ valid—as requested by control bit BST3 in the corresponding word in UPM	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.54	ns
B32d	CLKOUT falling edge to $\overline{BS}$ valid—as requested by control bit BST1 in the corresponding word in UPM, EBDF = 1	13.26	17.99	11.28	16.00	9.40	14.13	7.58	12.31	ns
B33	CLKOUT falling edge to $\overline{GPL}$ valid—as requested by control bit GxT4 in the corresponding word in UPM	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns
B33a	CLKOUT rising edge to $\overline{GPL}$ valid—as requested by control bit GxT3 in the corresponding word in UPM	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.54	ns
B34	A(0:31), BADDR(28:30), and D(0:31) to $\overline{CS}$ valid—as requested by control bit CST4 in the corresponding word in UPM	5.58	—	4.25	—	3.00	—	1.79	—	ns
B34a	A(0:31), BADDR(28:30), and D(0:31) to $\overline{CS}$ valid—as requested by control bit CST1 in the corresponding word in UPM	13.15	—	10.50	—	8.00	—	5.58	—	ns
B34b	A(0:31), BADDR(28:30), and D(0:31) to $\overline{CS}$ valid—as requested by control bit CST2 in the corresponding word in UPM	20.73	—	16.75	—	13.00	—	9.36	—	ns

Table 7. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B35	A(0:31), BADDR(28:30) to $\overline{CS}$ valid—as requested by control bit BST4 in the corresponding word in UPM	5.58	—	4.25	—	3.00	—	1.79	—	ns
B35a	A(0:31), BADDR(28:30), and D(0:31) to $\overline{BS}$ valid—as requested by control bit BST1 in the corresponding word in UPM	13.15	—	10.50	—	8.00	—	5.58	—	ns
B35b	A(0:31), BADDR(28:30), and D(0:31) to $\overline{BS}$ valid—as requested by control bit BST2 in the corresponding word in UPM	20.73	—	16.75	—	13.00	—	9.36	—	ns
B36	A(0:31), BADDR(28:30), and D(0:31) to $\overline{GPL}$ valid—as requested by control bit GxT4 in the corresponding word in UPM	5.58	—	4.25	—	3.00	—	1.79	—	ns
B37	UPWAIT valid to CLKOUT falling edge[9]	6.00	—	6.00	—	6.00	—	6.00	—	ns
B38	CLKOUT falling edge to UPWAIT valid[9]	1.00	—	1.00	—	1.00	—	1.00	—	ns
B39	$\overline{AS}$ valid to CLKOUT rising edge[10]	7.00	—	7.00	—	7.00	—	7.00	—	ns
B40	A(0:31), TSIZ(0:1), RD/$\overline{WR}$, $\overline{BURST}$, valid to CLKOUT rising edge	7.00	—	7.00	—	7.00	—	7.00	—	ns
B41	$\overline{TS}$ valid to CLKOUT rising edge (setup time)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B42	CLKOUT rising edge to $\overline{TS}$ valid (hold time)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B43	$\overline{AS}$ negation to memory controller signals negation	—	TBD	—	TBD	—	TBD	—	TBD	ns

1 Phase and frequency jitter performance results are only valid if the input jitter is less than the prescribed value.

2 If the rate of change of the frequency of EXTAL is slow (that is, it does not jump between the minimum and maximum values in one cycle) or the frequency of the jitter is fast (that is, it does not stay at an extreme value for a long time) then the maximum allowed jitter on EXTAL can be up to 2%.

3 The timings specified in B4 and B5 are based on full strength clock.

4 The timing for $\overline{BR}$ output is relevant when the MPC860 is selected to work with external bus arbiter. The timing for $\overline{BG}$ output is relevant when the MPC860 is selected to work with internal bus arbiter.

5 The timing required for $\overline{BR}$ input is relevant when the MPC860 is selected to work with internal bus arbiter. The timing for $\overline{BG}$ input is relevant when the MPC860 is selected to work with external bus arbiter.

6 The D(0:31) and DP(0:3) input timings B18 and B19 refer to the rising edge of the CLKOUT in which the $\overline{TA}$ input signal is asserted.

7 The D(0:31) and DP(0:3) input timings B20 and B21 refer to the falling edge of the CLKOUT. This timing is valid only for read accesses controlled by chip-selects under control of the UPM in the memory controller, for data beats where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

8 The timing B30 refers to $\overline{CS}$ when ACS = 00 and to $\overline{WE}$(0:3) when CSNT = 0.

9 The signal UPWAIT is considered asynchronous to the CLKOUT and synchronized internally. The timings specified in B37 and B38 are specified to enable the freeze of the UPM output signals as described in Figure 18.

10 The $\overline{AS}$ signal is considered asynchronous to the CLKOUT. The timing B39 is specified in order to allow the behavior specified in Figure 21.

Figure 7 provides the timing for the synchronous input signals.

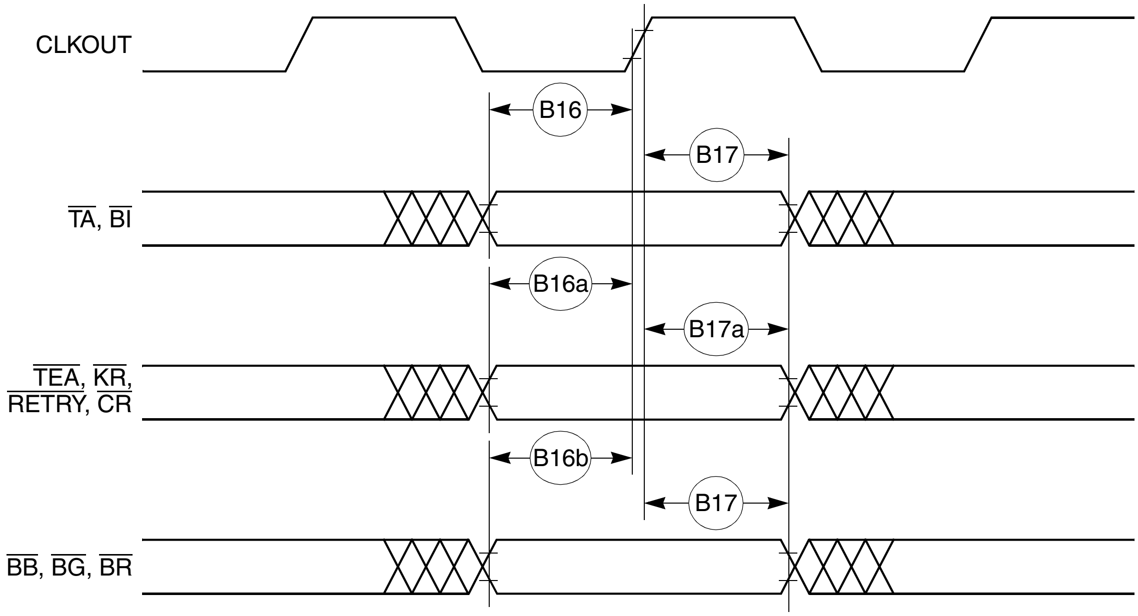


Figure 7. Synchronous Input Signals Timing

Figure 8 provides normal case timing for input data. It also applies to normal read accesses under the control of the UPM in the memory controller.

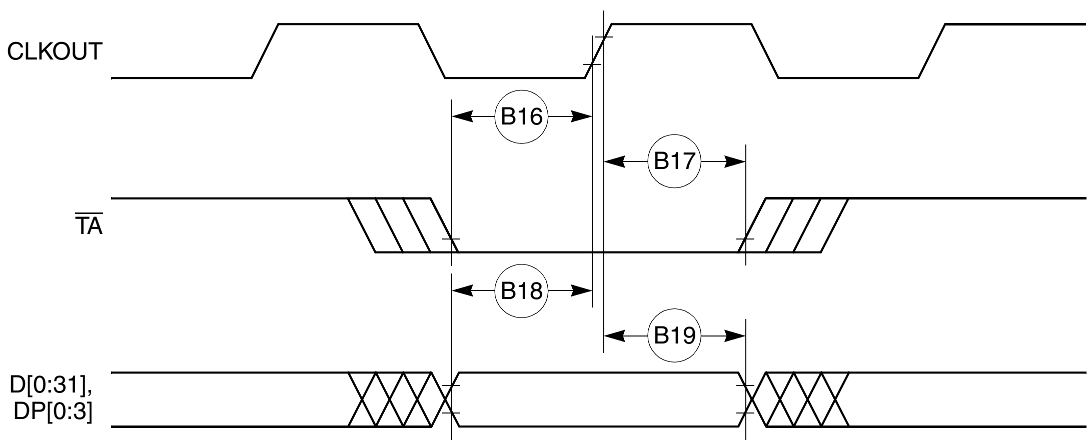


Figure 8. Input Data Timing in Normal Case

Figure 9 provides the timing for the input data controlled by the UPM for data beats where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

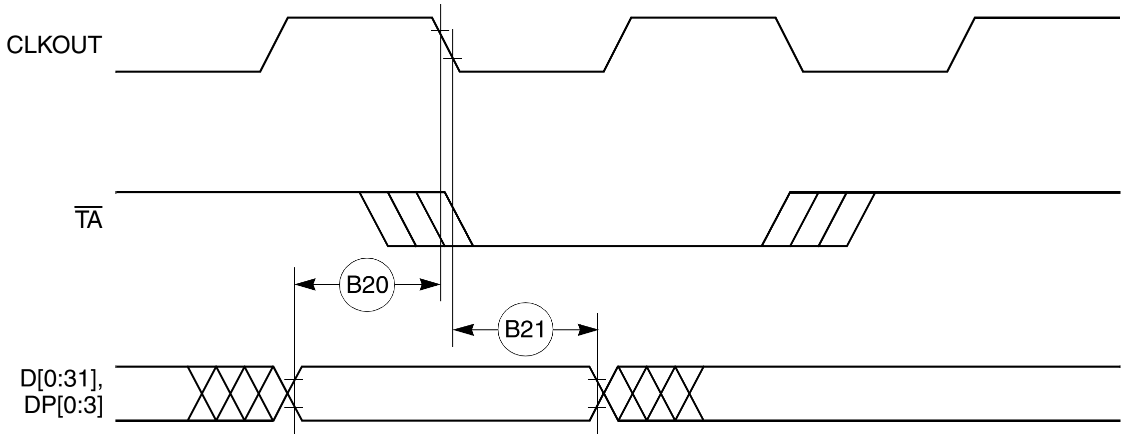


Figure 9. Input Data Timing when Controlled by UPM in the Memory Controller and DLT3 = 1

Figure 10 through Figure 13 provide the timing for the external bus read controlled by various GPCM factors.

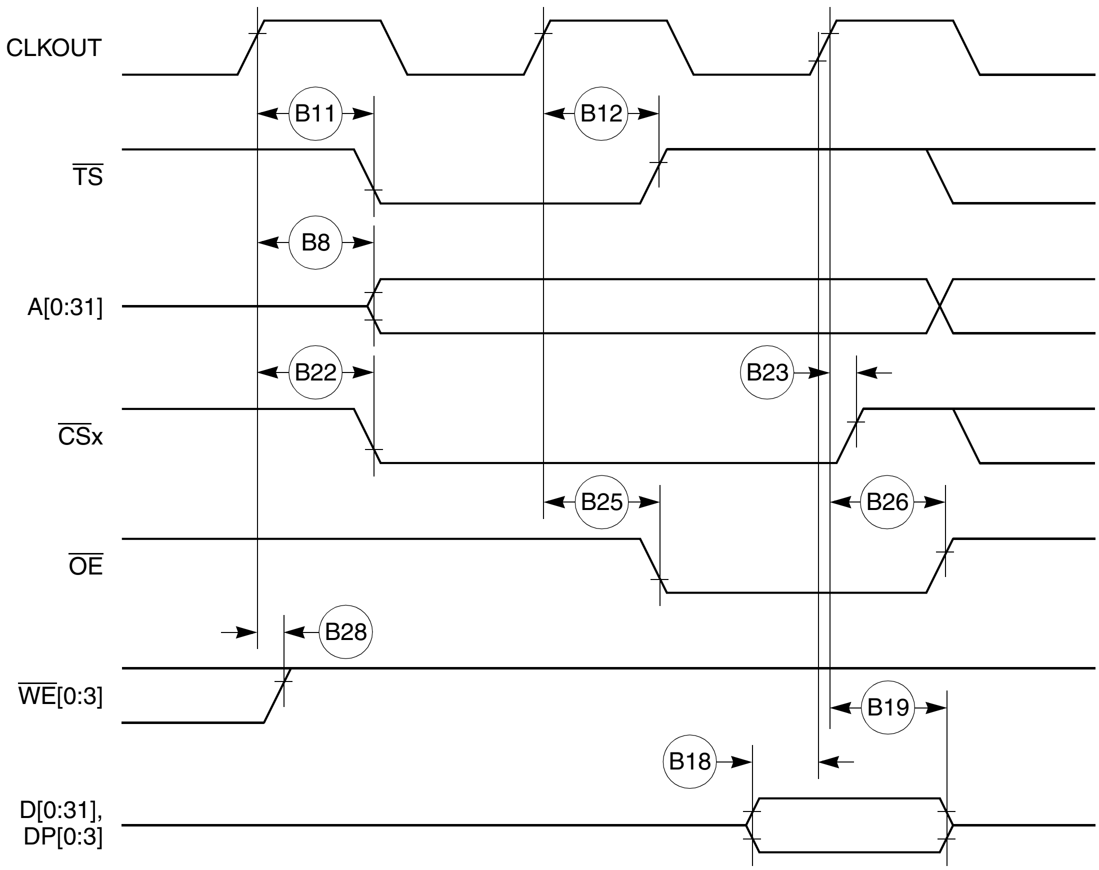


Figure 10. External Bus Read Timing (GPCM Controlled—ACS = 00)

Figure 17 provides the timing for the external bus controlled by the UPM.

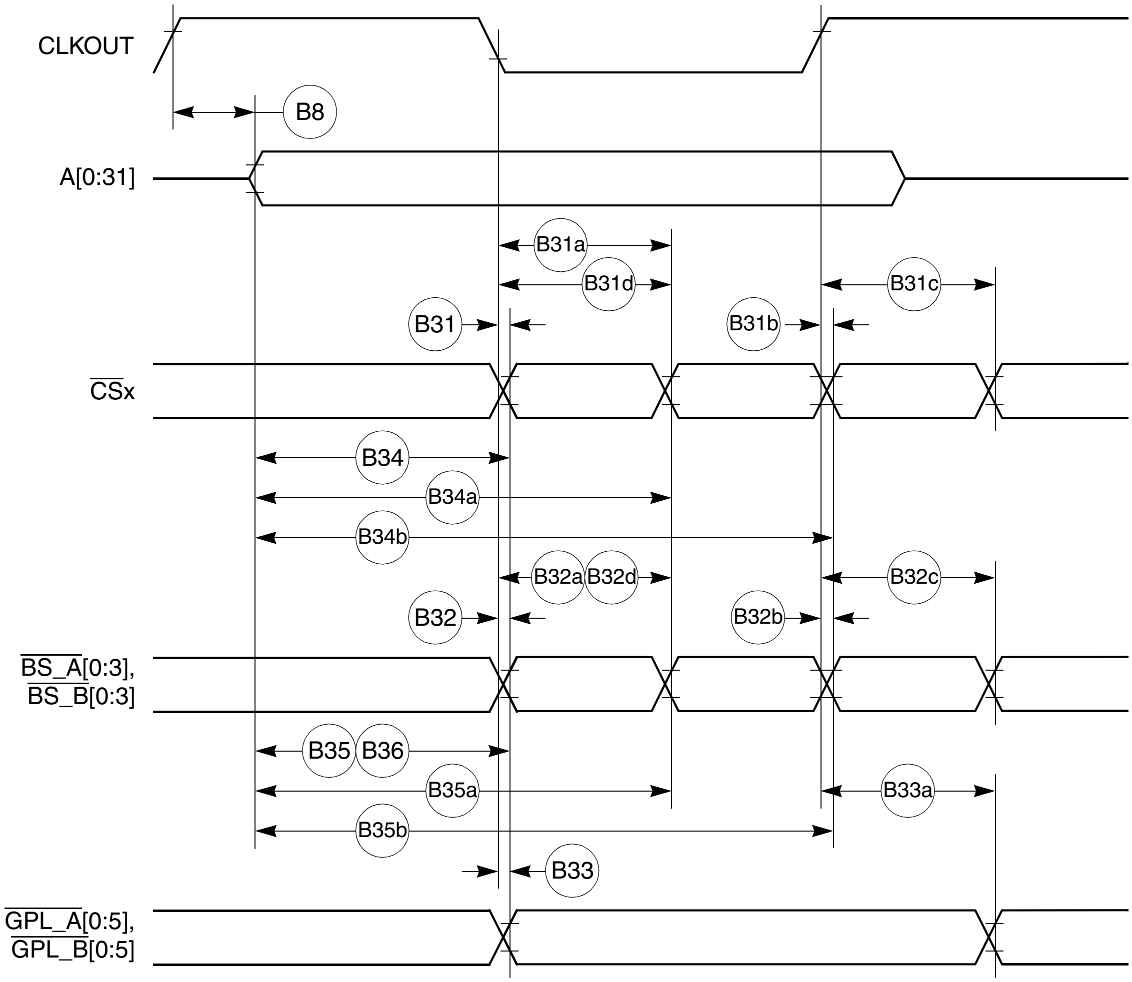


Figure 17. External Bus Timing (UPM Controlled Signals)

Figure 18 provides the timing for the asynchronous asserted UPWAIT signal controlled by the UPM.

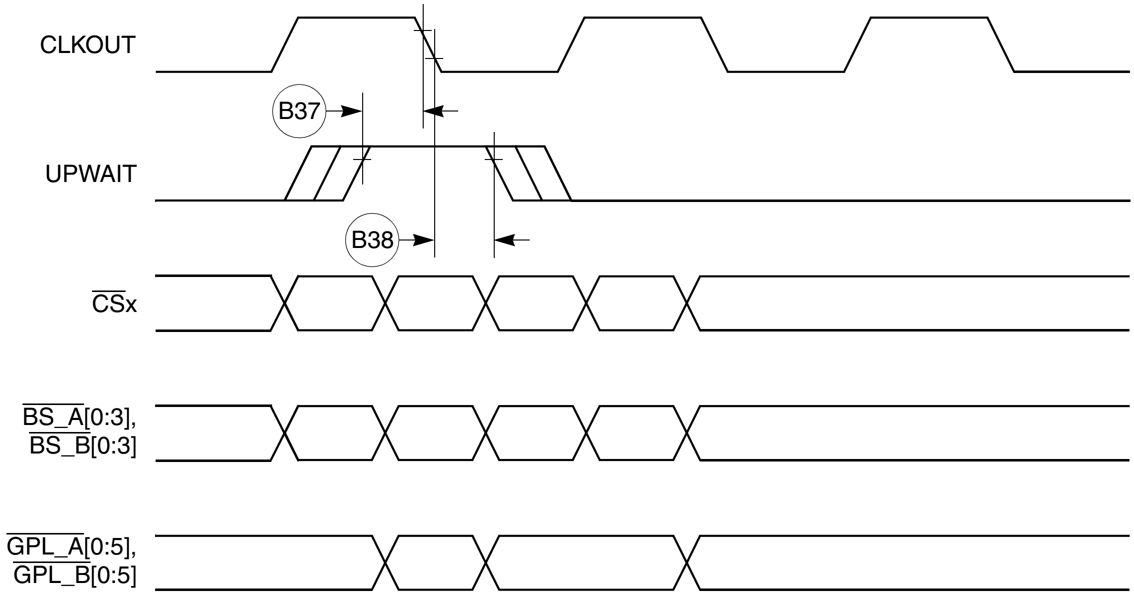


Figure 18. Asynchronous UPWAIT Asserted Detection in UPM Handled Cycles Timing

Figure 19 provides the timing for the asynchronous negated UPWAIT signal controlled by the UPM.

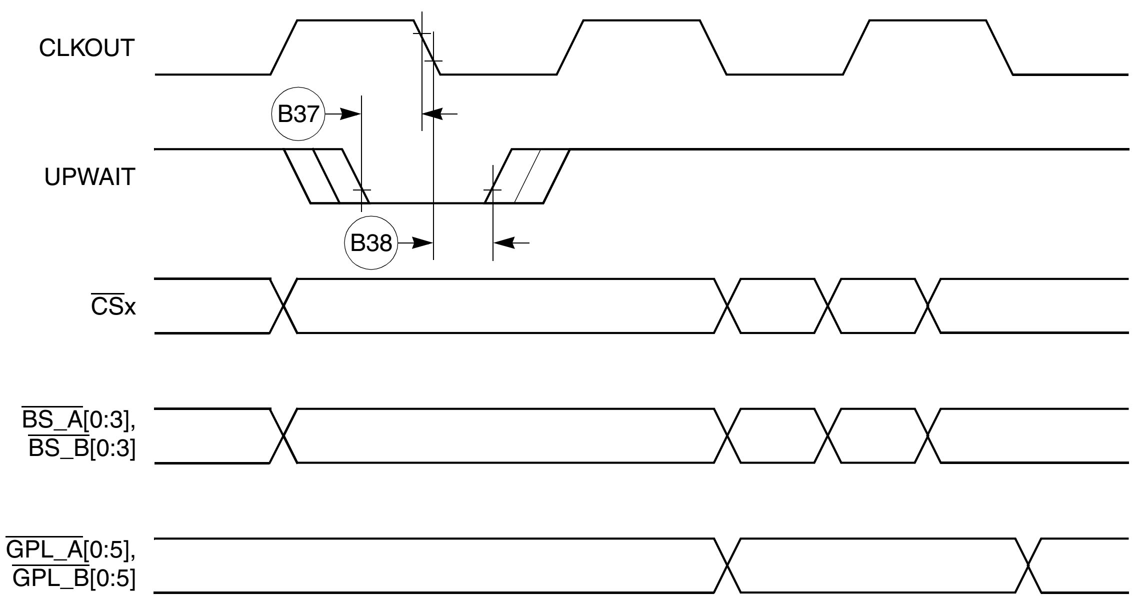


Figure 19. Asynchronous UPWAIT Negated Detection in UPM Handled Cycles Timing

Figure 20 provides the timing for the synchronous external master access controlled by the GPCM.

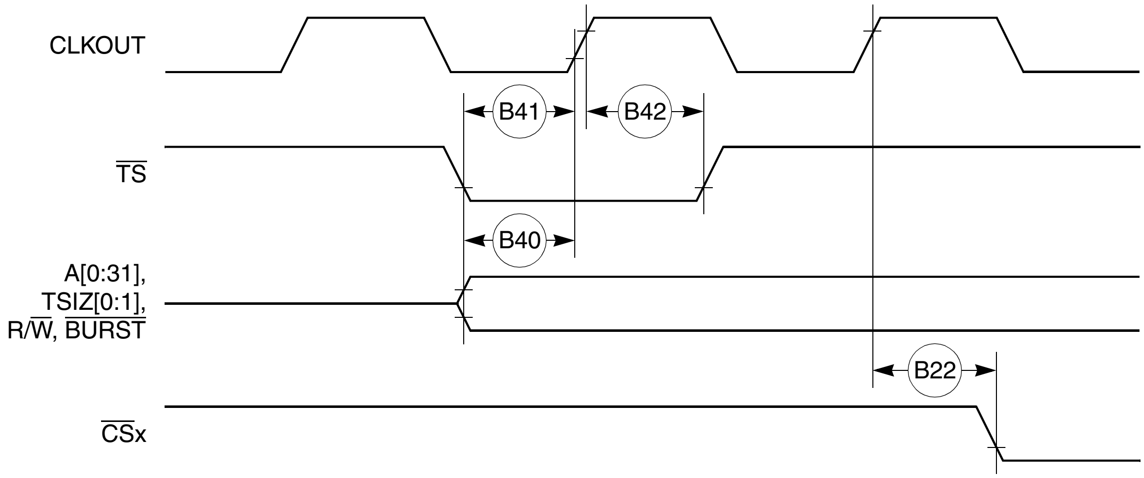


Figure 20. Synchronous External Master Access Timing (GPCM Handled ACS = 00)

Figure 21 provides the timing for the asynchronous external master memory access controlled by the GPCM.

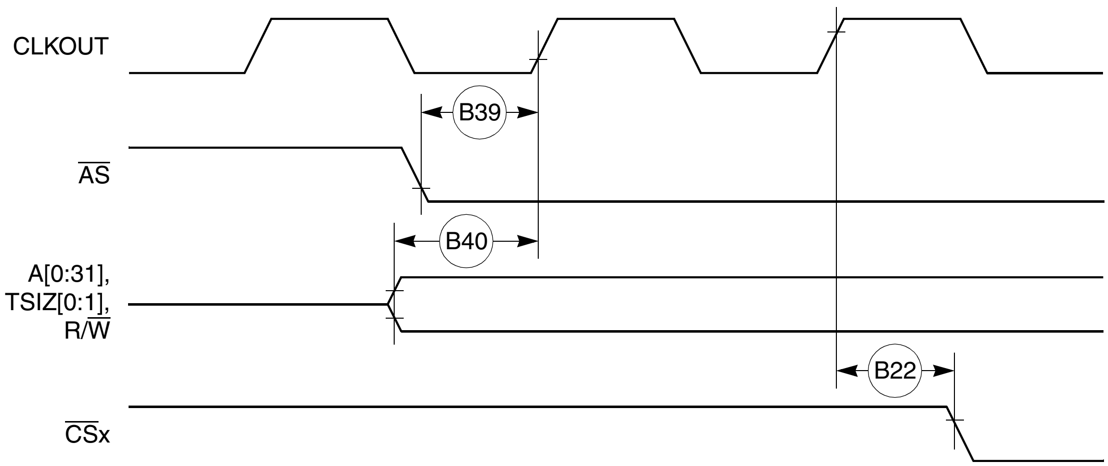


Figure 21. Asynchronous External Master Memory Access Timing (GPCM Controlled—ACS = 00)

Figure 22 provides the timing for the asynchronous external master control signals negation.

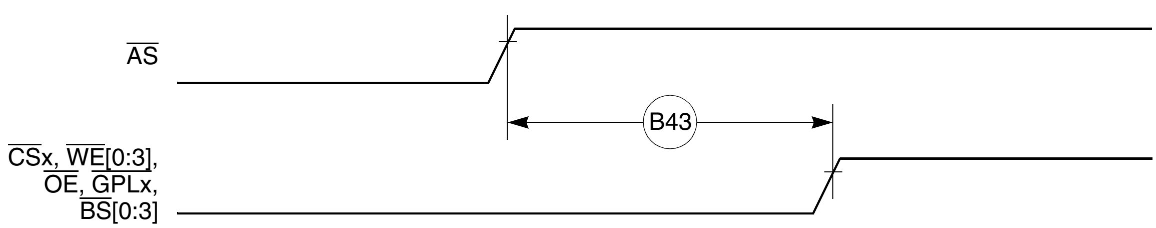


Figure 22. Asynchronous External Master—Control Signals Negation Timing

Table 8 provides interrupt timing for the MPC860.

Table 8. Interrupt Timing

Num	Characteristic[1]	All Frequencies		Unit
		Min	Max	
I39	$\overline{\text{IRQ}}$x valid to CLKOUT rising edge (setup time)	6.00	—	ns
I40	$\overline{\text{IRQ}}$x hold time after CLKOUT	2.00	—	ns
I41	$\overline{\text{IRQ}}$x pulse width low	3.00	—	ns
I42	$\overline{\text{IRQ}}$x pulse width high	3.00	—	ns
I43	$\overline{\text{IRQ}}$x edge-to-edge time	$4 \times T_{CLOCKOUT}$	—	—

[1] The timings I39 and I40 describe the testing conditions under which the $\overline{\text{IRQ}}$ lines are tested when being defined as level-sensitive. The $\overline{\text{IRQ}}$ lines are synchronized internally and do not have to be asserted or negated with reference to the CLKOUT.
The timings I41, I42, and I43 are specified to allow the correct function of the $\overline{\text{IRQ}}$ lines detection circuitry and have no direct relation with the total system interrupt latency that the MPC860 is able to support.

Figure 23 provides the interrupt detection timing for the external level-sensitive lines.

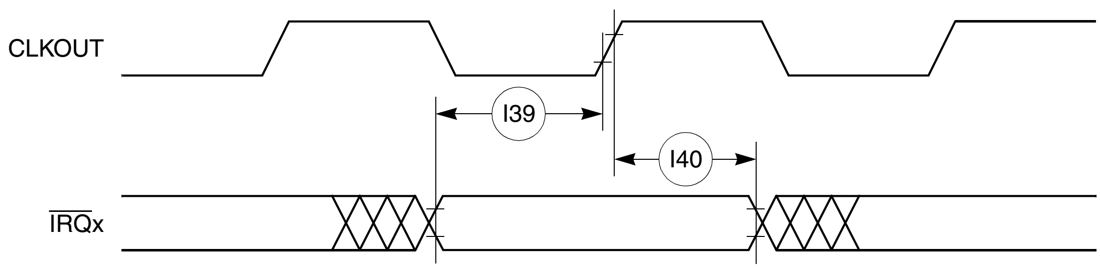


Figure 23. Interrupt Detection Timing for External Level Sensitive Lines

Figure 24 provides the interrupt detection timing for the external edge-sensitive lines.

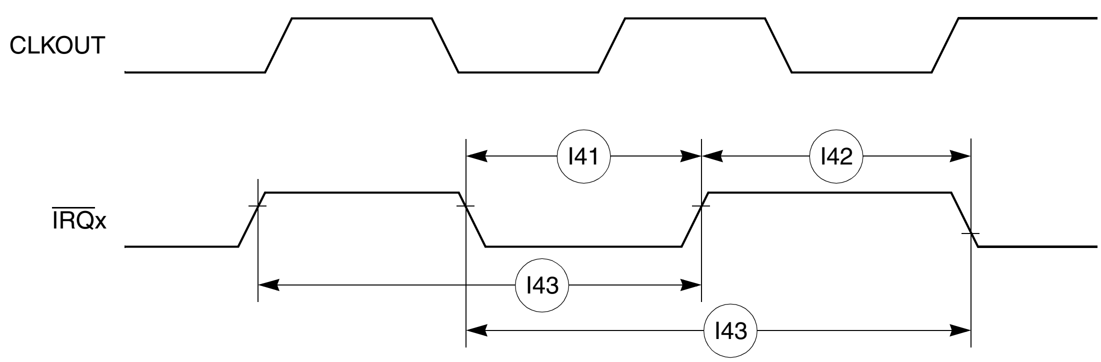


Figure 24. Interrupt Detection Timing for External Edge Sensitive Lines

Table 9 shows the PCMCIA timing for the MPC860.

Table 9. PCMCIA Timing

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
P44	A(0:31), $\overline{\text{REG}}$ valid to PCMCIA Strobe asserted[1]	20.73	—	16.75	—	13.00	—	9.36	—	ns
P45	A(0:31), $\overline{\text{REG}}$ valid to ALE negation[1]	28.30	—	23.00	—	18.00	—	13.15	—	ns
P46	CLKOUT to $\overline{\text{REG}}$ valid	7.58	15.58	6.25	14.25	5.00	13.00	3.79	11.84	ns
P47	CLKOUT to $\overline{\text{REG}}$ invalid	8.58	—	7.25	—	6.00	—	4.84	—	ns
P48	CLKOUT to $\overline{\text{CE1}}$, $\overline{\text{CE2}}$ asserted	7.58	15.58	6.25	14.25	5.00	13.00	3.79	11.84	ns
P49	CLKOUT to $\overline{\text{CE1}}$, $\overline{\text{CE2}}$ negated	7.58	15.58	6.25	14.25	5.00	13.00	3.79	11.84	ns
P50	CLKOUT to $\overline{\text{PCOE}}$, $\overline{\text{IORD}}$, $\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ assert time	—	11.00		11.00	—	11.00	—	11.00	ns
P51	CLKOUT to $\overline{\text{PCOE}}$, $\overline{\text{IORD}}$, $\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ negate time	2.00	11.00	2.00	11.00	2.00	11.00	2.00	11.00	ns
P52	CLKOUT to ALE assert time	7.58	15.58	6.25	14.25	5.00	13.00	3.79	10.04	ns
P53	CLKOUT to ALE negate time	—	15.58		14.25	—	13.00	—	11.84	ns
P54	$\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ negated to D(0:31) invalid[1]	5.58	—	4.25	—	3.00	—	1.79	—	ns
P55	$\overline{\text{WAITA}}$ and $\overline{\text{WAITB}}$ valid to CLKOUT rising edge[1]	8.00	—	8.00	—	8.00	—	8.00	—	ns
P56	CLKOUT rising edge to $\overline{\text{WAITA}}$ and $\overline{\text{WAITB}}$ invalid[1]	2.00	—	2.00	—	2.00	—	2.00	—	ns

[1] PSST = 1. Otherwise add PSST times cycle time.
PSHT = 0. Otherwise add PSHT times cycle time.

These synchronous timings define when the $\overline{\text{WAITx}}$ signals are detected in order to freeze (or relieve) the PCMCIA current cycle. The $\overline{\text{WAITx}}$ assertion will be effective only if it is detected 2 cycles before the PSL timer expiration. See Chapter 16, "PCMCIA Interface," in the *MPC860 PowerQUICC™ Family User's Manual*.

Figure 26 provides the PCMCIA access cycle timing for the external bus write.

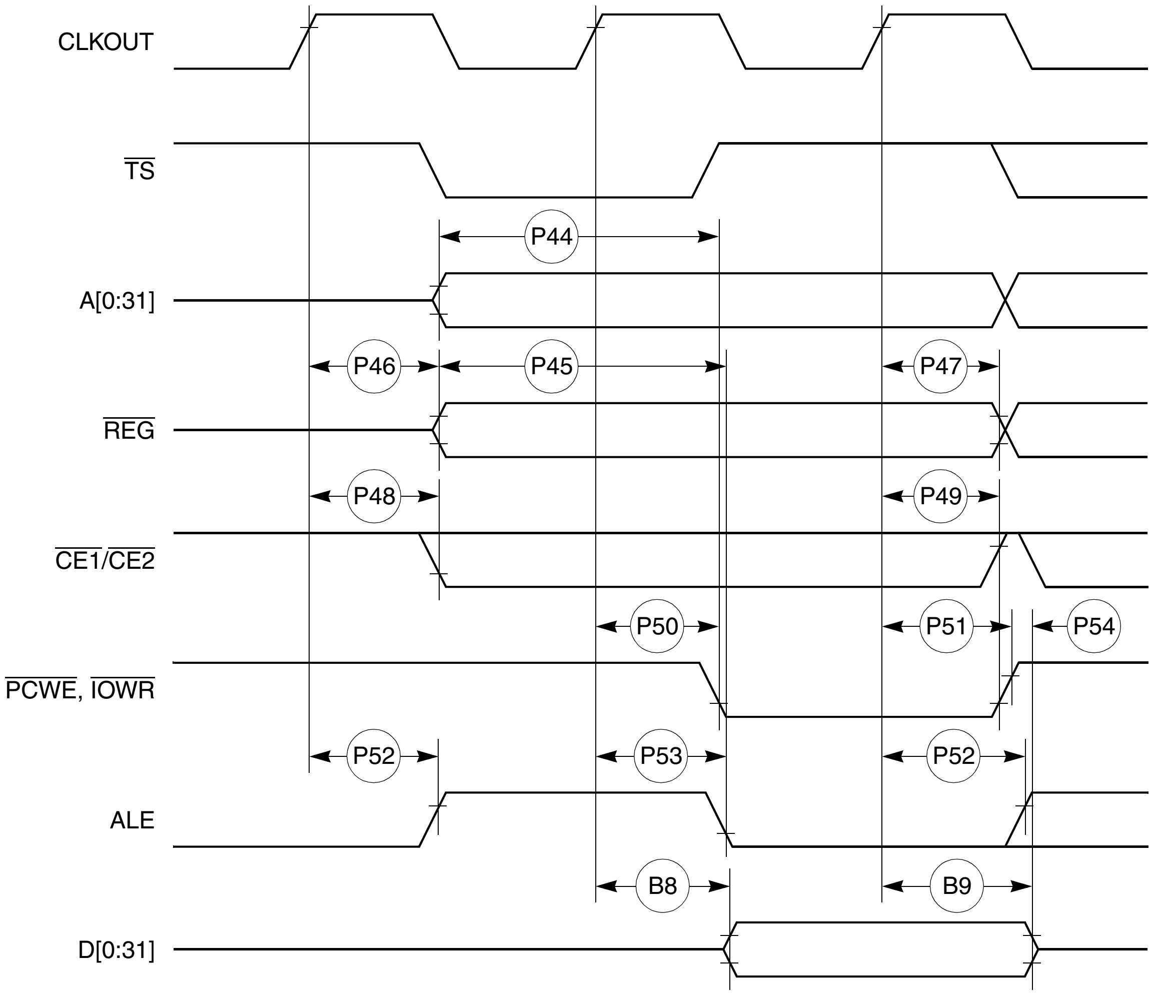


Figure 26. PCMCIA Access Cycle Timing External Bus Write

Figure 27 provides the PCMCIA WAIT signal detection timing.

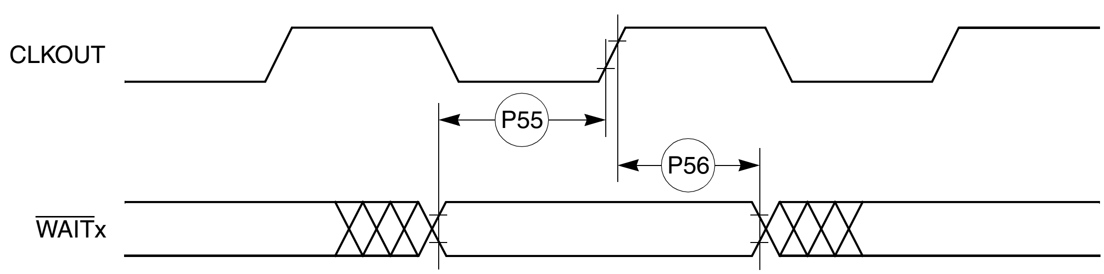


Figure 27. PCMCIA WAIT Signal Detection Timing

Table 11 shows the debug port timing for the MPC860.

Table 11. Debug Port Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
P61	DSCK cycle time	$3 \times T_{CLOCKOUT}$	—	—
P62	DSCK clock pulse width	$1.25 \times T_{CLOCKOUT}$	—	—
P63	DSCK rise and fall times	0.00	3.00	ns
P64	DSDI input data setup time	8.00	—	ns
P65	DSDI data hold time	5.00	—	ns
P66	DSCK low to DSDO data valid	0.00	15.00	ns
P67	DSCK low to DSDO invalid	0.00	2.00	ns

Figure 30 provides the input timing for the debug port clock.

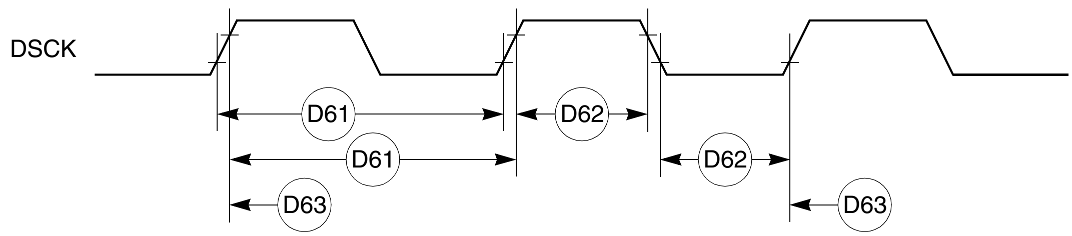


Figure 30. Debug Port Clock Input Timing

Figure 31 provides the timing for the debug port.

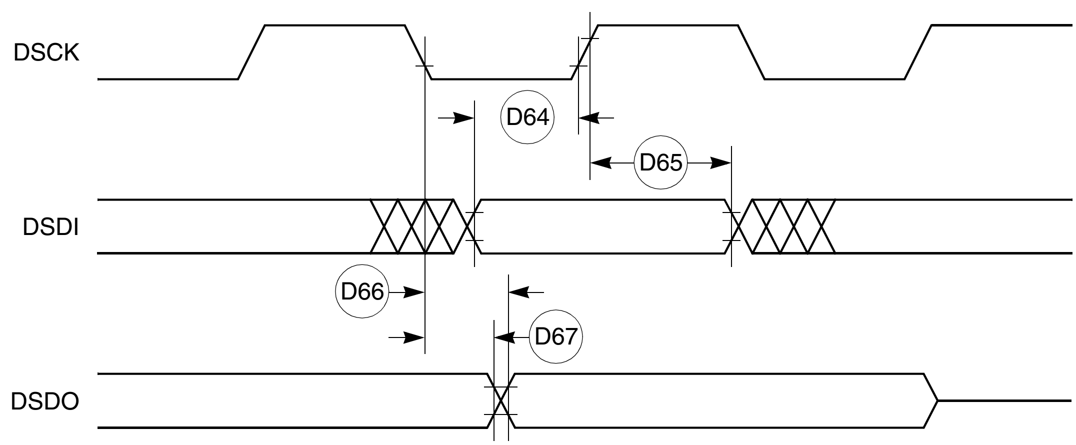


Figure 31. Debug Port Timings

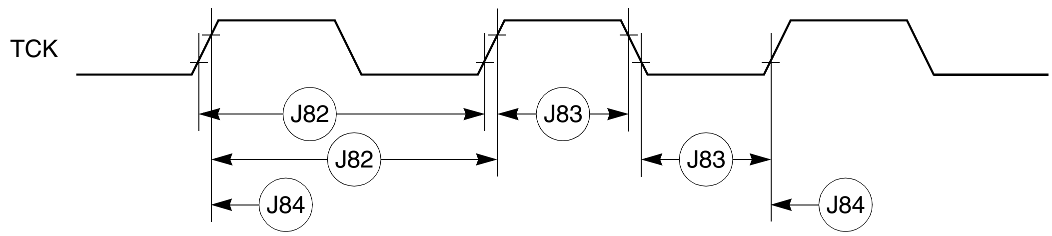


Figure 35. JTAG Test Clock Input Timing

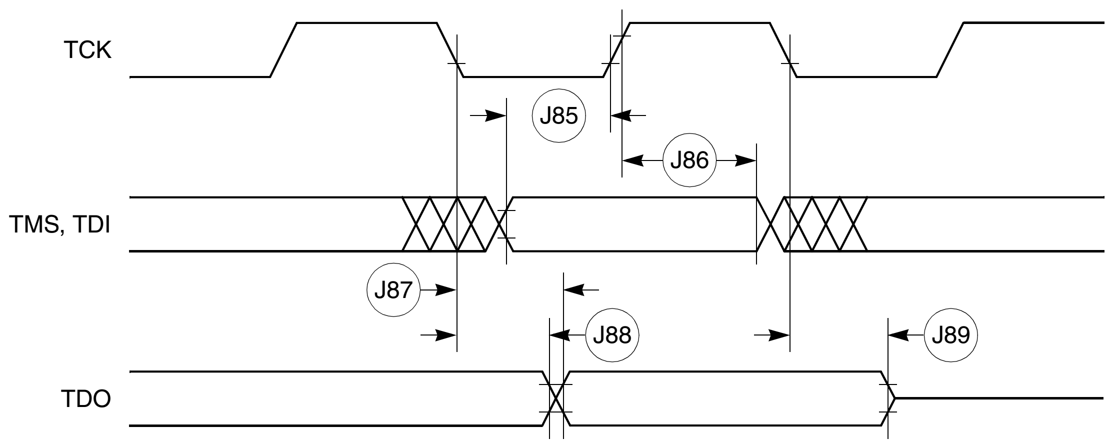


Figure 36. JTAG Test Access Port Timing Diagram

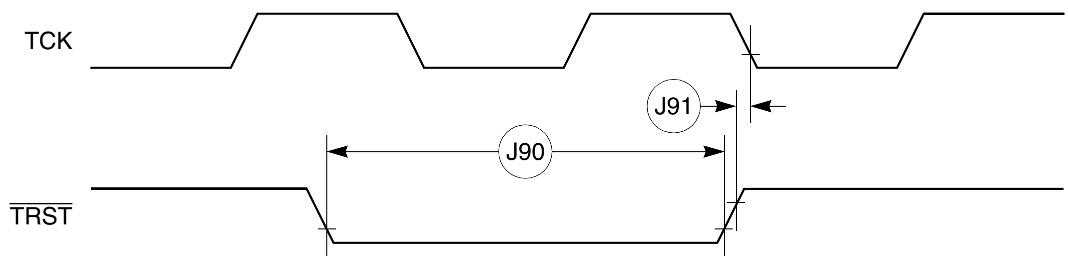


Figure 37. JTAG $\overline{\text{TRST}}$ Timing Diagram

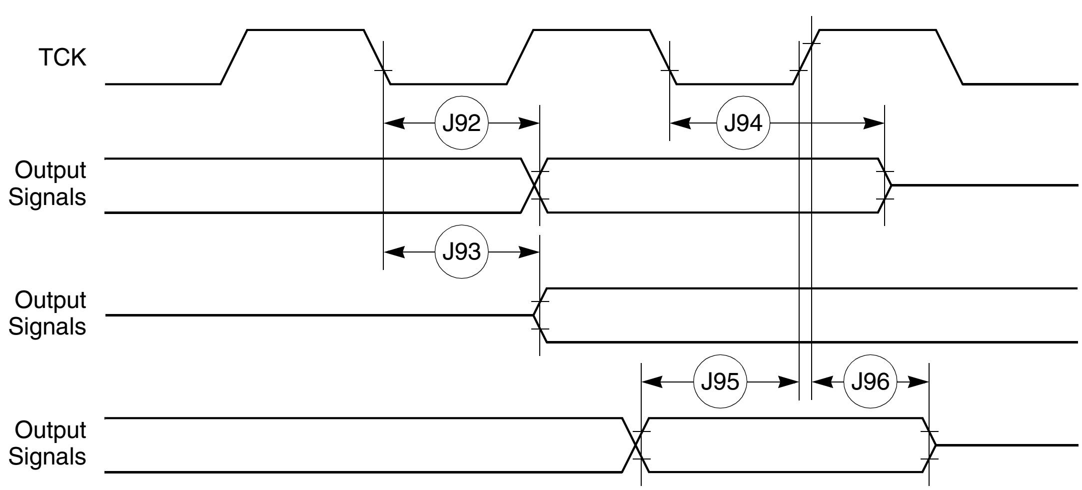


Figure 38. Boundary Scan (JTAG) Timing Diagram

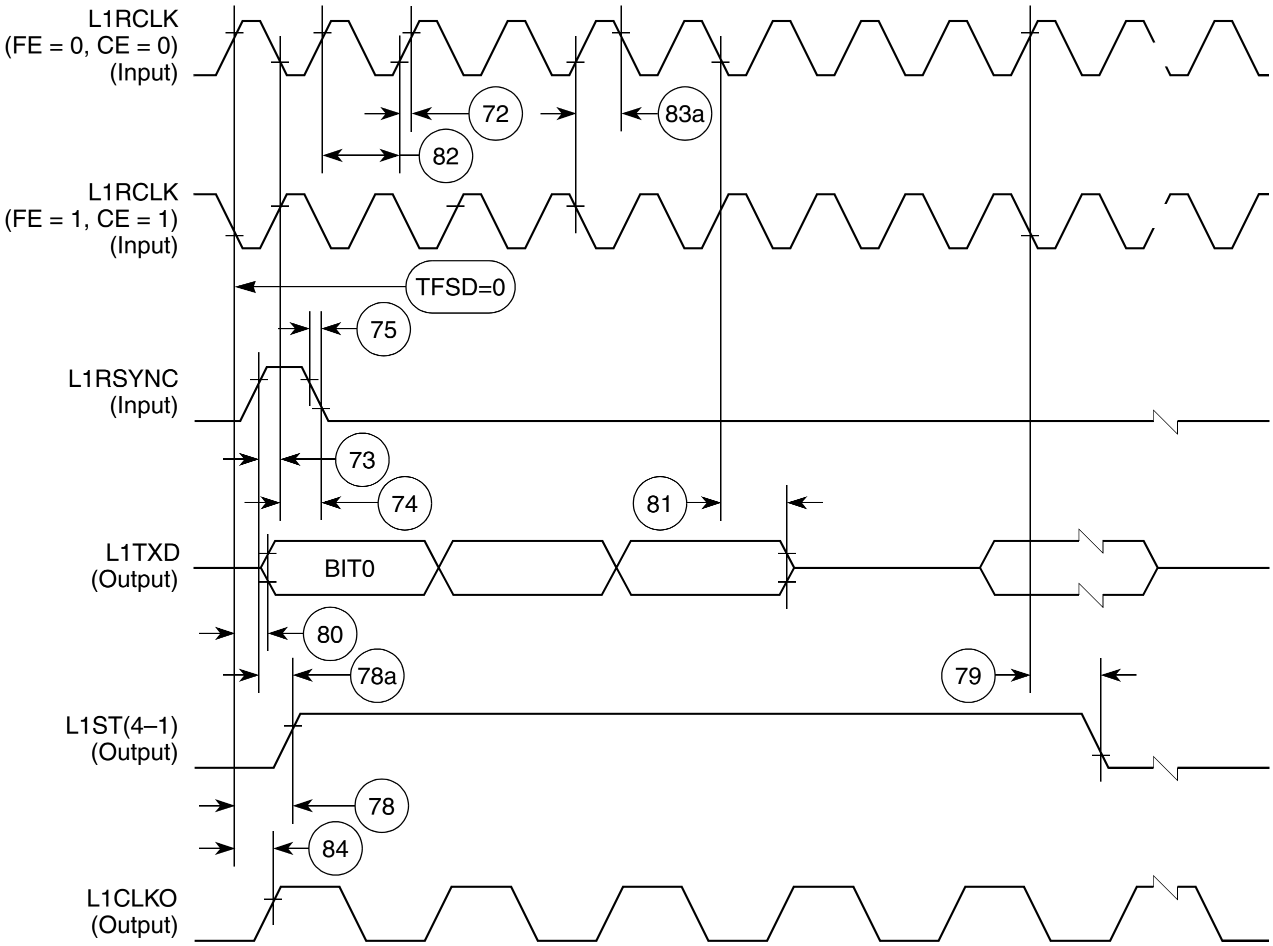


Figure 54. SI Transmit Timing with Double Speed Clocking (DSC = 1)

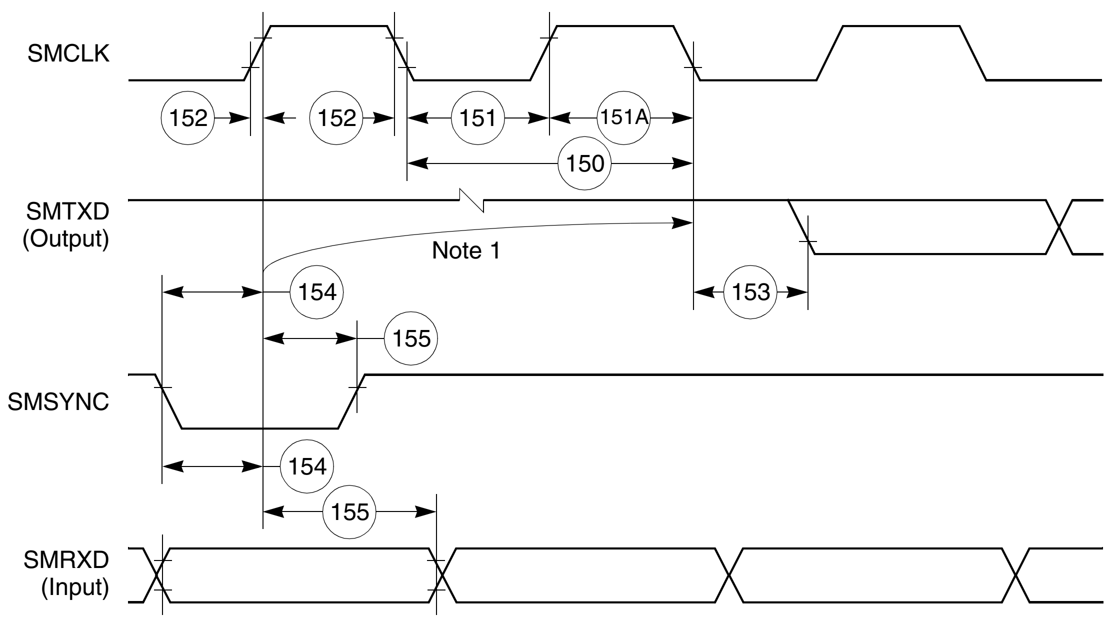
11.9 SMC Transparent AC Electrical Specifications

Table 23 provides the SMC transparent timings as shown in Figure 64.

Table 23. SMC Transparent Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
150	SMCLK clock period[1]	100	—	ns
151	SMCLK width low	50	—	ns
151A	SMCLK width high	50	—	ns
152	SMCLK rise/fall time	—	15	ns
153	SMTXD active delay (from SMCLK falling edge)	10	50	ns
154	SMRXD/SMSYNC setup time	20	—	ns
155	RXD1/SMSYNC hold time	5	—	ns

[1] SYNCCLK must be at least twice as fast as SMCLK.



Note:
1. This delay is equal to an integer number of character-length clocks.

Figure 64. SMC Transparent Timing Diagram

11.10 SPI Master AC Electrical Specifications

Table 24 provides the SPI master timings as shown in Figure 65 and Figure 66.

Table 24. SPI Master Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
160	MASTER cycle time	4	1024	t_{cyc}
161	MASTER clock (SCK) high or low time	2	512	t_{cyc}
162	MASTER data setup time (inputs)	50	—	ns
163	Master data hold time (inputs)	0	—	ns
164	Master data valid (after SCK edge)	—	20	ns
165	Master data hold time (outputs)	0	—	ns
166	Rise time output	—	15	ns
167	Fall time output	—	15	ns

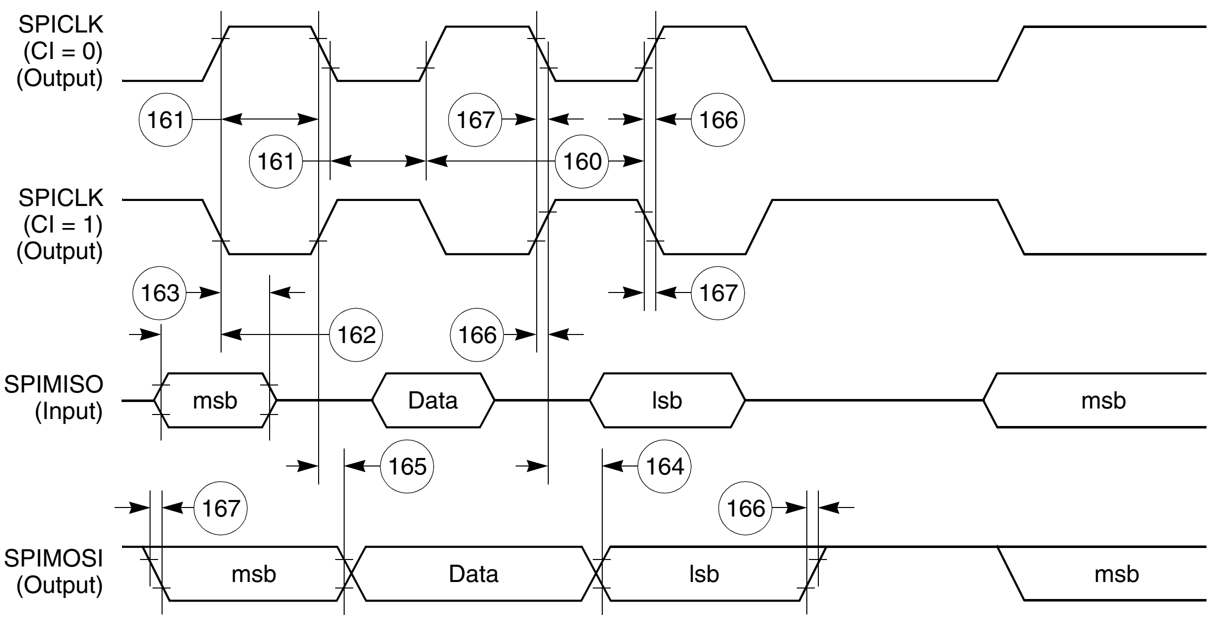


Figure 65. SPI Master (CP = 0) Timing Diagram

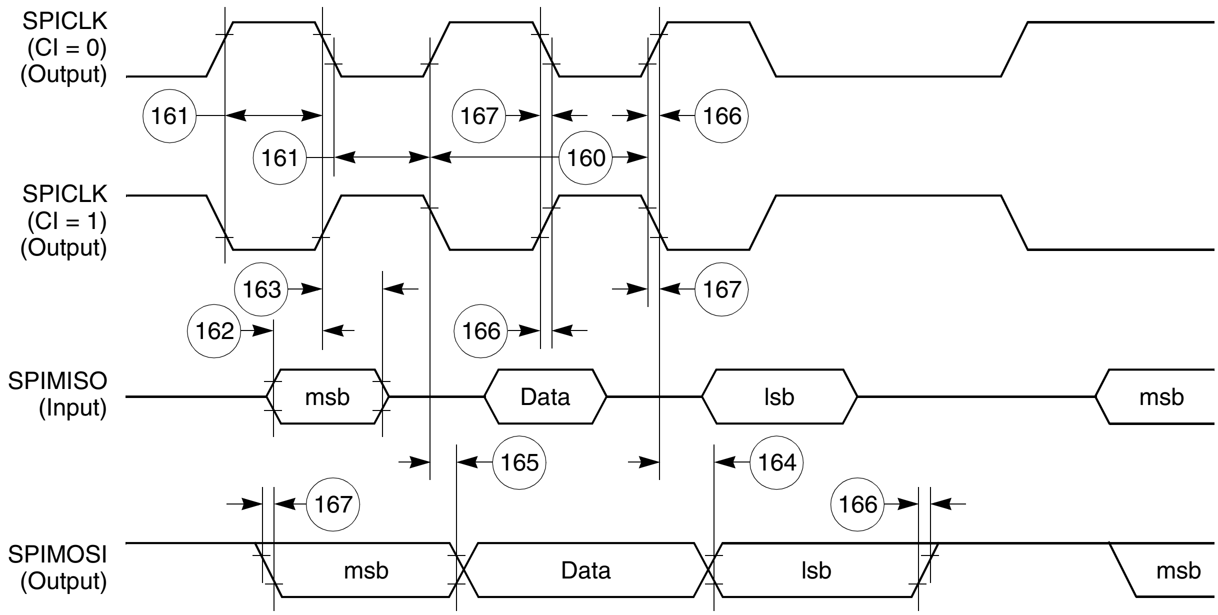


Figure 66. SPI Master (CP = 1) Timing Diagram

11.11 SPI Slave AC Electrical Specifications

Table 25 provides the SPI slave timings as shown in Figure 67 and Figure 68.

Table 25. SPI Slave Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
170	Slave cycle time	2	—	t_{cyc}
171	Slave enable lead time	15	—	ns
172	Slave enable lag time	15	—	ns
173	Slave clock (SPICLK) high or low time	1	—	t_{cyc}
174	Slave sequential transfer delay (does not require deselect)	1	—	t_{cyc}
175	Slave data setup time (inputs)	20	—	ns
176	Slave data hold time (inputs)	20	—	ns
177	Slave access time	—	50	ns

Figure 70 shows signal timings during UTOPIA receive operations.

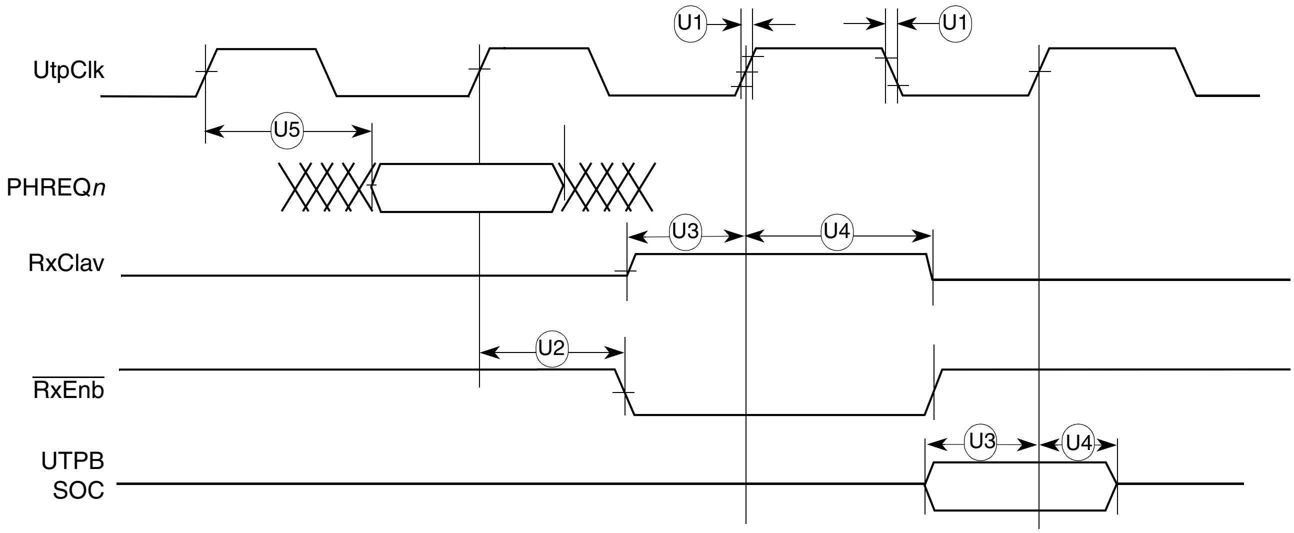


Figure 70. UTOPIA Receive Timing

Figure 71 shows signal timings during UTOPIA transmit operations.

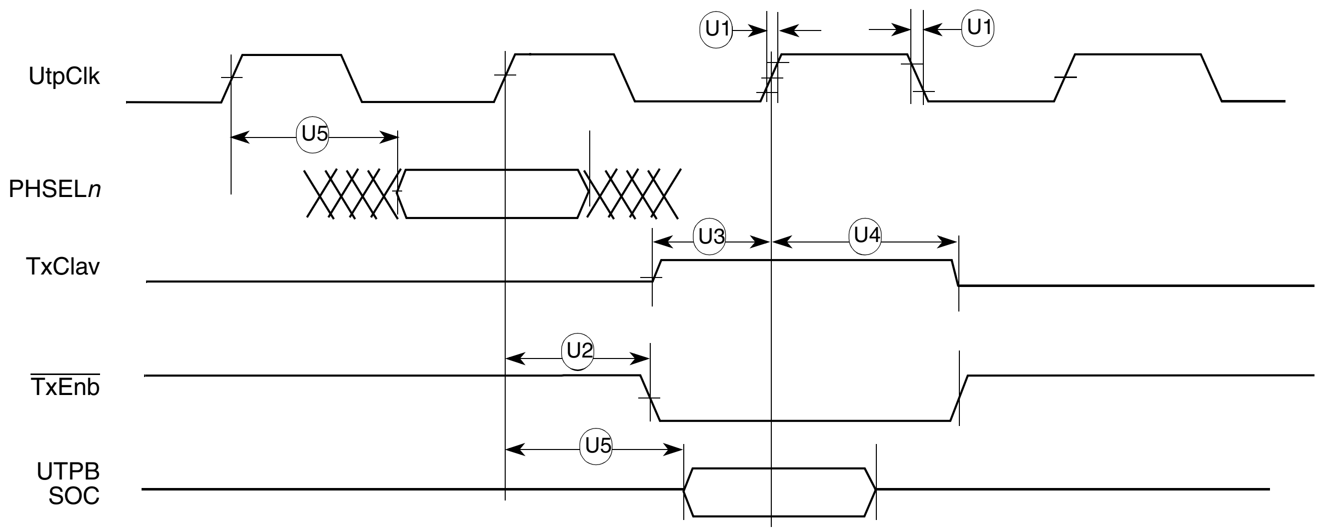


Figure 71. UTOPIA Transmit Timing

Table 34 identifies the packages and operating frequencies available for the MPC860.

Table 34. MPC860 Family Package/Frequency Availability

Package Type	Freq. (MHz) / Temp. (Tj)	Package	Order Number
Ball grid array ZP suffix—leaded ZQ suffix—leaded VR suffix—lead-free	50 0° to 95°C	ZP/ZQ[1]	MPC855TZQ50D4 MPC860DEZQ50D4 MPC860DTZQ50D4 MPC860ENZQ50D4 MPC860SRZQ50D4 MPC860TZQ50D4 MPC860DPZQ50D4 MPC860PZQ50D4
		Tape and Reel	MPC855TZQ50D4R2 MPC860DEZQ50D4R2 MPC860ENZQ50D4R2 MPC860SRZQ50D4R2 MPC860TZQ50D4R2 MPC860DPZQ50D4R2 MPC855TVR50D4R2 MPC860ENVR50D4R2 MPC860SRVR50D4R2 MPC860TVR50D4R2
		VR	MPC855TVR50D4 MPC860DEVR50D4 MPC860DPVR50D4 MPC860DTVR50D4 MPC860ENVR50D4 MPC860PVR50D4 MPC860SRVR50D4 MPC860TVR50D4
	66 0° to 95°C	ZP/ZQ[1]	MPC855TZQ66D4 MPC860DEZQ66D4 MPC860DTZQ66D4 MPC860ENZQ66D4 MPC860SRZQ66D4 MPC860TZQ66D4 MPC860DPZQ66D4 MPC860PZQ66D4
		Tape and Reel	MPC860SRZQ66D4R2 MPC860PZQ66D4R2
		VR	MPC855TVR66D4 MPC860DEVR66D4 MPC860DPVR66D4 MPC860DTVR66D4 MPC860ENVR66D4 MPC860PVR66D4 MPC860SRVR66D4 MPC860TVR66D4