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Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

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Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

#### Details

Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	50MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (2)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 95°C (TA)
Security Features	-
Package / Case	357-BBGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc860devr50d4r2">https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc860devr50d4r2</a>

# 1 Overview

The MPC860 power quad integrated communications controller (PowerQUICC™) is a versatile one-chip integrated microprocessor and peripheral combination designed for a variety of controller applications. It particularly excels in communications and networking systems. The PowerQUICC unit is referred to as the MPC860 in this hardware specification.

The MPC860 implements Power Architecture™ technology and contains a superset of Freescale's MC68360 quad integrated communications controller (QUICC), referred to here as the QUICC, RISC communications processor module (CPM). The CPU on the MPC860 is a 32-bit core built on Power Architecture technology that incorporates memory management units (MMUs) and instruction and data caches. The CPM from the MC68360 QUICC has been enhanced by the addition of the inter-integrated controller (I<sup>2</sup>C) channel. The memory controller has been enhanced, enabling the MPC860 to support any type of memory, including high-performance memories and new types of DRAMs. A PCMCIA socket controller supports up to two sockets. A real-time clock has also been integrated.

Table 1 shows the functionality supported by the MPC860 family.

**Table 1. MPC860 Family Functionality**

Part	Cache (Kbytes)		Ethernet		ATM	SCC	Reference <sup>1</sup>
	Instruction Cache	Data Cache	10T	10/100			
MPC860DE	4	4	Up to 2	—	—	2	1
MPC860DT	4	4	Up to 2	1	Yes	2	1
MPC860DP	16	8	Up to 2	1	Yes	2	1
MPC860EN	4	4	Up to 4	—	—	4	1
MPC860SR	4	4	Up to 4	—	Yes	4	1
MPC860T	4	4	Up to 4	1	Yes	4	1
MPC860P	16	8	Up to 4	1	Yes	4	1
MPC855T	4	4	1	1	Yes	1	2

<sup>1</sup> Supporting documentation for these devices refers to the following:

1. MPC860 PowerQUICC Family User's Manual (MPC860UM, Rev. 3)
2. MPC855T User's Manual (MPC855TUM, Rev. 1)

### 3 Maximum Tolerated Ratings

This section provides the maximum tolerated voltage and temperature ranges for the MPC860. [Table 2](#) provides the maximum ratings.

This device contains circuitry protecting against damage due to high-static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or  $V_{DD}$ ).

**Table 2. Maximum Tolerated Ratings**

(GND = 0 V)

Rating	Symbol	Value	Unit
Supply voltage <sup>1</sup>	$V_{DDH}$	−0.3 to 4.0	V
	$V_{DDL}$	−0.3 to 4.0	V
	KAPWR	−0.3 to 4.0	V
	$V_{DDSYN}$	−0.3 to 4.0	V
Input voltage <sup>2</sup>	$V_{in}$	GND − 0.3 to $V_{DDH}$	V
Temperature <sup>3</sup> (standard)	$T_{A(min)}$	0	°C
	$T_{j(max)}$	95	°C
Temperature <sup>3</sup> (extended)	$T_{A(min)}$	−40	°C
	$T_{j(max)}$	95	°C
Storage temperature range	$T_{stg}$	−55 to 150	°C

<sup>1</sup> The power supply of the device must start its ramp from 0.0 V.

<sup>2</sup> Functional operating conditions are provided with the DC electrical specifications in [Table 6](#). Absolute maximum ratings are stress ratings only; functional operation at the maxima is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device.

**Caution:** All inputs that tolerate 5 V cannot be more than 2.5 V greater than the supply voltage. This restriction applies to power-up and normal operation (that is, if the MPC860 is unpowered, voltage greater than 2.5 V must not be applied to its inputs).

<sup>3</sup> Minimum temperatures are guaranteed as ambient temperature,  $T_A$ . Maximum temperatures are guaranteed as junction temperature,  $T_j$ .

Table 6. DC Electrical Specifications (continued)

Characteristic	Symbol	Min	Max	Unit
Input leakage current, $V_{in} = 3.6$ V (except TMS, $\overline{TRST}$ , DSCK, and DSDI pins)	$I_{In}$	—	10	$\mu A$
Input leakage current, $V_{in} = 0$ V (except TMS, $\overline{TRST}$ , DSCK, and DSDI pins)	$I_{In}$	—	10	$\mu A$
Input capacitance <sup>2</sup>	$C_{in}$	—	20	pF
Output high voltage, $I_{OH} = -2.0$ mA, $V_{DDH} = 3.0$ V (except XTAL, XFC, and open-drain pins)	$V_{OH}$	2.4	—	V
Output low voltage $I_{OL} = 2.0$ mA, CLKOUT $I_{OL} = 3.2$ mA <sup>3</sup> $I_{OL} = 5.3$ mA <sup>4</sup> $I_{OL} = 7.0$ mA, TXD1/PA14, TXD2/PA12 $I_{OL} = 8.9$ mA, $\overline{TS}$ , $\overline{TA}$ , $\overline{TEA}$ , $\overline{BI}$ , $\overline{BB}$ , $\overline{HRESET}$ , $\overline{SRESET}$	$V_{OL}$	—	0.5	V

<sup>1</sup>  $V_{IL(max)}$  for the I<sup>2</sup>C interface is 0.8 V rather than the 1.5 V as specified in the I<sup>2</sup>C standard.

<sup>2</sup> Input capacitance is periodically sampled.

<sup>3</sup> A(0:31), TSIZ0/ $\overline{REG}$ , TSIZ1, D(0:31), DP(0:3)/ $\overline{IRQ}$ (3:6), RD/ $\overline{WR}$ ,  $\overline{BURST}$ ,  $\overline{RSV/IRQ2}$ , IP\_B(0:1)/IWP(0:1)/VFLS(0:1), IP\_B2/IOIS16\_B/AT2, IP\_B3/IWP2/VF2, IP\_B4/LWP0/VF0, IP\_B5/LWP1/VF1, IP\_B6/DSDI/AT0, IP\_B7/PTR/AT3, RXD1/PA15, RXD2/PA13, L1TXDB/PA11, L1RXDB/PA10, L1TXDA/PA9, L1RXDA/PA8, TIN1/L1RCLKA/BRGO1/CLK1/PA7, BRGCLK1/ $\overline{TOUT1/CLK2/PA6}$ , TIN2/L1TCLKA/BRGO2/CLK3/PA5,  $\overline{TOUT2/CLK4/PA4}$ , TIN3/BRGO3/CLK5/PA3, BRGCLK2/L1RCLKB/ $\overline{TOUT3/CLK6/PA2}$ , TIN4/BRGO4/CLK7/PA1, L1TCLKB/ $\overline{TOUT4/CLK8/PA0}$ ,  $\overline{REJECT1/SPISEL/PB31}$ , SPICLK/PB30, SPIMOSI/PB29, BRGO4/SPIMISO/PB28, BRGO1/I2CSDA/PB27, BRGO2/I2CSCL/PB26, SMTXD1/PB25, SMRXD1/PB24,  $\overline{SMSYN1/SDACK1/PB23}$ ,  $\overline{SMSYN2/SDACK2/PB22}$ , SMTXD2/L1CLKOB/PB21, SMRXD2/L1CLKOA/PB20, L1ST1/ $\overline{RTS1/PB19}$ , L1ST2/ $\overline{RTS2/PB18}$ , L1ST3/L1RQB/PB17, L1ST4/L1RQA/PB16, BRGO3/PB15,  $\overline{RSTRT1/PB14}$ , L1ST1/ $\overline{RTS1/DREQ0/PC15}$ , L1ST2/ $\overline{RTS2/DREQ1/PC14}$ , L1ST3/L1RQB/PC13, L1ST4/L1RQA/PC12,  $\overline{CTS1/PC11}$ ,  $\overline{TGATE1/CD1/PC10}$ ,  $\overline{CTS2/PC9}$ ,  $\overline{TGATE2/CD2/PC8}$ ,  $\overline{SDACK2/L1TSYNCA/PC7}$ , L1RSYNCA/PC6,  $\overline{SDACK1/L1TSYNCA/PC5}$ , L1RSYNCA/PC4, PD15, PD14, PD13, PD12, PD11, PD10, PD9, PD8, PD5, PD6, PD7, PD4, PD3, MII\_MDC, MII\_TX\_ER, MII\_EN, MII\_MDIO, and MII\_TXD[0:3]

<sup>4</sup>  $\overline{BDIP/GPL\_B(5)}$ ,  $\overline{BR}$ ,  $\overline{BG}$ ,  $\overline{FRZ/IRQ6}$ ,  $\overline{CS(0:5)}$ ,  $\overline{CS(6)/CE(1)_B}$ ,  $\overline{CS(7)/CE(2)_B}$ ,  $\overline{WE0/BS\_B0/IORD}$ ,  $\overline{WE1/BS\_B1/IOWR}$ ,  $\overline{WE2/BS\_B2/PCOE}$ ,  $\overline{WE3/BS\_B3/PCWE}$ ,  $\overline{BS\_A(0:3)}$ ,  $\overline{GPL\_A0/GPL\_B0}$ ,  $\overline{OE/GPL\_A1/GPL\_B1}$ ,  $\overline{GPL\_A(2:3)/GPL\_B(2:3)/CS(2:3)}$ , UPWAITA/ $\overline{GPL\_A4}$ , UPWAITB/ $\overline{GPL\_B4}$ ,  $\overline{GPL\_A5}$ , ALE\_A,  $\overline{CE1\_A}$ ,  $\overline{CE2\_A}$ , ALE\_B/DSCK/AT1, OP(0:1), OP2/MODCK1/ $\overline{STS}$ , OP3/MODCK2/DSDO, and BADDR(28:30)

## 9 Bus Signal Timing

Table 7 provides the bus operation timing for the MPC860 at 33, 40, 50, and 66 MHz.

The maximum bus speed supported by the MPC860 is 66 MHz. Higher-speed parts must be operated in half-speed bus mode (for example, an MPC860 used at 80 MHz must be configured for a 40-MHz bus).

The timing for the MPC860 bus shown assumes a 50-pF load for maximum delays and a 0-pF load for minimum delays.

**Table 7. Bus Operation Timings**

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B1	CLKOUT period	30.30	30.30	25.00	30.30	20.00	30.30	15.15	30.30	ns
B1a	EXTCLK to CLKOUT phase skew (EXTCLK > 15 MHz and MF <= 2)	-0.90	0.90	-0.90	0.90	-0.90	0.90	-0.90	0.90	ns
B1b	EXTCLK to CLKOUT phase skew (EXTCLK > 10 MHz and MF < 10)	-2.30	2.30	-2.30	2.30	-2.30	2.30	-2.30	2.30	ns
B1c	CLKOUT phase jitter (EXTCLK > 15 MHz and MF <= 2) <sup>1</sup>	-0.60	0.60	-0.60	0.60	-0.60	0.60	-0.60	0.60	ns
B1d	CLKOUT phase jitter <sup>1</sup>	-2.00	2.00	-2.00	2.00	-2.00	2.00	-2.00	2.00	ns
B1e	CLKOUT frequency jitter (MF < 10) <sup>1</sup>	—	0.50	—	0.50	—	0.50	—	0.50	%
B1f	CLKOUT frequency jitter (10 < MF < 500) <sup>1</sup>	—	2.00	—	2.00	—	2.00	—	2.00	%
B1g	CLKOUT frequency jitter (MF > 500) <sup>1</sup>	—	3.00	—	3.00	—	3.00	—	3.00	%
B1h	Frequency jitter on EXTCLK <sup>2</sup>	—	0.50	—	0.50	—	0.50	—	0.50	%
B2	CLKOUT pulse width low	12.12	—	10.00	—	8.00	—	6.06	—	ns
B3	CLKOUT width high	12.12	—	10.00	—	8.00	—	6.06	—	ns
B4	CLKOUT rise time <sup>3</sup>	—	4.00	—	4.00	—	4.00	—	4.00	ns
B5 <sup>33</sup>	CLKOUT fall time <sup>3</sup>	—	4.00	—	4.00	—	4.00	—	4.00	ns
B7	CLKOUT to A(0:31), BADDR(28:30), RD/WR, BURST, D(0:31), DP(0:3) invalid	7.58	—	6.25	—	5.00	—	3.80	—	ns
B7a	CLKOUT to TSIZ(0:1), REG, RSV, AT(0:3), BDIP, PTR invalid	7.58	—	6.25	—	5.00	—	3.80	—	ns
B7b	CLKOUT to BR, BG, FRZ, VFLS(0:1), VF(0:2) IWP(0:2), LWP(0:1), STS invalid <sup>4</sup>	7.58	—	6.25	—	5.00	—	3.80	—	ns
B8	CLKOUT to A(0:31), BADDR(28:30) RD/WR, BURST, D(0:31), DP(0:3) valid	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.04	ns
B8a	CLKOUT to TSIZ(0:1), REG, RSV, AT(0:3) BDIP, PTR valid	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.04	ns
B8b	CLKOUT to BR, BG, VFLS(0:1), VF(0:2), IWP(0:2), FRZ, LWP(0:1), STS valid <sup>4</sup>	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.04	ns

Table 7. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B23	CLKOUT rising edge to $\overline{CS}$ negated GPCM read access, GPCM write access ACS = 00, TRLX = 0, and CSNT = 0	2.00	8.00	2.00	8.00	2.00	8.00	2.00	8.00	ns
B24	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 0	5.58	—	4.25	—	3.00	—	1.79	—	ns
B24a	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 0	13.15	—	10.50	—	8.00	—	5.58	—	ns
B25	CLKOUT rising edge to $\overline{OE}$ , $\overline{WE}(0:3)$ asserted	—	9.00	—	9.00	—	9.00	—	9.00	ns
B26	CLKOUT rising edge to $\overline{OE}$ negated	2.00	9.00	2.00	9.00	2.00	9.00	2.00	9.00	ns
B27	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 1	35.88	—	29.25	—	23.00	—	16.94	—	ns
B27a	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 1	43.45	—	35.50	—	28.00	—	20.73	—	ns
B28	CLKOUT rising edge to $\overline{WE}(0:3)$ negated GPCM write access CSNT = 0	—	9.00	—	9.00	—	9.00	—	9.00	ns
B28a	CLKOUT falling edge to $\overline{WE}(0:3)$ negated GPCM write access TRLX = 0, 1, CSNT = 1, EBDF = 0	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.54	ns
B28b	CLKOUT falling edge to $\overline{CS}$ negated GPCM write access TRLX = 0, 1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 0	—	14.33	—	13.00	—	11.75	—	10.54	ns
B28c	CLKOUT falling edge to $\overline{WE}(0:3)$ negated GPCM write access TRLX = 0, 1, CSNT = 1 write access TRLX = 0, CSNT = 1, EBDF = 1	10.86	17.99	8.88	16.00	7.00	14.13	5.18	12.31	ns
B28d	CLKOUT falling edge to $\overline{CS}$ negated GPCM write access TRLX = 0, 1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 1	—	17.99	—	16.00	—	14.13	—	12.31	ns
B29	$\overline{WE}(0:3)$ negated to D(0:31), DP(0:3) High-Z GPCM write access CSNT = 0, EBDF = 0	5.58	—	4.25	—	3.00	—	1.79	—	ns
B29a	$\overline{WE}(0:3)$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 0	13.15	—	10.5	—	8.00	—	5.58	—	ns
B29b	$\overline{CS}$ negated to D(0:31), DP(0:3), High-Z GPCM write access, ACS = 00, TRLX = 0, 1, and CSNT = 0	5.58	—	4.25	—	3.00	—	1.79	—	ns
B29c	$\overline{CS}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 0	13.15	—	10.5	—	8.00	—	5.58	—	ns

Table 7. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B31a	CLKOUT falling edge to $\overline{CS}$ valid—as requested by control bit CST1 in the corresponding word in UPM	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.54	ns
B31b	CLKOUT rising edge to $\overline{CS}$ valid—as requested by control bit CST2 in the corresponding word in UPM	1.50	8.00	1.50	8.00	1.50	8.00	1.50	8.00	ns
B31c	CLKOUT rising edge to $\overline{CS}$ valid—as requested by control bit CST3 in the corresponding word in UPM	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.04	ns
B31d	CLKOUT falling edge to $\overline{CS}$ valid—as requested by control bit CST1 in the corresponding word in UPM, EBDF = 1	13.26	17.99	11.28	16.00	9.40	14.13	7.58	12.31	ns
B32	CLKOUT falling edge to $\overline{BS}$ valid—as requested by control bit BST4 in the corresponding word in UPM	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns
B32a	CLKOUT falling edge to $\overline{BS}$ valid—as requested by control bit BST1 in the corresponding word in UPM, EBDF = 0	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.54	ns
B32b	CLKOUT rising edge to $\overline{BS}$ valid—as requested by control bit BST2 in the corresponding word in UPM	1.50	8.00	1.50	8.00	1.50	8.00	1.50	8.00	ns
B32c	CLKOUT rising edge to $\overline{BS}$ valid—as requested by control bit BST3 in the corresponding word in UPM	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.54	ns
B32d	CLKOUT falling edge to $\overline{BS}$ valid—as requested by control bit BST1 in the corresponding word in UPM, EBDF = 1	13.26	17.99	11.28	16.00	9.40	14.13	7.58	12.31	ns
B33	CLKOUT falling edge to $\overline{GPL}$ valid—as requested by control bit GxT4 in the corresponding word in UPM	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns
B33a	CLKOUT rising edge to $\overline{GPL}$ valid—as requested by control bit GxT3 in the corresponding word in UPM	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.54	ns
B34	A(0:31), BADDR(28:30), and D(0:31) to $\overline{CS}$ valid—as requested by control bit CST4 in the corresponding word in UPM	5.58	—	4.25	—	3.00	—	1.79	—	ns
B34a	A(0:31), BADDR(28:30), and D(0:31) to $\overline{CS}$ valid—as requested by control bit CST1 in the corresponding word in UPM	13.15	—	10.50	—	8.00	—	5.58	—	ns
B34b	A(0:31), BADDR(28:30), and D(0:31) to $\overline{CS}$ valid—as requested by control bit CST2 in the corresponding word in UPM	20.73	—	16.75	—	13.00	—	9.36	—	ns

Table 7. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B35	A(0:31), BADDR(28:30) to $\overline{CS}$ valid—as requested by control bit BST4 in the corresponding word in UPM	5.58	—	4.25	—	3.00	—	1.79	—	ns
B35a	A(0:31), BADDR(28:30), and D(0:31) to $\overline{BS}$ valid—as requested by control bit BST1 in the corresponding word in UPM	13.15	—	10.50	—	8.00	—	5.58	—	ns
B35b	A(0:31), BADDR(28:30), and D(0:31) to $\overline{BS}$ valid—as requested by control bit BST2 in the corresponding word in UPM	20.73	—	16.75	—	13.00	—	9.36	—	ns
B36	A(0:31), BADDR(28:30), and D(0:31) to $\overline{GPL}$ valid—as requested by control bit GxT4 in the corresponding word in UPM	5.58	—	4.25	—	3.00	—	1.79	—	ns
B37	UPWAIT valid to CLKOUT falling edge <sup>9</sup>	6.00	—	6.00	—	6.00	—	6.00	—	ns
B38	CLKOUT falling edge to UPWAIT valid <sup>9</sup>	1.00	—	1.00	—	1.00	—	1.00	—	ns
B39	$\overline{AS}$ valid to CLKOUT rising edge <sup>10</sup>	7.00	—	7.00	—	7.00	—	7.00	—	ns
B40	A(0:31), TSIZ(0:1), RD/ $\overline{WR}$ , $\overline{BURST}$ , valid to CLKOUT rising edge	7.00	—	7.00	—	7.00	—	7.00	—	ns
B41	$\overline{TS}$ valid to CLKOUT rising edge (setup time)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B42	CLKOUT rising edge to $\overline{TS}$ valid (hold time)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B43	$\overline{AS}$ negation to memory controller signals negation	—	TBD	—	TBD	—	TBD	—	TBD	ns

<sup>1</sup> Phase and frequency jitter performance results are only valid if the input jitter is less than the prescribed value.

<sup>2</sup> If the rate of change of the frequency of EXTAL is slow (that is, it does not jump between the minimum and maximum values in one cycle) or the frequency of the jitter is fast (that is, it does not stay at an extreme value for a long time) then the maximum allowed jitter on EXTAL can be up to 2%.

<sup>3</sup> The timings specified in B4 and B5 are based on full strength clock.

<sup>4</sup> The timing for  $\overline{BR}$  output is relevant when the MPC860 is selected to work with external bus arbiter. The timing for  $\overline{BG}$  output is relevant when the MPC860 is selected to work with internal bus arbiter.

<sup>5</sup> The timing required for  $\overline{BR}$  input is relevant when the MPC860 is selected to work with internal bus arbiter. The timing for  $\overline{BG}$  input is relevant when the MPC860 is selected to work with external bus arbiter.

<sup>6</sup> The D(0:31) and DP(0:3) input timings B18 and B19 refer to the rising edge of the CLKOUT in which the  $\overline{TA}$  input signal is asserted.

<sup>7</sup> The D(0:31) and DP(0:3) input timings B20 and B21 refer to the falling edge of the CLKOUT. This timing is valid only for read accesses controlled by chip-selects under control of the UPM in the memory controller, for data beats where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

<sup>8</sup> The timing B30 refers to  $\overline{CS}$  when ACS = 00 and to  $\overline{WE}$ (0:3) when CSNT = 0.

<sup>9</sup> The signal UPWAIT is considered asynchronous to the CLKOUT and synchronized internally. The timings specified in B37 and B38 are specified to enable the freeze of the UPM output signals as described in [Figure 18](#).

<sup>10</sup> The  $\overline{AS}$  signal is considered asynchronous to the CLKOUT. The timing B39 is specified in order to allow the behavior specified in [Figure 21](#).



Figure 9 provides the timing for the input data controlled by the UPM for data beats where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

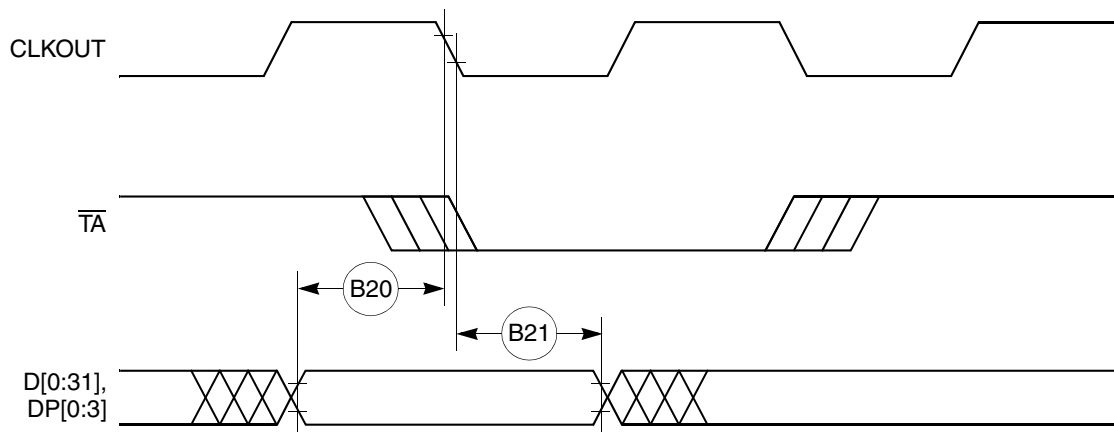


Figure 9. Input Data Timing when Controlled by UPM in the Memory Controller and DLT3 = 1

Figure 10 through Figure 13 provide the timing for the external bus read controlled by various GPCM factors.

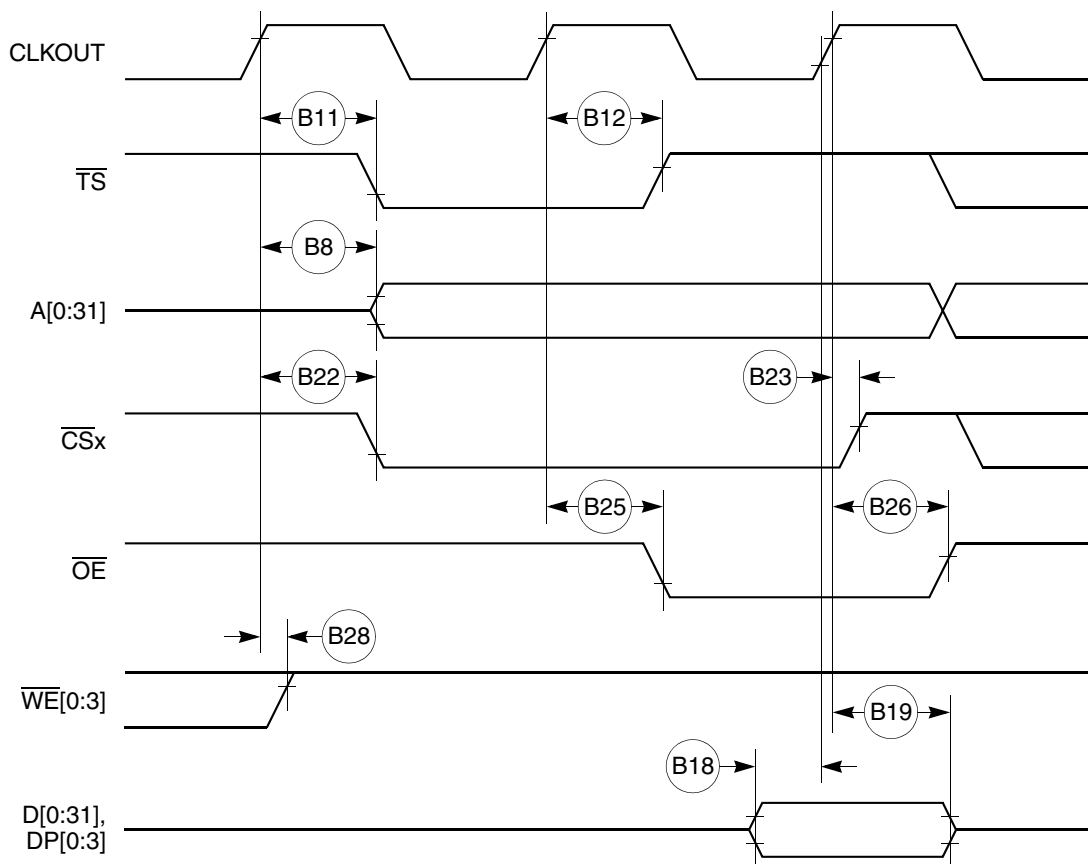


Figure 10. External Bus Read Timing (GPCM Controlled—ACS = 00)

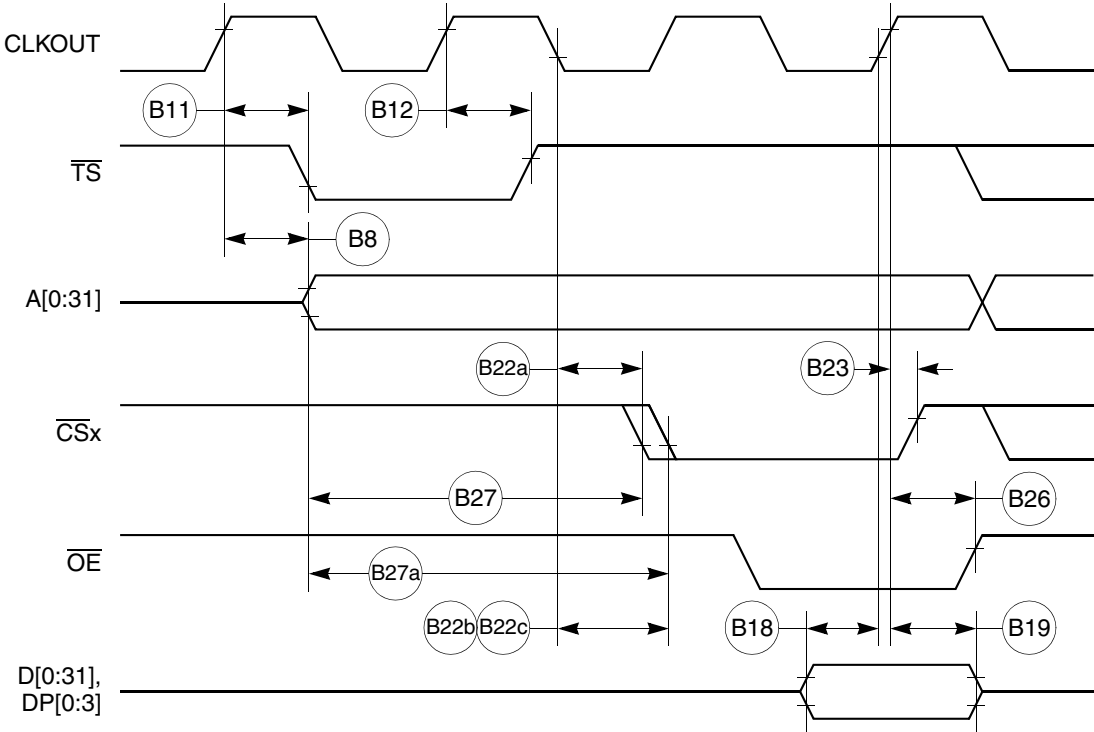


Figure 13. External Bus Read Timing (GPCM Controlled—TRLX = 0 or 1, ACS = 10, ACS = 11)

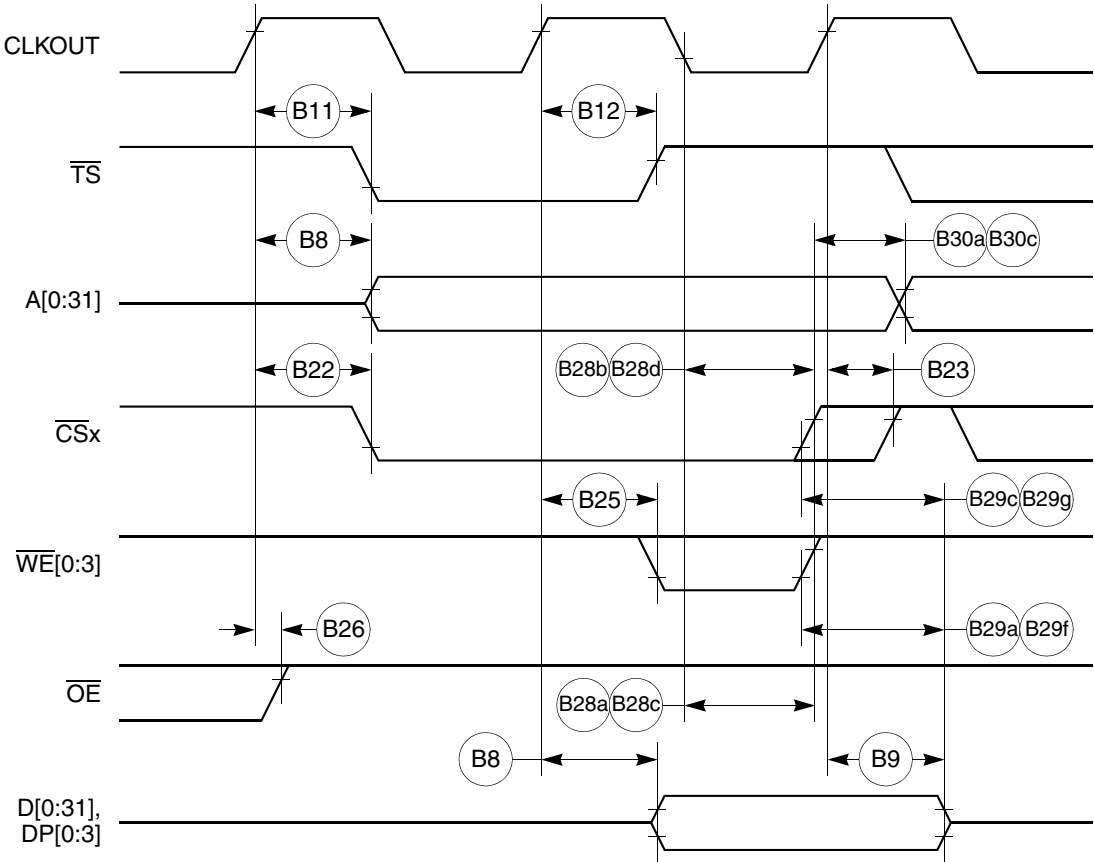


Figure 15. External Bus Write Timing (GPCM Controlled—TRLX = 0 or 1, CSNT = 1)

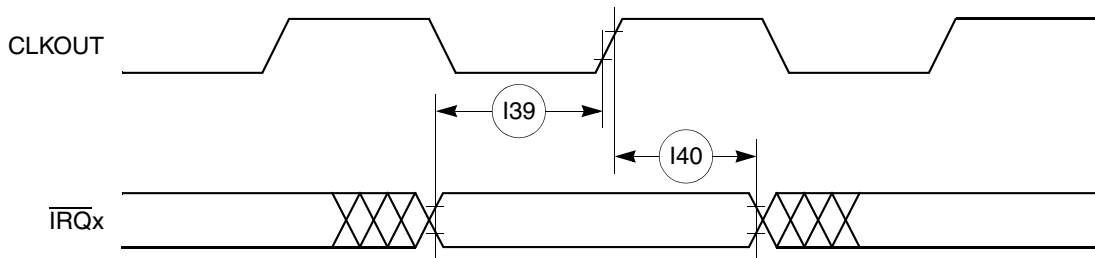
Table 8 provides interrupt timing for the MPC860.

**Table 8. Interrupt Timing**

Num	Characteristic <sup>1</sup>	All Frequencies		Unit
		Min	Max	
I39	$\overline{\text{IRQ}}_x$ valid to CLKOUT rising edge (setup time)	6.00	—	ns
I40	$\overline{\text{IRQ}}_x$ hold time after CLKOUT	2.00	—	ns
I41	$\overline{\text{IRQ}}_x$ pulse width low	3.00	—	ns
I42	$\overline{\text{IRQ}}_x$ pulse width high	3.00	—	ns
I43	$\overline{\text{IRQ}}_x$ edge-to-edge time	$4 \times T_{\text{CLOCKOUT}}$	—	—

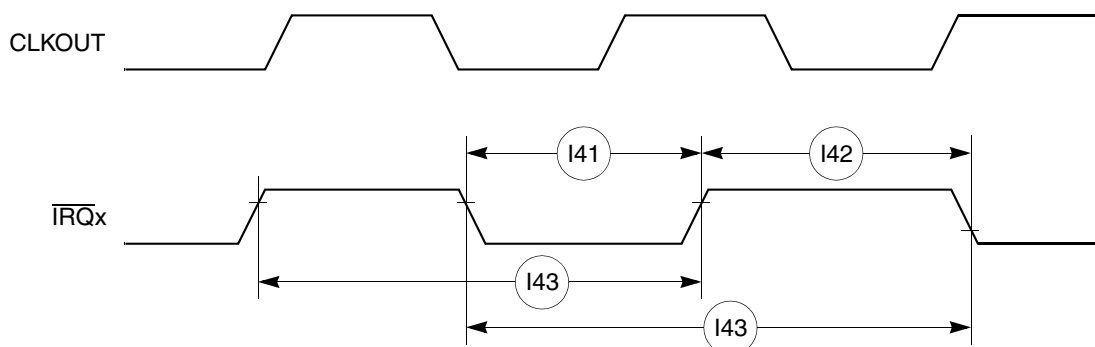
<sup>1</sup> The timings I39 and I40 describe the testing conditions under which the  $\overline{\text{IRQ}}$  lines are tested when being defined as level-sensitive. The  $\overline{\text{IRQ}}$  lines are synchronized internally and do not have to be asserted or negated with reference to the CLKOUT. The timings I41, I42, and I43 are specified to allow the correct function of the  $\overline{\text{IRQ}}$  lines detection circuitry and have no direct relation with the total system interrupt latency that the MPC860 is able to support.

Figure 23 provides the interrupt detection timing for the external level-sensitive lines.



**Figure 23. Interrupt Detection Timing for External Level Sensitive Lines**

Figure 24 provides the interrupt detection timing for the external edge-sensitive lines.



**Figure 24. Interrupt Detection Timing for External Edge Sensitive Lines**

Figure 25 provides the PCMCIA access cycle timing for the external bus read.

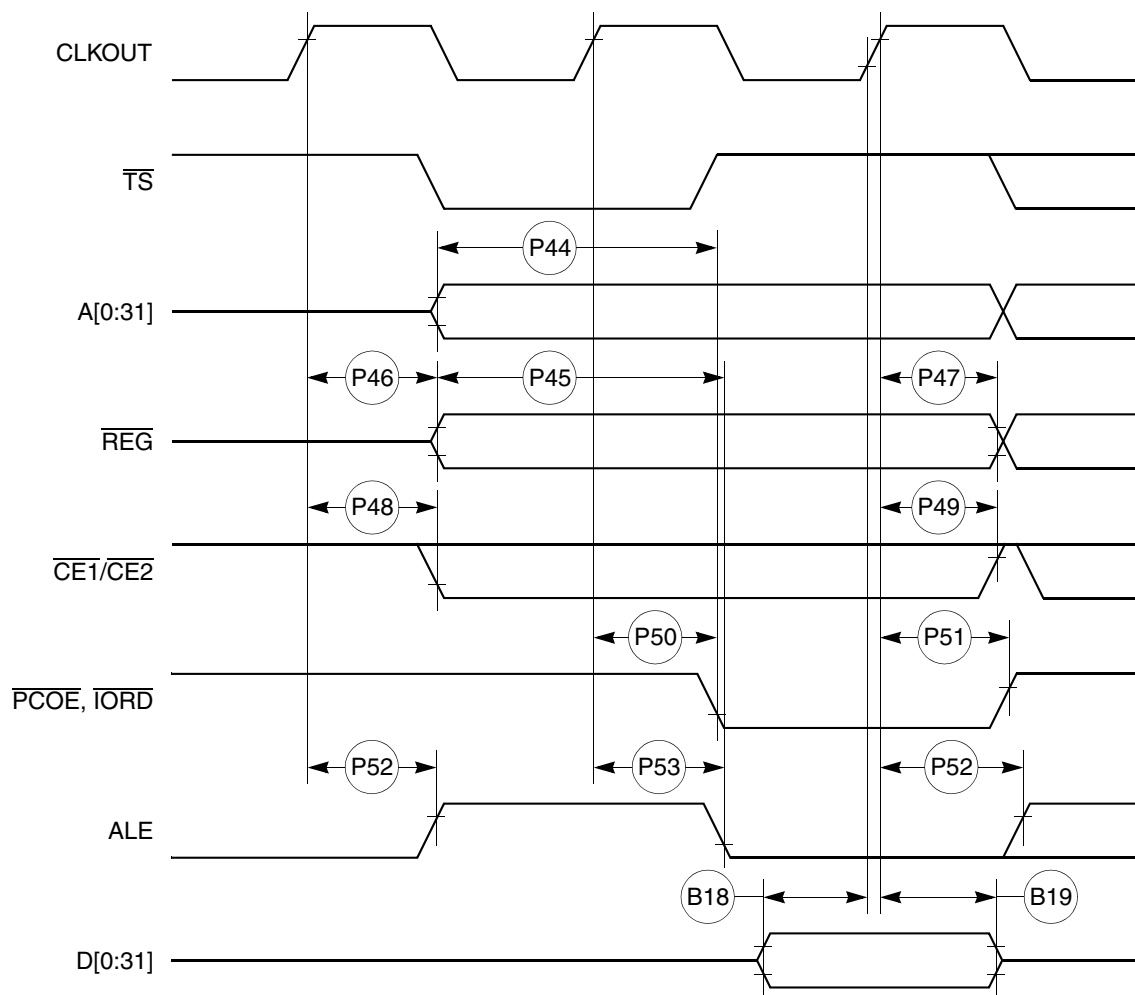


Figure 25. PCMCIA Access Cycle Timing External Bus Read

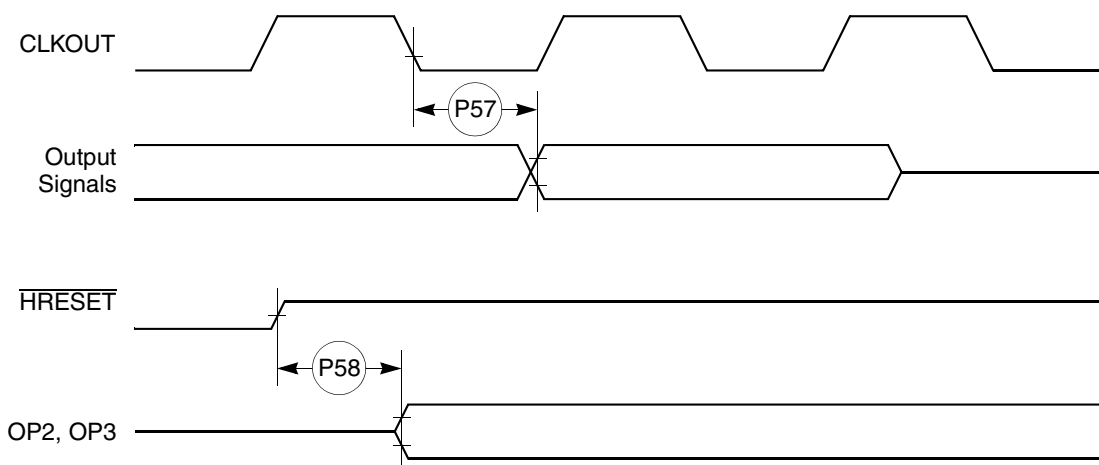
Table 10 shows the PCMCIA port timing for the MPC860.

**Table 10. PCMCIA Port Timing**

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
P57	CLKOUT to OPx valid	—	19.00	—	19.00	—	19.00	—	19.00	ns
P58	$\overline{\text{HRESET}}$ negated to OPx drive <sup>1</sup>	25.73	—	21.75	—	18.00	—	14.36	—	ns
P59	IP_Xx valid to CLKOUT rising edge	5.00	—	5.00	—	5.00	—	5.00	—	ns
P60	CLKOUT rising edge to IP_Xx invalid	1.00	—	1.00	—	1.00	—	1.00	—	ns

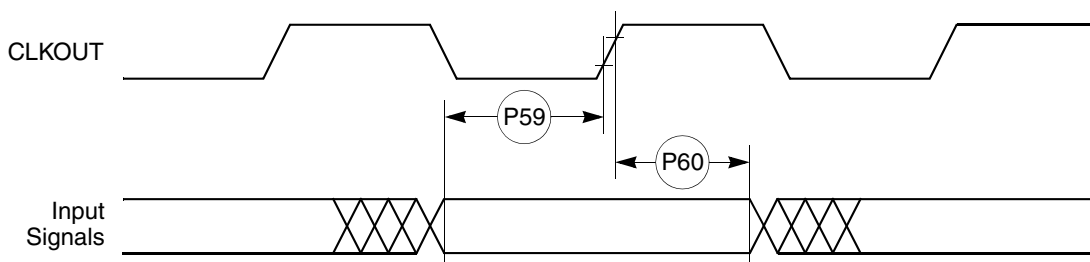
<sup>1</sup> OP2 and OP3 only.

Figure 28 provides the PCMCIA output port timing for the MPC860.



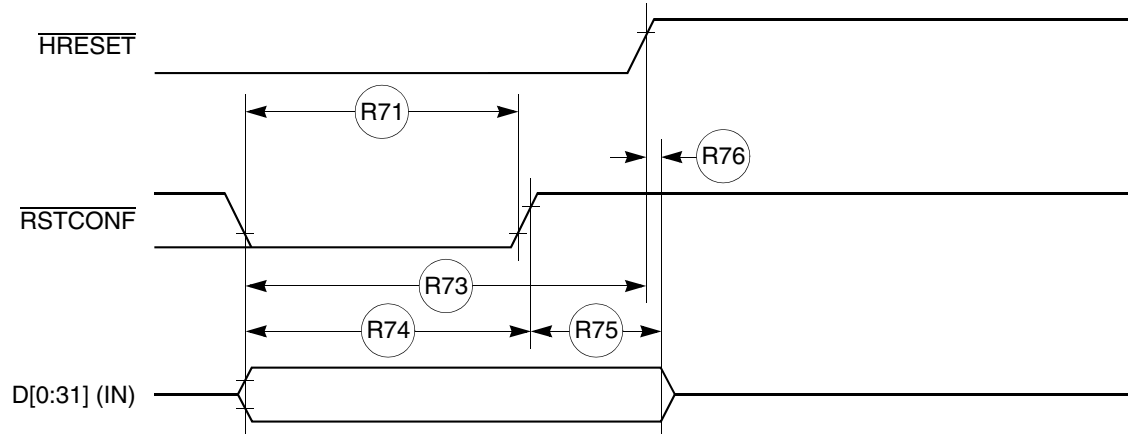
**Figure 28. PCMCIA Output Port Timing**

Figure 29 provides the PCMCIA output port timing for the MPC860.



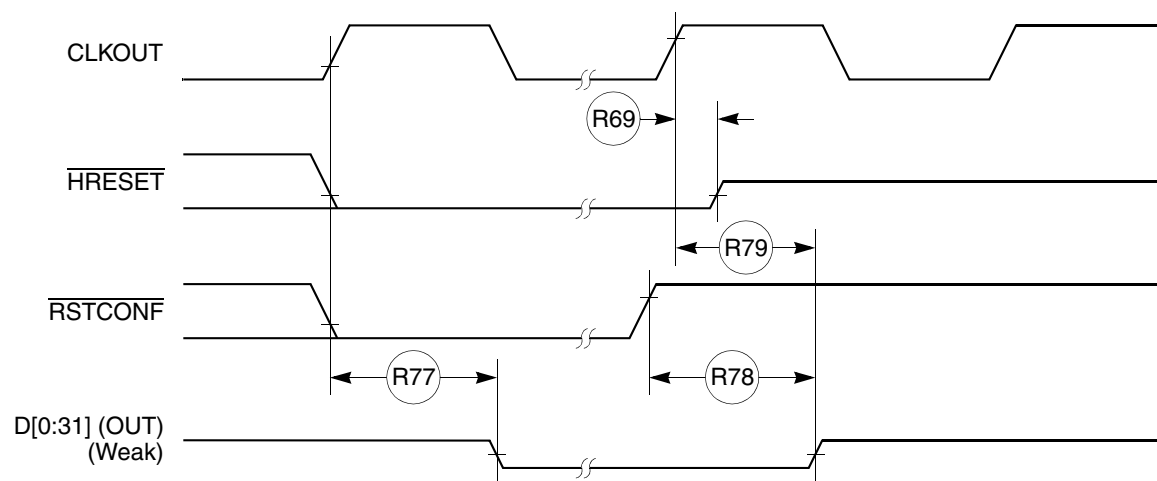
**Figure 29. PCMCIA Input Port Timing**

Figure 32 shows the reset timing for the data bus configuration.



**Figure 32. Reset Timing—Configuration from Data Bus**

Figure 33 provides the reset timing for the data bus weak drive during configuration.



**Figure 33. Reset Timing—Data Bus Weak Drive During Configuration**

Figure 34 provides the reset timing for the debug port configuration.

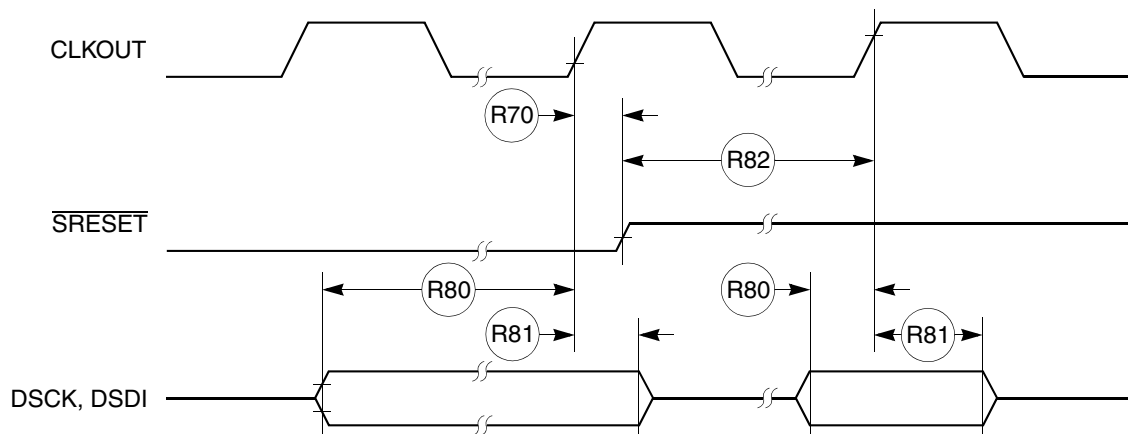


Figure 34. Reset Timing—Debug Port Configuration

## 10 IEEE 1149.1 Electrical Specifications

Table 13 provides the JTAG timings for the MPC860 shown in Figure 35 through Figure 38.

Table 13. JTAG Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
J82	TCK cycle time	100.00	—	ns
J83	TCK clock pulse width measured at 1.5 V	40.00	—	ns
J84	TCK rise and fall times	0.00	10.00	ns
J85	TMS, TDI data setup time	5.00	—	ns
J86	TMS, TDI data hold time	25.00	—	ns
J87	TCK low to TDO data valid	—	27.00	ns
J88	TCK low to TDO data invalid	0.00	—	ns
J89	TCK low to TDO high impedance	—	20.00	ns
J90	$\overline{\text{TRST}}$ assert time	100.00	—	ns
J91	$\overline{\text{TRST}}$ setup time to TCK low	40.00	—	ns
J92	TCK falling edge to output valid	—	50.00	ns
J93	TCK falling edge to output valid out of high impedance	—	50.00	ns
J94	TCK falling edge to output high impedance	—	50.00	ns
J95	Boundary scan input valid to TCK rising edge	50.00	—	ns
J96	TCK rising edge to boundary scan input invalid	50.00	—	ns



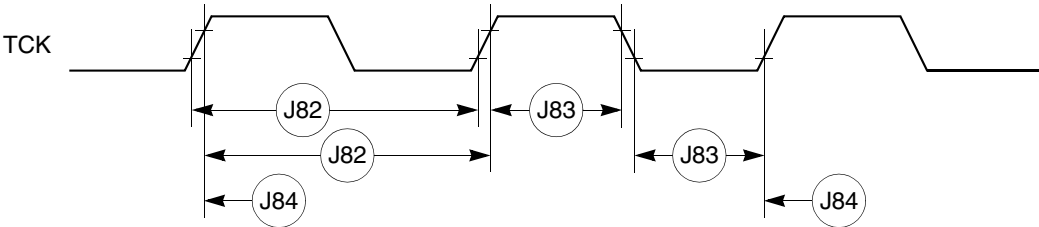


Figure 35. JTAG Test Clock Input Timing

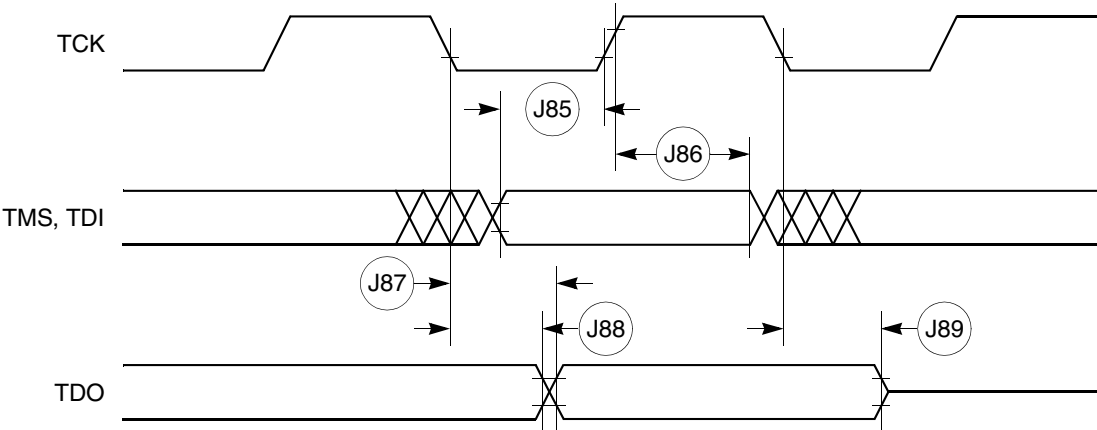


Figure 36. JTAG Test Access Port Timing Diagram

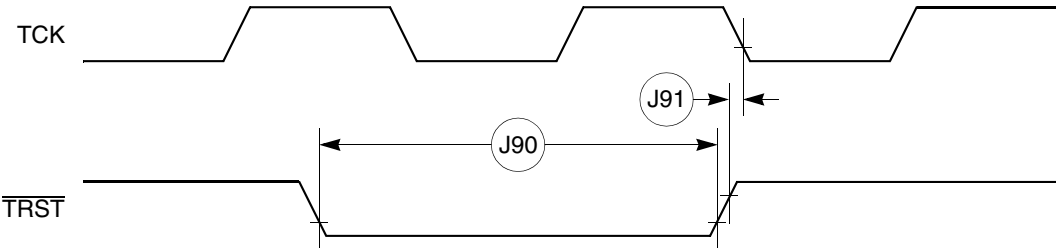


Figure 37. JTAG  $\overline{\text{TRST}}$  Timing Diagram

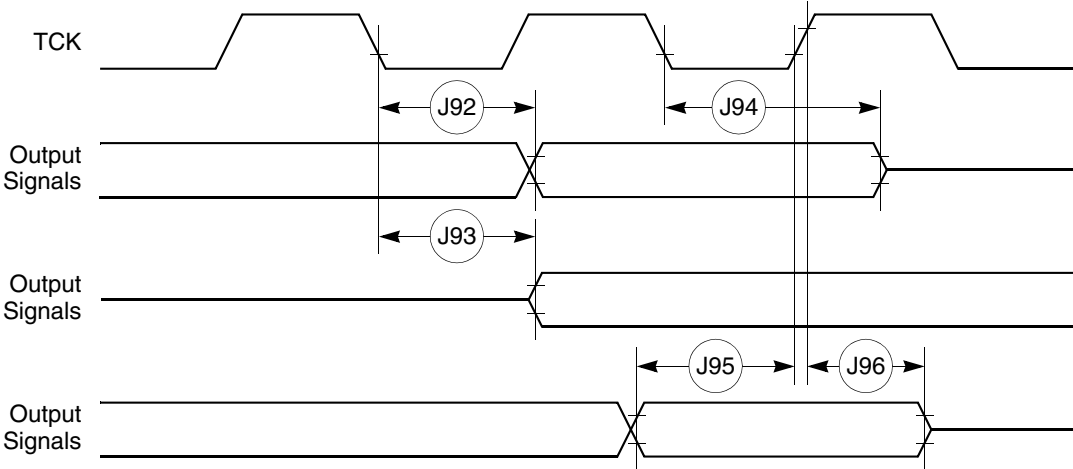
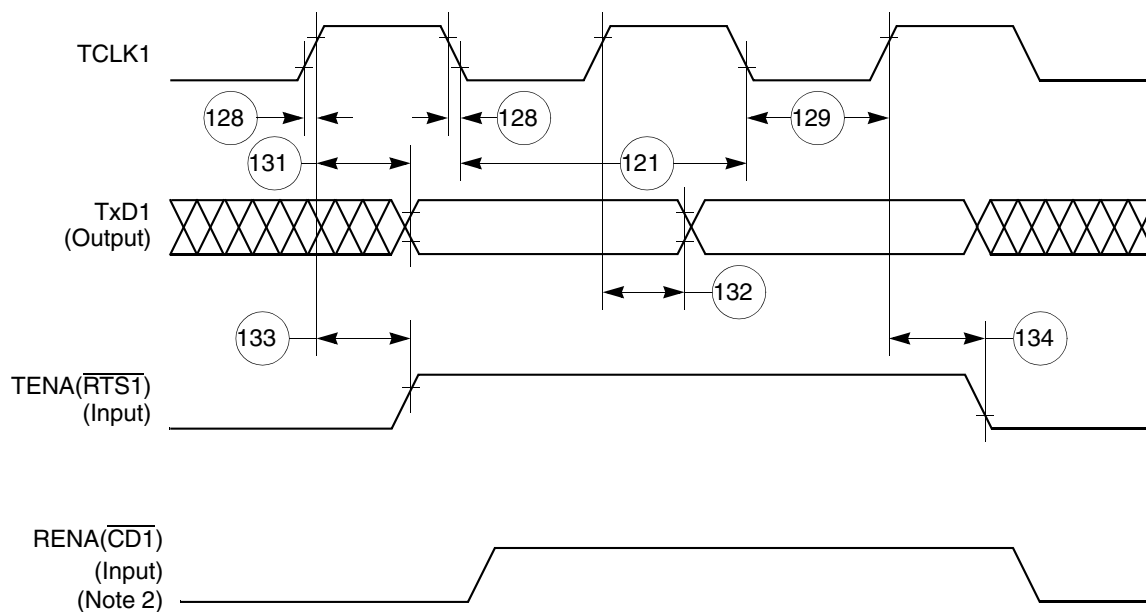


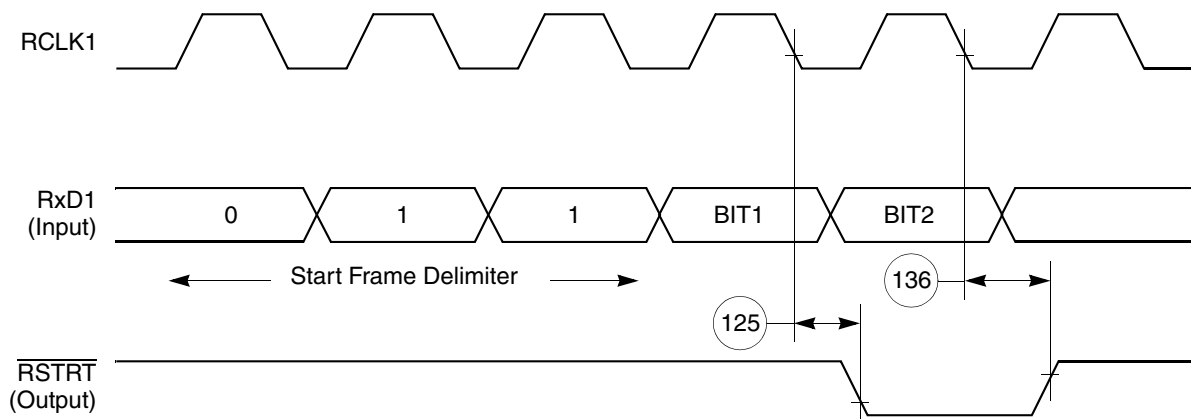
Figure 38. Boundary Scan (JTAG) Timing Diagram



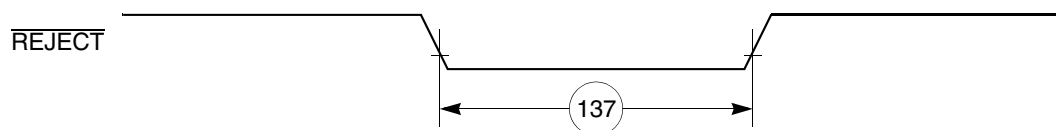
**Notes:**

1. Transmit clock invert (TCI) bit in GSMR is set.
2. If RENA is deasserted before TENA, or RENA is not asserted at all during transmit, then the CSL bit is set in the buffer descriptor at the end of the frame transmission.

**Figure 61. Ethernet Transmit Timing Diagram**



**Figure 62. CAM Interface Receive Start Timing Diagram**



**Figure 63. CAM Interface  $\overline{\text{REJECT}}$  Timing Diagram**

# 13 FEC Electrical Characteristics

This section provides the AC electrical specifications for the Fast Ethernet controller (FEC). Note that the timing specifications for the MII signals are independent of system clock frequency (part speed designation). Also, MII signals use TTL signal levels compatible with devices operating at either 5.0 V or 3.3 V.

## 13.1 MII Receive Signal Timing (MII\_RXD[3:0], MII\_RX\_DV, MII\_RX\_ER, MII\_RX\_CLK)

The receiver functions correctly up to a MII\_RX\_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed the MII\_RX\_CLK frequency – 1%.

Table 29 provides information on the MII receive signal timing.

Table 29. MII Receive Signal Timing

Num	Characteristic	Min	Max	Unit
M1	MII_RXD[3:0], MII_RX_DV, MII_RX_ER to MII_RX_CLK setup	5	—	ns
M2	MII_RX_CLK to MII_RXD[3:0], MII_RX_DV, MII_RX_ER hold	5	—	ns
M3	MII_RX_CLK pulse width high	35%	65%	MII_RX_CLK period
M4	MII_RX_CLK pulse width low	35%	65%	MII_RX_CLK period

Figure 72 shows MII receive signal timing.

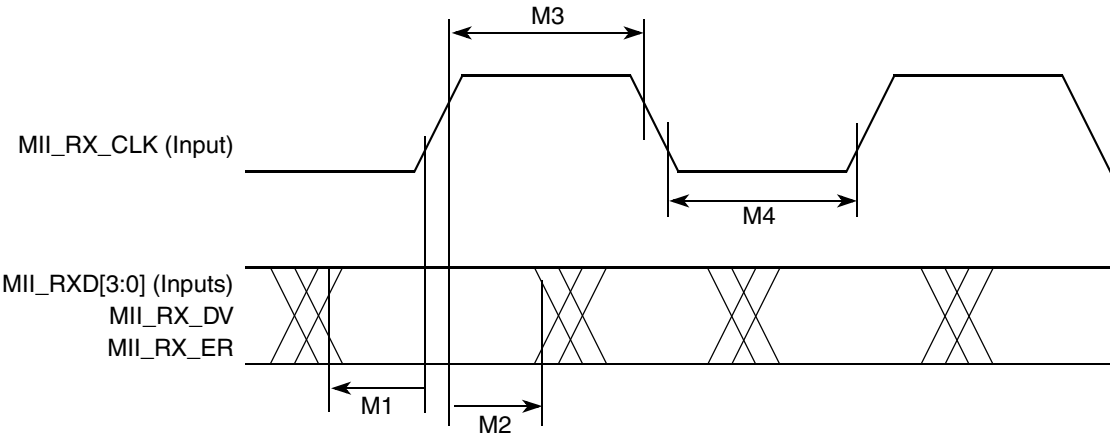


Figure 72. MII Receive Signal Timing Diagram

# 14.3 Mechanical Dimensions of the PBGA Package

Figure 77 shows the mechanical dimensions of the ZP PBGA package.

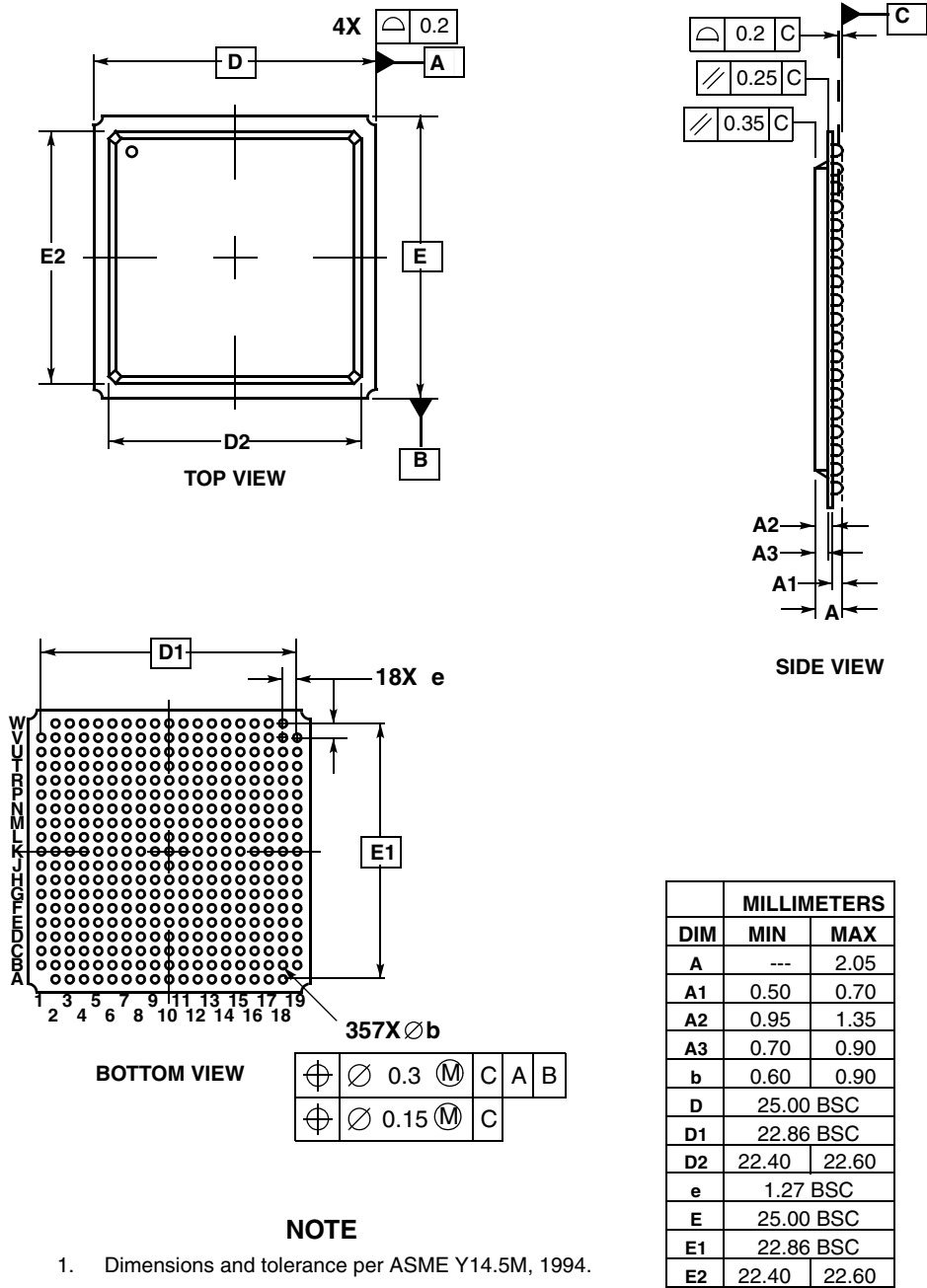


Figure 77. Mechanical Dimensions and Bottom Surface Nomenclature of the ZP PBGA Package

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