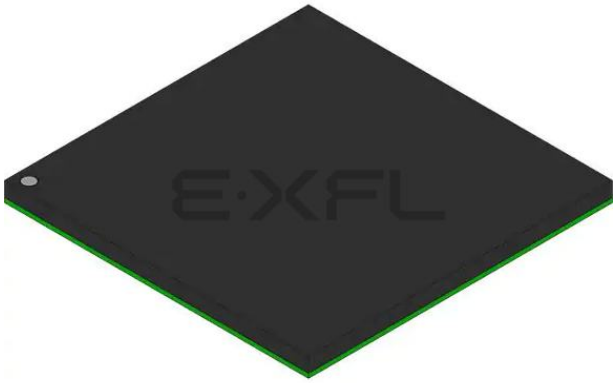

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	50MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (2)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 95°C (TA)
Security Features	-
Package / Case	357-BBGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc860dezq50d4

- System integration unit (SIU)
  - Bus monitor
  - Software watchdog
  - Periodic interrupt timer (PIT)
  - Low-power stop mode
  - Clock synthesizer
  - Decrementer, time base, and real-time clock (RTC)
  - Reset controller
  - IEEE 1149.1™ Std. test access port (JTAG)
- Interrupts
  - Seven external interrupt request (IRQ) lines
  - 12 port pins with interrupt capability
  - 23 internal interrupt sources
  - Programmable priority between SCCs
  - Programmable highest priority request
- 10/100 Mbps Ethernet support, fully compliant with the IEEE 802.3u® Standard (not available when using ATM over UTOPIA interface)
- ATM support compliant with ATM forum UNI 4.0 specification
  - Cell processing up to 50–70 Mbps at 50-MHz system clock
  - Cell multiplexing/demultiplexing
  - Support of AAL5 and AAL0 protocols on a per-VC basis. AAL0 support enables OAM and software implementation of other protocols.
  - ATM pace control (APC) scheduler, providing direct support for constant bit rate (CBR) and unspecified bit rate (UBR) and providing control mechanisms enabling software support of available bit rate (ABR)
  - Physical interface support for UTOPIA (10/100-Mbps is not supported with this interface) and byte-aligned serial (for example, T1/E1/ADSL)
  - UTOPIA-mode ATM supports level-1 master with cell-level handshake, multi-PHY (up to four physical layer devices), connection to 25-, 51-, or 155-Mbps framers, and UTOPIA/system clock ratios of 1/2 or 1/3.
  - Serial-mode ATM connection supports transmission convergence (TC) function for T1/E1/ADSL lines, cell delineation, cell payload scrambling/descrambling, automatic idle/unassigned cell insertion/stripping, header error control (HEC) generation, checking, and statistics.
- Communications processor module (CPM)
  - RISC communications processor (CP)
  - Communication-specific commands (for example, GRACEFUL STOP TRANSMIT, ENTER HUNT MODE, and RESTART TRANSMIT)
  - Supports continuous mode transmission and reception on all serial channels

Table 7. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B29d	$\overline{WE}$(0:3) negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 0	43.45	—	35.5	—	28.00	—	20.73	—	ns
B29e	$\overline{CS}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 0	43.45	—	35.5	—	28.00	—	29.73	—	ns
B29f	$\overline{WE}$(0:3) negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 1	8.86	—	6.88	—	5.00	—	3.18	—	ns
B29g	$\overline{CS}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 1	8.86	—	6.88	—	5.00	—	3.18	—	ns
B29h	$\overline{WE}$(0:3) negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 1	38.67	—	31.38	—	24.50	—	17.83	—	ns
B29i	$\overline{CS}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 1	38.67	—	31.38	—	24.50	—	17.83	—	ns
B30	$\overline{CS}$, $\overline{WE}$(0:3) negated to A(0:31), BADDR(28:30) invalid GPCM write access [8]	5.58	—	4.25	—	3.00	—	1.79	—	ns
B30a	$\overline{WE}$(0:3) negated to A(0:31), BADDR(28:30) invalid GPCM, write access, TRLX = 0, CSNT = 1, $\overline{CS}$ negated to A(0:31) invalid GPCM write access, TRLX = 0, CSNT = 1 ACS = 10, or ACS = 11, EBDF = 0	13.15	—	10.50	—	8.00	—	5.58	—	ns
B30b	$\overline{WE}$(0:3) negated to A(0:31), invalid GPCM BADDR(28:30) invalid GPCM write access, TRLX = 1, CSNT = 1. $\overline{CS}$ negated to A(0:31), Invalid GPCM, write access, TRLX = 1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 0	43.45	—	35.50	—	28.00	—	20.73	—	ns
B30c	$\overline{WE}$(0:3) negated to A(0:31), BADDR(28:30) invalid GPCM write access, TRLX = 0, CSNT = 1. $\overline{CS}$ negated to A(0:31) invalid GPCM write access, TRLX = 0, CSNT = 1, ACS = 10, ACS = 11, EBDF = 1	8.36	—	6.38	—	4.50	—	2.68	—	ns
B30d	$\overline{WE}$(0:3) negated to A(0:31), BADDR(28:30) invalid GPCM write access, TRLX = 1, CSNT =1. $\overline{CS}$ negated to A(0:31) invalid GPCM write access TRLX = 1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 1	38.67	—	31.38	—	24.50	—	17.83	—	ns
B31	CLKOUT falling edge to $\overline{CS}$ valid—as requested by control bit CST4 in the corresponding word in UPM	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns

Table 7. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B31a	CLKOUT falling edge to $\overline{CS}$ valid—as requested by control bit CST1 in the corresponding word in UPM	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.54	ns
B31b	CLKOUT rising edge to $\overline{CS}$ valid—as requested by control bit CST2 in the corresponding word in UPM	1.50	8.00	1.50	8.00	1.50	8.00	1.50	8.00	ns
B31c	CLKOUT rising edge to $\overline{CS}$ valid—as requested by control bit CST3 in the corresponding word in UPM	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.04	ns
B31d	CLKOUT falling edge to $\overline{CS}$ valid—as requested by control bit CST1 in the corresponding word in UPM, EBDF = 1	13.26	17.99	11.28	16.00	9.40	14.13	7.58	12.31	ns
B32	CLKOUT falling edge to $\overline{BS}$ valid—as requested by control bit BST4 in the corresponding word in UPM	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns
B32a	CLKOUT falling edge to $\overline{BS}$ valid—as requested by control bit BST1 in the corresponding word in UPM, EBDF = 0	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.54	ns
B32b	CLKOUT rising edge to $\overline{BS}$ valid—as requested by control bit BST2 in the corresponding word in UPM	1.50	8.00	1.50	8.00	1.50	8.00	1.50	8.00	ns
B32c	CLKOUT rising edge to $\overline{BS}$ valid—as requested by control bit BST3 in the corresponding word in UPM	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.54	ns
B32d	CLKOUT falling edge to $\overline{BS}$ valid—as requested by control bit BST1 in the corresponding word in UPM, EBDF = 1	13.26	17.99	11.28	16.00	9.40	14.13	7.58	12.31	ns
B33	CLKOUT falling edge to $\overline{GPL}$ valid—as requested by control bit GxT4 in the corresponding word in UPM	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns
B33a	CLKOUT rising edge to $\overline{GPL}$ valid—as requested by control bit GxT3 in the corresponding word in UPM	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.54	ns
B34	A(0:31), BADDR(28:30), and D(0:31) to $\overline{CS}$ valid—as requested by control bit CST4 in the corresponding word in UPM	5.58	—	4.25	—	3.00	—	1.79	—	ns
B34a	A(0:31), BADDR(28:30), and D(0:31) to $\overline{CS}$ valid—as requested by control bit CST1 in the corresponding word in UPM	13.15	—	10.50	—	8.00	—	5.58	—	ns
B34b	A(0:31), BADDR(28:30), and D(0:31) to $\overline{CS}$ valid—as requested by control bit CST2 in the corresponding word in UPM	20.73	—	16.75	—	13.00	—	9.36	—	ns

Table 7. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B35	A(0:31), BADDR(28:30) to $\overline{CS}$ valid—as requested by control bit BST4 in the corresponding word in UPM	5.58	—	4.25	—	3.00	—	1.79	—	ns
B35a	A(0:31), BADDR(28:30), and D(0:31) to $\overline{BS}$ valid—as requested by control bit BST1 in the corresponding word in UPM	13.15	—	10.50	—	8.00	—	5.58	—	ns
B35b	A(0:31), BADDR(28:30), and D(0:31) to $\overline{BS}$ valid—as requested by control bit BST2 in the corresponding word in UPM	20.73	—	16.75	—	13.00	—	9.36	—	ns
B36	A(0:31), BADDR(28:30), and D(0:31) to $\overline{GPL}$ valid—as requested by control bit GxT4 in the corresponding word in UPM	5.58	—	4.25	—	3.00	—	1.79	—	ns
B37	UPWAIT valid to CLKOUT falling edge[9]	6.00	—	6.00	—	6.00	—	6.00	—	ns
B38	CLKOUT falling edge to UPWAIT valid[9]	1.00	—	1.00	—	1.00	—	1.00	—	ns
B39	$\overline{AS}$ valid to CLKOUT rising edge[10]	7.00	—	7.00	—	7.00	—	7.00	—	ns
B40	A(0:31), TSIZ(0:1), RD/$\overline{WR}$, $\overline{BURST}$, valid to CLKOUT rising edge	7.00	—	7.00	—	7.00	—	7.00	—	ns
B41	$\overline{TS}$ valid to CLKOUT rising edge (setup time)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B42	CLKOUT rising edge to $\overline{TS}$ valid (hold time)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B43	$\overline{AS}$ negation to memory controller signals negation	—	TBD	—	TBD	—	TBD	—	TBD	ns

1 Phase and frequency jitter performance results are only valid if the input jitter is less than the prescribed value.

2 If the rate of change of the frequency of EXTAL is slow (that is, it does not jump between the minimum and maximum values in one cycle) or the frequency of the jitter is fast (that is, it does not stay at an extreme value for a long time) then the maximum allowed jitter on EXTAL can be up to 2%.

3 The timings specified in B4 and B5 are based on full strength clock.

4 The timing for $\overline{BR}$ output is relevant when the MPC860 is selected to work with external bus arbiter. The timing for $\overline{BG}$ output is relevant when the MPC860 is selected to work with internal bus arbiter.

5 The timing required for $\overline{BR}$ input is relevant when the MPC860 is selected to work with internal bus arbiter. The timing for $\overline{BG}$ input is relevant when the MPC860 is selected to work with external bus arbiter.

6 The D(0:31) and DP(0:3) input timings B18 and B19 refer to the rising edge of the CLKOUT in which the $\overline{TA}$ input signal is asserted.

7 The D(0:31) and DP(0:3) input timings B20 and B21 refer to the falling edge of the CLKOUT. This timing is valid only for read accesses controlled by chip-selects under control of the UPM in the memory controller, for data beats where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

8 The timing B30 refers to $\overline{CS}$ when ACS = 00 and to $\overline{WE}$(0:3) when CSNT = 0.

9 The signal UPWAIT is considered asynchronous to the CLKOUT and synchronized internally. The timings specified in B37 and B38 are specified to enable the freeze of the UPM output signals as described in Figure 18.

10 The $\overline{AS}$ signal is considered asynchronous to the CLKOUT. The timing B39 is specified in order to allow the behavior specified in Figure 21.

Figure 26 provides the PCMCIA access cycle timing for the external bus write.

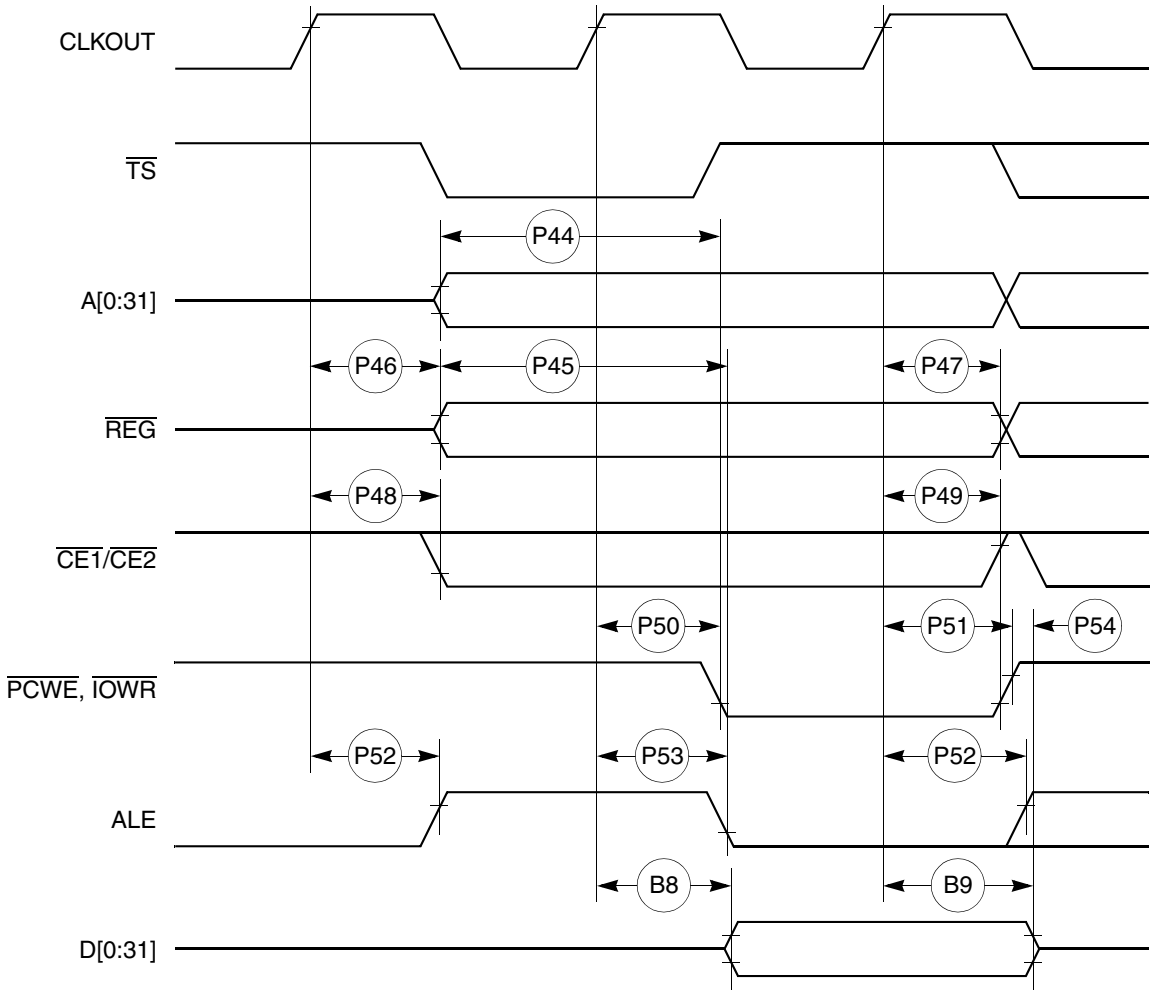


Figure 26. PCMCIA Access Cycle Timing External Bus Write

Figure 27 provides the PCMCIA WAIT signal detection timing.

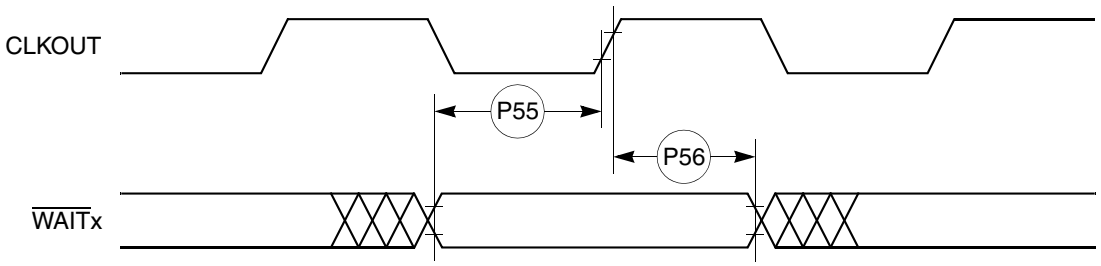


Figure 27. PCMCIA WAIT Signal Detection Timing

Figure 32 shows the reset timing for the data bus configuration.

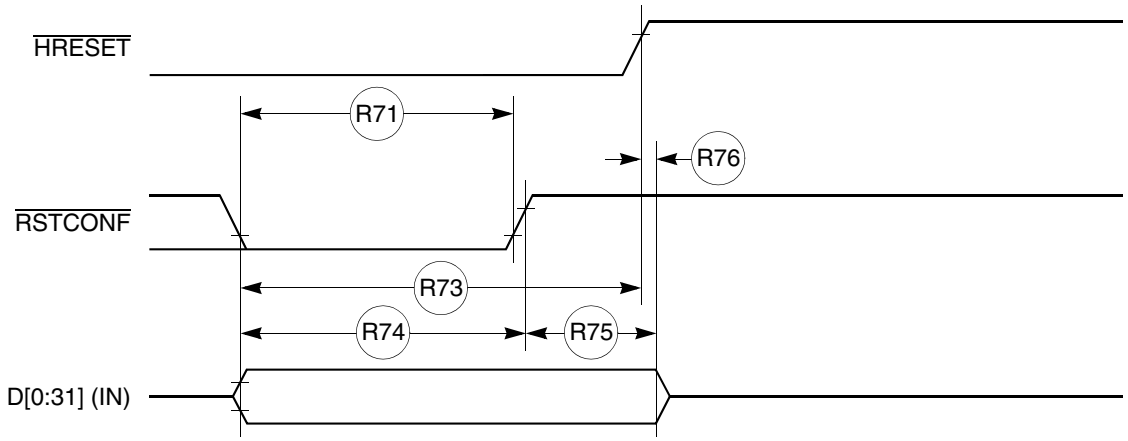


Figure 32. Reset Timing—Configuration from Data Bus

Figure 33 provides the reset timing for the data bus weak drive during configuration.

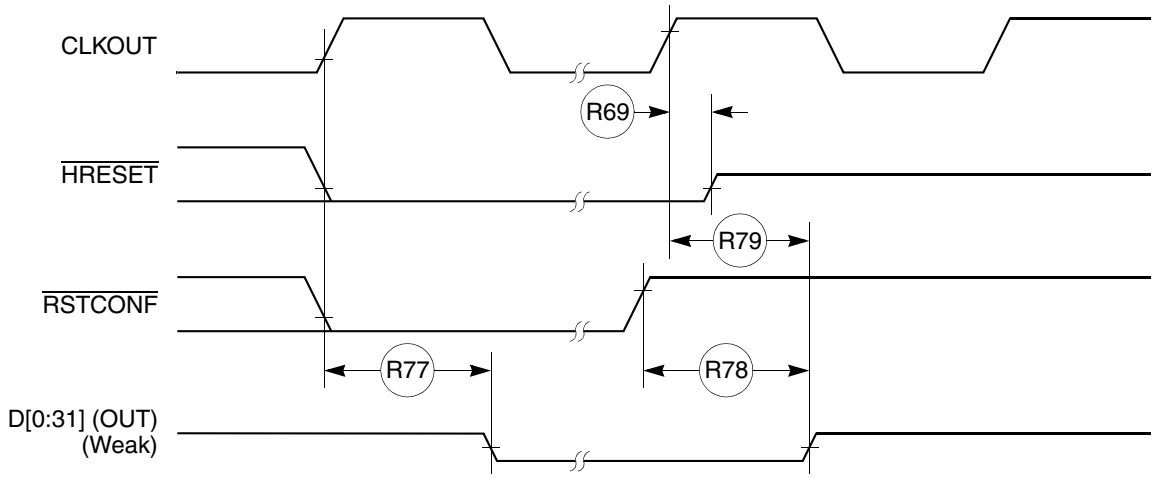


Figure 33. Reset Timing—Data Bus Weak Drive During Configuration

11.4 Baud Rate Generator AC Electrical Specifications

Table 17 provides the baud rate generator timings as shown in Figure 49.

Table 17. Baud Rate Generator Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
50	BRGO rise and fall time	—	10	ns
51	BRGO duty cycle	40	60	%
52	BRGO cycle	40	—	ns

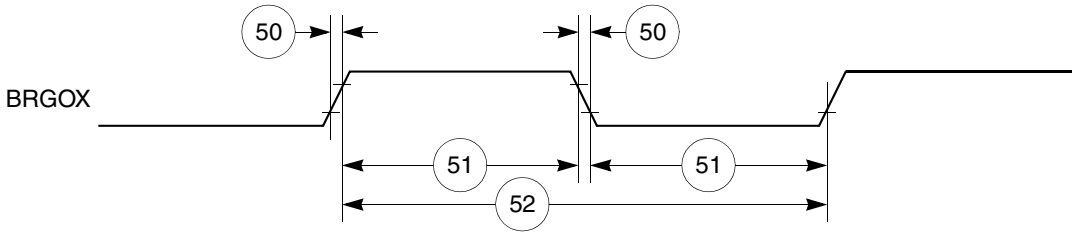


Figure 49. Baud Rate Generator Timing Diagram

11.5 Timer AC Electrical Specifications

Table 18 provides the general-purpose timer timings as shown in Figure 50.

Table 18. Timer Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
61	TIN/$\overline{\text{TGATE}}$ rise and fall time	10	—	ns
62	TIN/$\overline{\text{TGATE}}$ low time	1	—	CLK
63	TIN/$\overline{\text{TGATE}}$ high time	2	—	CLK
64	TIN/$\overline{\text{TGATE}}$ cycle time	3	—	CLK
65	CLKO low to $\overline{\text{TOUT}}$ valid	3	25	ns

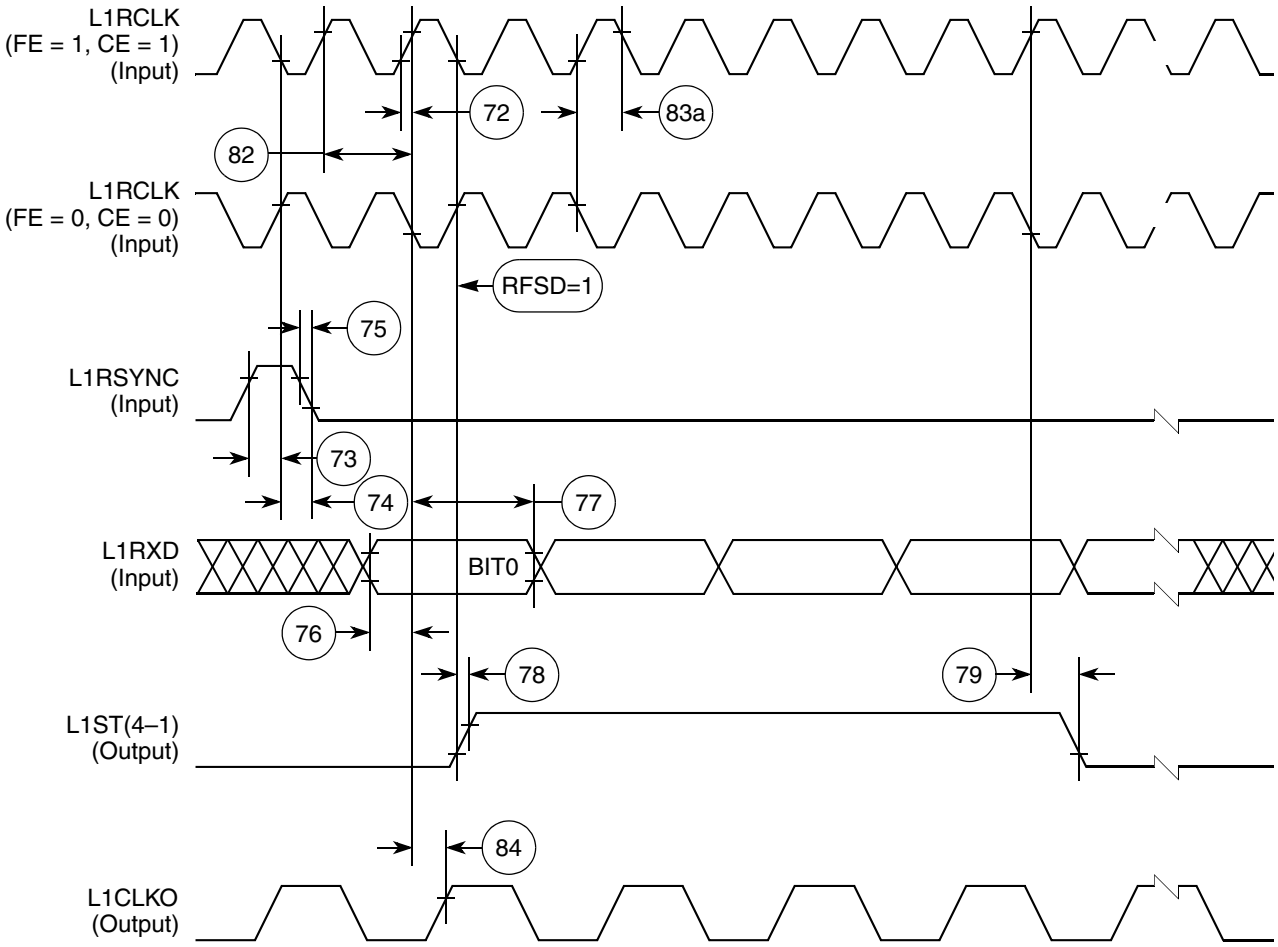


Figure 52. SI Receive Timing with Double-Speed Clocking (DSC = 1)

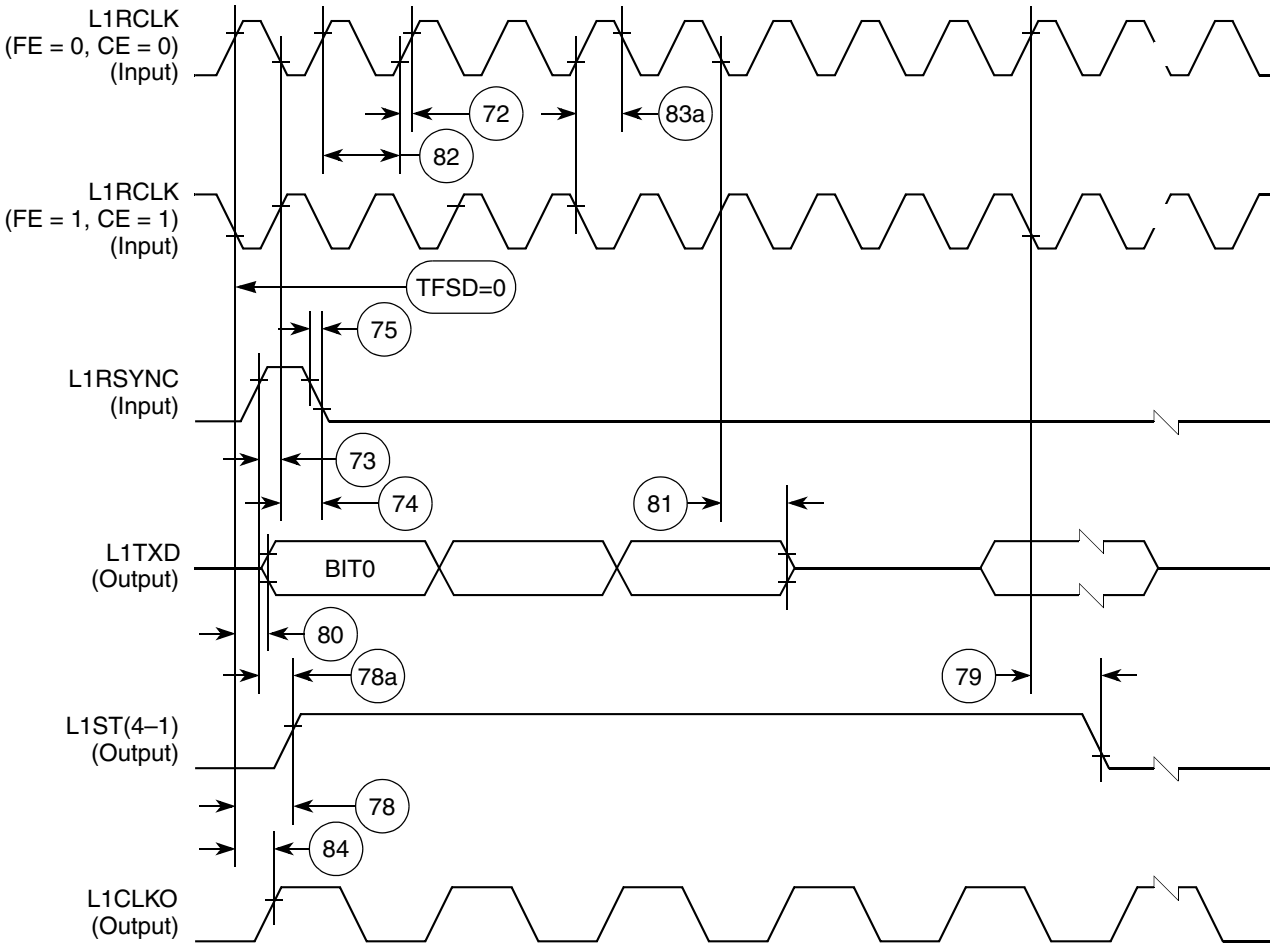


Figure 54. SI Transmit Timing with Double Speed Clocking (DSC = 1)

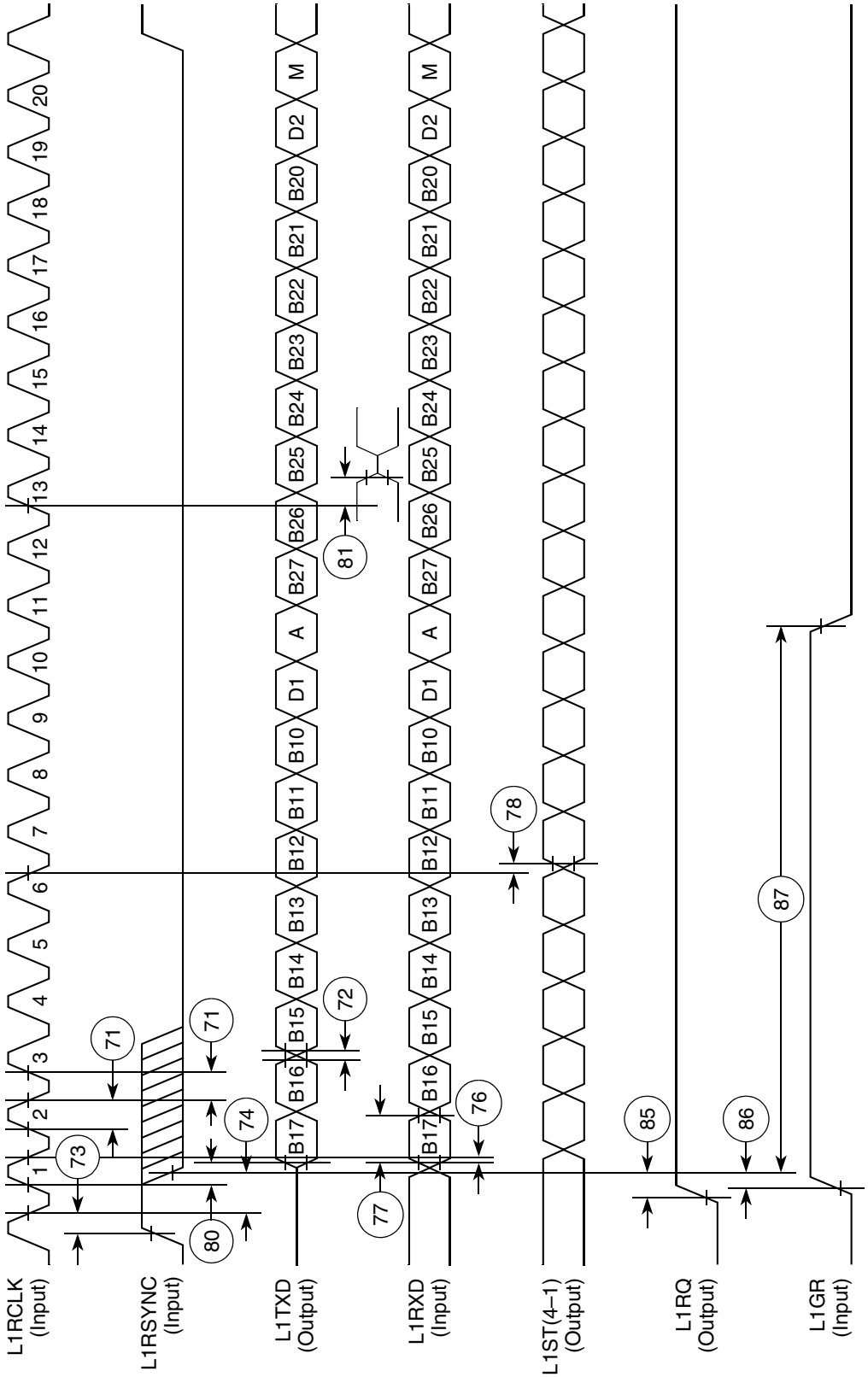


Figure 55. IDL Timing

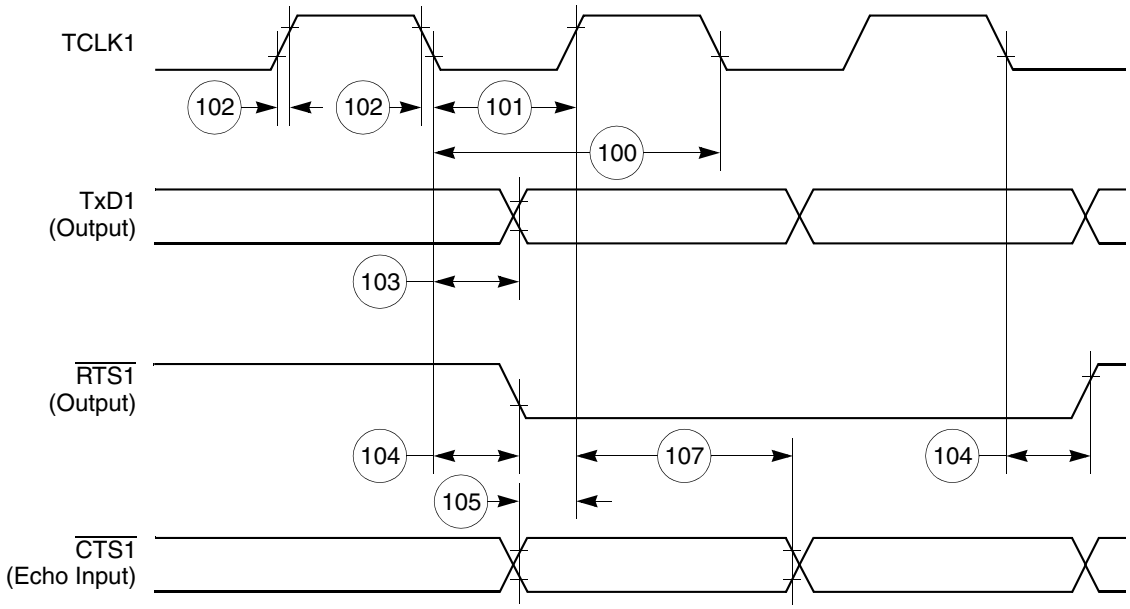


Figure 58. HDLC Bus Timing Diagram

11.8 Ethernet Electrical Specifications

Table 22 provides the Ethernet timings as shown in Figure 59 through Figure 63.

Table 22. Ethernet Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
120	CLSN width high	40	—	ns
121	RCLK1 rise/fall time	—	15	ns
122	RCLK1 width low	40	—	ns
123	RCLK1 clock period[1]	80	120	ns
124	RXD1 setup time	20	—	ns
125	RXD1 hold time	5	—	ns
126	RENA active delay (from RCLK1 rising edge of the last data bit)	10	—	ns
127	RENA width low	100	—	ns
128	TCLK1 rise/fall time	—	15	ns
129	TCLK1 width low	40	—	ns
130	TCLK1 clock period[1]	99	101	ns
131	TXD1 active delay (from TCLK1 rising edge)	10	50	ns
132	TXD1 inactive delay (from TCLK1 rising edge)	10	50	ns
133	TENA active delay (from TCLK1 rising edge)	10	50	ns
134	TENA inactive delay (from TCLK1 rising edge)	10	50	ns

Table 22. Ethernet Timing (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
135	$\overline{\text{RSTRT}}$ active delay (from TCLK1 falling edge)	10	50	ns
136	$\overline{\text{RSTRT}}$ inactive delay (from TCLK1 falling edge)	10	50	ns
137	$\overline{\text{REJECT}}$ width low	1	—	CLK
138	CLKO1 low to $\overline{\text{SDACK}}$ asserted[2]	—	20	ns
139	CLKO1 low to $\overline{\text{SDACK}}$ negated[2]	—	20	ns

1 The ratios SYNCCLK/RCLK1 and SYNCCLK/TCLK1 must be greater than or equal to 2/1.
2 $\overline{\text{SDACK}}$ is asserted whenever the SDMA writes the incoming frame DA into memory.

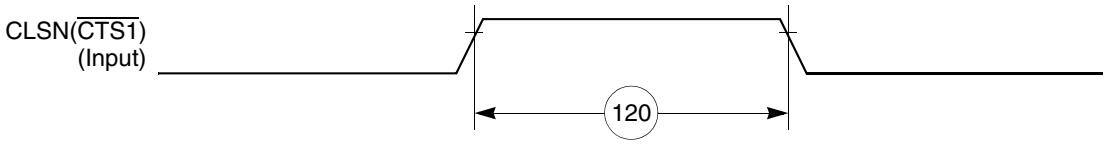


Figure 59. Ethernet Collision Timing Diagram

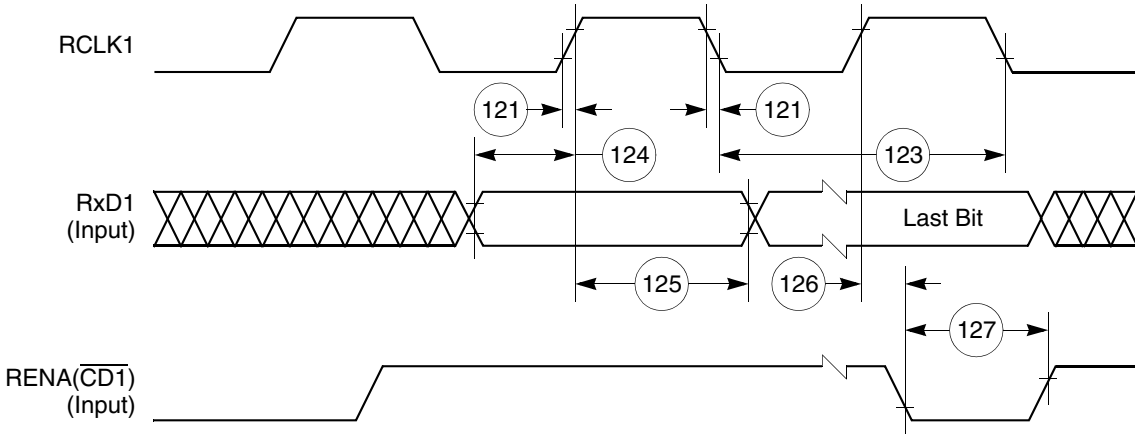


Figure 60. Ethernet Receive Timing Diagram

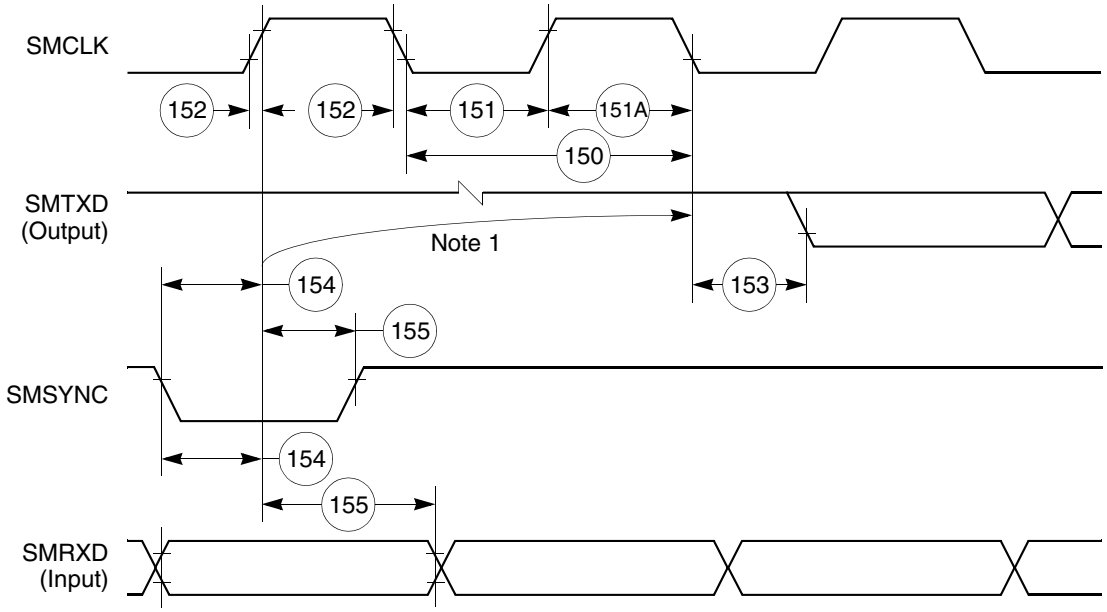
11.9 SMC Transparent AC Electrical Specifications

Table 23 provides the SMC transparent timings as shown in Figure 64.

Table 23. SMC Transparent Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
150	SMCLK clock period[1]	100	—	ns
151	SMCLK width low	50	—	ns
151A	SMCLK width high	50	—	ns
152	SMCLK rise/fall time	—	15	ns
153	SMTXD active delay (from SMCLK falling edge)	10	50	ns
154	SMRXD/SMSYNC setup time	20	—	ns
155	RXD1/SMSYNC hold time	5	—	ns

1 SYNCCLK must be at least twice as fast as SMCLK.



Note:
1. This delay is equal to an integer number of character-length clocks.

Figure 64. SMC Transparent Timing Diagram

11.10 SPI Master AC Electrical Specifications

Table 24 provides the SPI master timings as shown in Figure 65 and Figure 66.

Table 24. SPI Master Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
160	MASTER cycle time	4	1024	t_{cyc}
161	MASTER clock (SCK) high or low time	2	512	t_{cyc}
162	MASTER data setup time (inputs)	50	—	ns
163	Master data hold time (inputs)	0	—	ns
164	Master data valid (after SCK edge)	—	20	ns
165	Master data hold time (outputs)	0	—	ns
166	Rise time output	—	15	ns
167	Fall time output	—	15	ns

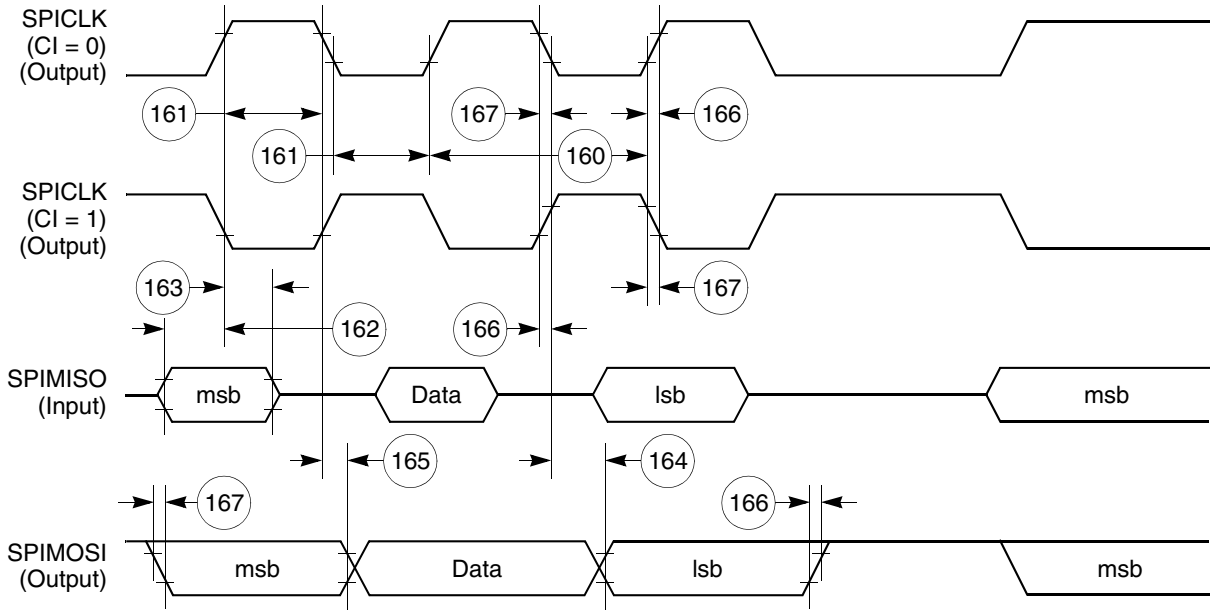


Figure 65. SPI Master (CP = 0) Timing Diagram

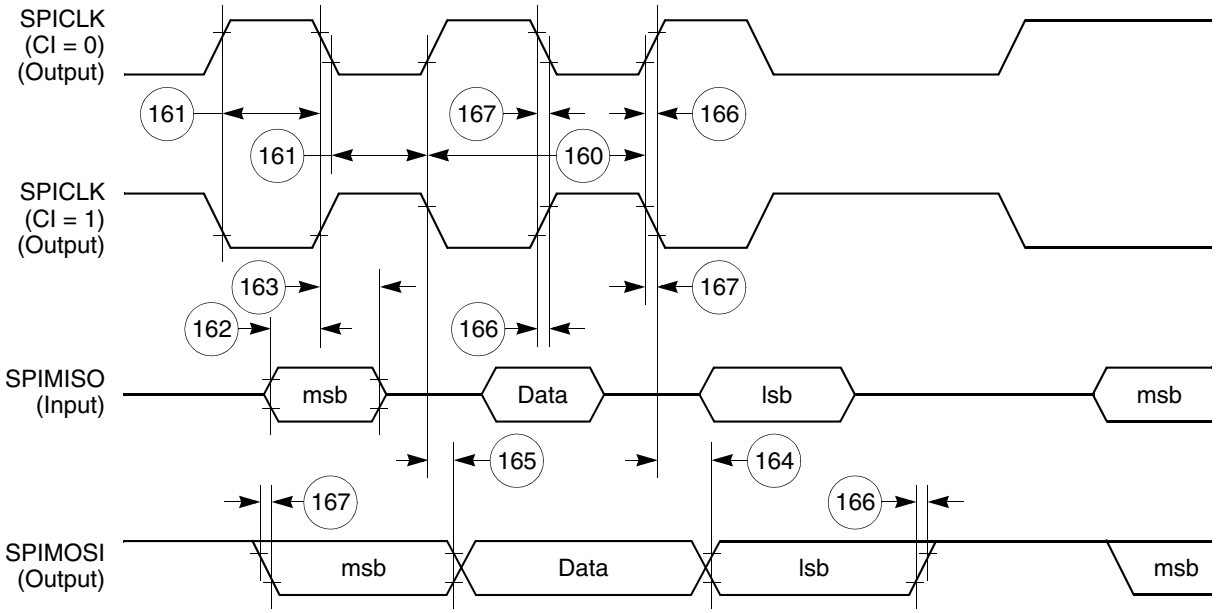


Figure 66. SPI Master (CP = 1) Timing Diagram

11.11 SPI Slave AC Electrical Specifications

Table 25 provides the SPI slave timings as shown in Figure 67 and Figure 68.

Table 25. SPI Slave Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
170	Slave cycle time	2	—	t_{cyc}
171	Slave enable lead time	15	—	ns
172	Slave enable lag time	15	—	ns
173	Slave clock (SPICLK) high or low time	1	—	t_{cyc}
174	Slave sequential transfer delay (does not require deselect)	1	—	t_{cyc}
175	Slave data setup time (inputs)	20	—	ns
176	Slave data hold time (inputs)	20	—	ns
177	Slave access time	—	50	ns

11.12 I²C AC Electrical Specifications

Table 26 provides the I²C (SCL < 100 kHz) timings.

Table 26. I²C Timing (SCL < 100 kHz)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
200	SCL clock frequency (slave)	0	100	kHz
200	SCL clock frequency (master)[1]	1.5	100	kHz
202	Bus free time between transmissions	4.7	—	µs
203	Low period of SCL	4.7	—	µs
204	High period of SCL	4.0	—	µs
205	Start condition setup time	4.7	—	µs
206	Start condition hold time	4.0	—	µs
207	Data hold time	0	—	µs
208	Data setup time	250	—	ns
209	SDL/SCL rise time	—	1	µs
210	SDL/SCL fall time	—	300	ns
211	Stop condition setup time	4.7	—	µs

1 SCL frequency is given by SCL = BRGCLK_frequency / ((BRG register + 3 × pre_scaler × 2).
The ratio SYNCCLK/(BRGCLK/pre_scaler) must be greater than or equal to 4/1.

Table 27 provides the I²C (SCL > 100 kHz) timings.

Table 27. . I²C Timing (SCL > 100 kHz)

Num	Characteristic	Expression	All Frequencies		Unit
			Min	Max	
200	SCL clock frequency (slave)	fSCL	0	BRGCLK/48	Hz
200	SCL clock frequency (master)[1]	fSCL	BRGCLK/16512	BRGCLK/48	Hz
202	Bus free time between transmissions		1/(2.2 * fSCL)	—	s
203	Low period of SCL		1/(2.2 * fSCL)	—	s
204	High period of SCL		1/(2.2 * fSCL)	—	s
205	Start condition setup time		1/(2.2 * fSCL)	—	s
206	Start condition hold time		1/(2.2 * fSCL)	—	s
207	Data hold time		0	—	s
208	Data setup time		1/(40 * fSCL)	—	s
209	SDL/SCL rise time		—	1/(10 * fSCL)	s
210	SDL/SCL fall time		—	1/(33 * fSCL)	s
211	Stop condition setup time		1/2(2.2 * fSCL)	—	s

1 SCL frequency is given by SCL = BRGCLK_frequency / ((BRG register + 3) × pre_scaler × 2).
The ratio SYNCCLK/(BRGCLK / pre_scaler) must be greater than or equal to 4/1.

Figure 69 shows the I^2C bus timing.

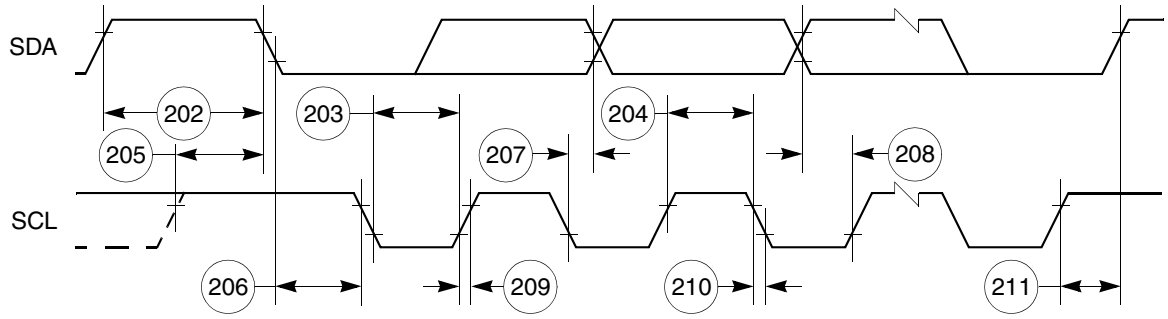


Figure 69. I^2C Bus Timing Diagram

12 UTOPIA AC Electrical Specifications

Table 28 shows the AC electrical specifications for the UTOPIA interface.

Table 28. UTOPIA AC Electrical Specifications

Num	Signal Characteristic	Direction	Min	Max	Unit
U1	UtpClk rise/fall time (Internal clock option)	Output	—	3.5	ns
	Duty cycle		50	50	%
	Frequency		—	50	MHz
U1a	UtpClk rise/fall time (external clock option)	Input	—	3.5	ns
	Duty cycle		40	60	%
	Frequency		—	50	MHz
U2	$\overline{\text{RxEnb}}$ and $\overline{\text{TxEnb}}$ active delay	Output	2	16	ns
U3	UTPB, SOC, Rxclav and Txclav setup time	Input	8	—	ns
U4	UTPB, SOC, Rxclav and Txclav hold time	Input	1	—	ns
U5	UTPB, SOC active delay (and PHREQ and PHSEL active delay in MPHY mode)	Output	2	16	ns

Table 34 identifies the packages and operating frequencies available for the MPC860.

Table 34. MPC860 Family Package/Frequency Availability

Package Type	Freq. (MHz) / Temp. (Tj)	Package	Order Number
Ball grid array ZP suffix—leaded ZQ suffix—leaded VR suffix—lead-free	50 0° to 95°C	ZP/ZQ[1]	MPC855TZQ50D4 MPC860DEZQ50D4 MPC860DTZQ50D4 MPC860ENZQ50D4 MPC860SRZQ50D4 MPC860TZQ50D4 MPC860DPZQ50D4 MPC860PZQ50D4
		Tape and Reel	MPC855TZQ50D4R2 MPC860DEZQ50D4R2 MPC860ENZQ50D4R2 MPC860SRZQ50D4R2 MPC860TZQ50D4R2 MPC860DPZQ50D4R2 MPC855TVR50D4R2 MPC860ENVR50D4R2 MPC860SRVR50D4R2 MPC860TVR50D4R2
		VR	MPC855TVR50D4 MPC860DEVR50D4 MPC860DPVR50D4 MPC860DTVR50D4 MPC860ENVR50D4 MPC860PVR50D4 MPC860SRVR50D4 MPC860TVR50D4
	66 0° to 95°C	ZP/ZQ[1]	MPC855TZQ66D4 MPC860DEZQ66D4 MPC860DTZQ66D4 MPC860ENZQ66D4 MPC860SRZQ66D4 MPC860TZQ66D4 MPC860DPZQ66D4 MPC860PZQ66D4
		Tape and Reel	MPC860SRZQ66D4R2 MPC860PZQ66D4R2
		VR	MPC855TVR66D4 MPC860DEVR66D4 MPC860DPVR66D4 MPC860DTVR66D4 MPC860ENVR66D4 MPC860PVR66D4 MPC860SRVR66D4 MPC860TVR66D4

Table 34. MPC860 Family Package/Frequency Availability (continued)

Package Type	Freq. (MHz) / Temp. (Tj)	Package	Order Number
Ball grid array *(continued)* ZP suffix—leaded ZQ suffix—leaded VR suffix—lead-free	80 0° to 95°C	ZP/ZQ[1]	MPC855TZQ80D4 MPC860DEZQ80D4 MPC860DTZQ80D4 MPC860ENZQ80D4 MPC860SRZQ80D4 MPC860TZQ80D4 MPC860DPZQ80D4 MPC860PZQ80D4
		Tape and Reel	MPC860PZQ80D4R2 MPC860PVR80D4R2
		VR	MPC855TVR80D4 MPC860DEVR80D4 MPC860DPVR80D4 MPC860ENVR80D4 MPC860PVR80D4 MPC860SRVR80D4 MPC860TVR80D4
Ball grid array (CZP suffix) CZP suffix—leaded CZQ suffix—leaded CVR suffix—lead-free	50 –40° to 95°C	ZP/ZQ[1]	MPC855TCZQ50D4 MPC855TCVR50D4 MPC860DECZQ50D4 MPC860DTCZQ50D4 MPC860ENCZQ50D4 MPC860SRCZQ50D4 MPC860TCZQ50D4 MPC860DPCZQ50D4 MPC860PCZQ50D4
		Tape and Reel	MPC855TCZQ50D4R2 MC860ENCVR50D4R2
		CVR	MPC860DECVR50D4 MPC860DTCVR50D4 MPC860ENCVR50D4 MPC860PCVR50D4 MPC860SRCVR50D4 MPC860TCVR50D4
	66 –40° to 95°C	ZP/ZQ[1]	MPC855TCZQ66D4 MPC855TCVR66D4 MPC860ENCZQ66D4 MPC860SRCZQ66D4 MPC860TCZQ66D4 MPC860DPCZQ66D4 MPC860PCZQ66D4
		CVR	MPC860DTCVR66D4 MPC860ENCVR66D4 MPC860PCVR66D4 MPC860SRCVR66D4 MPC860TCVR66D4

[1] The ZP package is no longer recommended for use. The ZQ package replaces the ZP package.

15 Document Revision History

Table 35 lists significant changes between revisions of this hardware specification.

Table 35. Document Revision History

Revision	Date	Changes
10	09/2015	In Table 34, moved MPC855TCVR50D4 and MPC855TCVR66D4 under the extended temperature (–40° to 95°C) and removed MC860ENCVR50D4R2 from the normal temperature Tape and Reel.
9	10/2011	Updated orderable part numbers in Table 34, “MPC860 Family Package/Frequency Availability.”
8	08/2007	• Updated template. • On page 1, added a second paragraph. • After Table 2, inserted a new figure showing the undershoot/overshoot voltage (Figure 1) and renumbered the rest of the figures. • In Figure 3, changed all reference voltage measurement points from 0.2 and 0.8 V to 50% level. • In Table 16, changed num 46 description to read, “$\overline{TA}$ assertion to rising edge ...” • In Figure 46, changed $\overline{TA}$ to reflect the rising edge of the clock.
7.0	9/2004	• Added a tablefootnote to Table 6 DC Electrical Specifications about meeting the VIL Max of the I2C Standard • Replaced the thermal characteristics in Table 4 by the ZQ package • Add the new parts to the Ordering and Availablity Chart in Table 34 • Added the mechanical spec of the ZQ package in Figure 78 • Removed all of the old revisions from Table 5
6.3	9/2003	• Added Section 11.2 on the Port C interrupt pins • Nontechnical reformatting
6.2	8/2003	• Changed B28a through B28d and B29d to show that TRLX can be 0 or 1 • Changed reference documentation to reflect the Rev 2 MPC860 PowerQUICC Family Users Manual • Nontechnical reformatting
6.1	11/2002	• Corrected UTOPIA RXenb* and TXenb* timing values • Changed incorrect usage of Vcc to Vdd • Corrected dual port RAM to 8 Kbytes
6	10/2002	• Added the MPC855T. Corrected Figure 26 on page -36.
5.1	11/2001	• Revised template format, removed references to MAC functionality, changed Table 7 B23 max value @ 66 MHz from 2ns to 8ns, added this revision history table