NXP USA Inc. - MPC860DPVR50D4 Datasheet



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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	50MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (2), 10/100Mbps (1)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 95°C (TA)
Security Features	-
Package / Case	357-BBGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc860dpvr50d4

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2 Features

The following list summarizes the key MPC860 features:

- Embedded single-issue, 32-bit core (implementing the Power Architecture technology) with thirty-two 32-bit general-purpose registers (GPRs)
 - The core performs branch prediction with conditional prefetch without conditional execution.
 - 4- or 8-Kbyte data cache and 4- or 16-Kbyte instruction cache (see Table 1)
 - 16-Kbyte instruction caches are four-way, set-associative with 256 sets; 4-Kbyte instruction caches are two-way, set-associative with 128 sets.
 - 8-Kbyte data caches are two-way, set-associative with 256 sets; 4-Kbyte data caches are two-way, set-associative with 128 sets.
 - Cache coherency for both instruction and data caches is maintained on 128-bit (4-word) cache blocks.
 - Caches are physically addressed, implement a least recently used (LRU) replacement algorithm, and are lockable on a cache block basis.
 - MMUs with 32-entry TLB, fully-associative instruction, and data TLBs
 - MMUs support multiple page sizes of 4-, 16-, and 512-Kbytes, and 8-Mbytes; 16 virtual address spaces and 16 protection groups
 - Advanced on-chip-emulation debug mode
- Up to 32-bit data bus (dynamic bus sizing for 8, 16, and 32 bits)
- 32 address lines
- Operates at up to 80 MHz
- Memory controller (eight banks)
 - Contains complete dynamic RAM (DRAM) controller
 - Each bank can be a chip select or \overline{RAS} to support a DRAM bank.
 - Up to 15 wait states programmable per memory bank
 - Glueless interface to DRAM, SIMMS, SRAM, EPROM, Flash EPROM, and other memory devices
 - DRAM controller programmable to support most size and speed memory interfaces
 - Four $\overline{\text{CAS}}$ lines, four $\overline{\text{WE}}$ lines, and one $\overline{\text{OE}}$ line
 - Boot chip-select available at reset (options for 8-, 16-, or 32-bit memory)
 - Variable block sizes (32 Kbytes to 256 Mbytes)
 - Selectable write protection
 - On-chip bus arbitration logic
- General-purpose timers
 - Four 16-bit timers or two 32-bit timers
 - Gate mode can enable/disable counting
 - Interrupt can be masked on reference match and event capture.



- Up to 8 Kbytes of dual-port RAM
- 16 serial DMA (SDMA) channels
- Three parallel I/O registers with open-drain capability
- Four baud-rate generators (BRGs)
 - Independent (can be tied to any SCC or SMC)
 - Allows changes during operation
 - Autobaud support option
- Four serial communications controllers (SCCs)
 - Ethernet/IEEE 802.3[®] standard optional on SCC1–4, supporting full 10-Mbps operation (available only on specially programmed devices)
 - HDLC/SDLC (all channels supported at 2 Mbps)
 - HDLC bus (implements an HDLC-based local area network (LAN))
 - Asynchronous HDLC to support point-to-point protocol (PPP)
 - AppleTalk
 - Universal asynchronous receiver transmitter (UART)
 - Synchronous UART
 - Serial infrared (IrDA)
 - Binary synchronous communication (BISYNC)
 - Totally transparent (bit streams)
 - Totally transparent (frame-based with optional cyclic redundancy check (CRC))
- Two SMCs (serial management channels)
 - UART
 - Transparent
 - General circuit interface (GCI) controller
 - Can be connected to the time-division multiplexed (TDM) channels
- One SPI (serial peripheral interface)
 - Supports master and slave modes
 - Supports multimaster operation on the same bus
- One I²C (inter-integrated circuit) port
 - Supports master and slave modes
 - Multiple-master environment support
- Time-slot assigner (TSA)
 - Allows SCCs and SMCs to run in multiplexed and/or non-multiplexed operation
 - Supports T1, CEPT, PCM highway, ISDN basic rate, ISDN primary rate, user defined
 - 1- or 8-bit resolution
 - Allows independent transmit and receive routing, frame synchronization, and clocking



Thermal Calculation and Measurement



Figure 2. Effect of Board Temperature Rise on Thermal Behavior

If the board temperature is known, an estimate of the junction temperature in the environment can be made using the following equation:

$$T_{J} = T_{B} + (R_{\theta JB} \times P_{D})$$

where:

 $R_{\theta JB}$ = junction-to-board thermal resistance (°C/W)

 $T_B = board temperature (°C)$

 P_D = power dissipation in package

If the board temperature is known and the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. For this method to work, the board and board mounting must be similar to the test board used to determine the junction-to-board thermal resistance, namely a 2s2p (board with a power and a ground plane) and by attaching the thermal balls to the ground plane.

7.4 Estimation Using Simulation

When the board temperature is not known, a thermal simulation of the application is needed. The simple two-resistor model can be used with the thermal simulation of the application [2], or a more accurate and complex model of the package can be used in the thermal simulation.

7.5 Experimental Determination

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$





Table 7 provides the bus operation timing for the MPC860 at 33, 40, 50, and 66 MHz.

The maximum bus speed supported by the MPC860 is 66 MHz. Higher-speed parts must be operated in half-speed bus mode (for example, an MPC860 used at 80 MHz must be configured for a 40-MHz bus).

The timing for the MPC860 bus shown assumes a 50-pF load for maximum delays and a 0-pF load for minimum delays.

Num B1 B1a B1b B1c B1c B1d B1e B1f B1g	Oh ann at an i a tio	33	MHz	40	MHz	50 I	MHz	66 I	Unit	
NUM	Characteristic	Min	Max	Min	Max	Min	Max	Min	Max	Unit
B1	CLKOUT period	30.30	30.30	25.00	30.30	20.00	30.30	15.15	30.30	ns
B1a	EXTCLK to CLKOUT phase skew (EXTCLK > 15 MHz and MF <= 2)	-0.90	0.90	-0.90	0.90	-0.90	0.90	-0.90	0.90	ns
B1b	EXTCLK to CLKOUT phase skew (EXTCLK > 10 MHz and MF < 10)	-2.30	2.30	-2.30	2.30	-2.30	2.30	-2.30	2.30	ns
B1c	CLKOUT phase jitter (EXTCLK > 15 MHz and MF <= 2) ¹	-0.60	0.60	-0.60	0.60	-0.60	0.60	-0.60	0.60	ns
B1d	CLKOUT phase jitter ¹	-2.00	2.00	-2.00	2.00	-2.00	2.00	-2.00	2.00	ns
B1e	CLKOUT frequency jitter (MF < 10) ¹	_	0.50	_	0.50	_	0.50	_	0.50	%
B1f	CLKOUT frequency jitter (10 < MF < 500) ¹	_	2.00	_	2.00	_	2.00	_	2.00	%
B1g	CLKOUT frequency jitter (MF > 500) ¹	_	3.00	—	3.00	—	3.00	_	3.00	%
B1h	Frequency jitter on EXTCLK ²	_	0.50	_	0.50	_	0.50	_	0.50	%
B2	CLKOUT pulse width low	12.12	—	10.00	_	8.00	—	6.06	_	ns
B3	CLKOUT width high	12.12	—	10.00	_	8.00	—	6.06	_	ns
B4	CLKOUT rise time ³	_	4.00	—	4.00	—	4.00	—	4.00	ns
B5 ³³	CLKOUT fall time ³	_	4.00	—	4.00	—	4.00	—	4.00	ns
B7	CLKOUT to A(0:31), BADDR(28:30), RD/WR, BURST, D(0:31), DP(0:3) invalid	7.58	—	6.25	—	5.00	—	3.80	—	ns
B7a	CLKOUT to TSIZ(0:1), REG, RSV, AT(0:3), BDIP, PTR invalid	7.58	—	6.25	—	5.00	—	3.80	—	ns
B7b	CLKOUT to BR, BG, FRZ, VFLS(0:1), VF(0:2) IWP(0:2), LWP(0:1), STS invalid ⁴	7.58	—	6.25	—	5.00	—	3.80	—	ns
B8	CLKOUT to A(0:31), BADDR(28:30) RD/WR, BURST, D(0:31), DP(0:3) valid	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.04	ns
B8a	CLKOUT to TSIZ(0:1), REG, RSV, AT(0:3) BDIP, PTR valid	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.04	ns
B8b	CLKOUT to BR, BG, VFLS(0:1), VF(0:2), IWP(0:2), FRZ, LWP(0:1), STS valid ⁴	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.04	ns

Table 7. Bus Operation Timings



		33	MHz	40 1	MHz	50 I	MHz	66 I		
Num	Characteristic	Min	Мах	Min	Мах	Min	Мах	Min	Max	Unit
B29d	$\overline{WE}(0:3)$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 0	43.45		35.5	_	28.00		20.73	_	ns
B29e	$\overline{\text{CS}}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 0	43.45		35.5		28.00		29.73	_	ns
B29f	\overline{WE} (0:3) negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 1	8.86		6.88	_	5.00	_	3.18		ns
B29g	$\overline{\text{CS}}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 1	8.86	_	6.88	—	5.00	—	3.18	_	ns
B29h	$\overline{WE}(0:3)$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 1	38.67	_	31.38	—	24.50	—	17.83	_	ns
B29i	$\overline{\text{CS}}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 1	38.67		31.38		24.50		17.83	_	ns
B30	\overline{CS} , \overline{WE} (0:3) negated to A(0:31), BADDR(28:30) invalid GPCM write access ⁸	5.58	—	4.25	—	3.00	—	1.79		ns
B30a	$\overline{\text{WE}}(0:3)$ negated to A(0:31), BADDR(28:30) invalid GPCM, write access, TRLX = 0, CSNT = 1, $\overline{\text{CS}}$ negated to A(0:31) invalid GPCM write access, TRLX = 0, CSNT = 1 ACS = 10, or ACS = 11, EBDF = 0	13.15	_	10.50	_	8.00	_	5.58		ns
B30b	$\label{eq:weighted} \hline WE(0:3) \ negated to \ A(0:31), \ invalid \ GPCM \\ BADDR(28:30) \ invalid \ GPCM \ write \ access, \\ TRLX = 1, \ CSNT = 1. \ \overline{CS} \ negated to \\ A(0:31), \ Invalid \ GPCM, \ write \ access, \\ TRLX = 1, \ CSNT = 1, \ ACS = 10, \ or \\ ACS = 11, \ EBDF = 0 \\ \hline \hline \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \$	43.45	_	35.50	_	28.00	_	20.73	_	ns
B30c	$\label{eq:weighted} \begin{array}{ c c c c } \hline \hline WE(0:3) \mbox{ negated to } A(0:31), \mbox{ BADDR}(28:30) \\ \hline \mbox{ invalid GPCM write access, TRLX = 0, } \\ \hline CSNT = 1. \end{cmathcelline CS} \mbox{ negated to } A(0:31) \mbox{ invalid GPCM write access, TRLX = 0, } \\ \hline GPCM \mbox{ write access, TRLX = 0, } \\ \hline ACS = 10, \mbox{ ACS = 11, EBDF = 1} \end{array}$	8.36	_	6.38	_	4.50	_	2.68	_	ns
B30d	$\overline{WE}(0:3)$ negated to A(0:31), BADDR(28:30) invalid GPCM write access, TRLX = 1, CSNT =1. \overline{CS} negated to A(0:31) invalid GPCM write access TRLX = 1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 1	38.67	_	31.38	_	24.50	_	17.83		ns
B31	CLKOUT falling edge to CS valid—as requested by control bit CST4 in the corresponding word in UPM	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns

Table 7. Bus Operation Timings (continued)



Figure 3 is the control timing diagram.



Figure 4 provides the timing for the external clock.



Figure 4. External Clock Timing



Figure 5 provides the timing for the synchronous output signals.



Figure 5. Synchronous Output Signals Timing

Figure 6 provides the timing for the synchronous active pull-up and open-drain output signals.



Figure 6. Synchronous Active Pull-Up Resistor and Open-Drain Outputs Signals Timing



Figure 9 provides the timing for the input data controlled by the UPM for data beats where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)



Figure 9. Input Data Timing when Controlled by UPM in the Memory Controller and DLT3 = 1

Figure 10 through Figure 13 provide the timing for the external bus read controlled by various GPCM factors.











Figure 12. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 11)





Figure 13. External Bus Read Timing (GPCM Controlled—TRLX = 0 or 1, ACS = 10, ACS = 11)





Figure 15. External Bus Write Timing (GPCM Controlled—TRLX = 0 or 1, CSNT = 1)







Figure 16. External Bus Write Timing (GPCM Controlled—TRLX = 0 or 1, CSNT = 1)







Figure 17. External Bus Timing (UPM Controlled Signals)





Figure 25 provides the PCMCIA access cycle timing for the external bus read.

Figure 25. PCMCIA Access Cycle Timing External Bus Read







Figure 26. PCMCIA Access Cycle Timing External Bus Write

Figure 27 provides the PCMCIA \overline{WAIT} signal detection timing.



Figure 27. PCMCIA WAIT Signal Detection Timing





Figure 34 provides the reset timing for the debug port configuration.

Figure 34. Reset Timing—Debug Port Configuration

10 IEEE 1149.1 Electrical Specifications

Table 13 provides the JTAG timings for the MPC860 shown in Figure 35 through Figure 38.

Num	Charactariatia	All Freq	uencies	Unit
Nulli	Characteristic	Min	Мах	Onit
J82	TCK cycle time	100.00	_	ns
J83	TCK clock pulse width measured at 1.5 V	40.00	_	ns
J84	TCK rise and fall times	0.00	10.00	ns
J85	TMS, TDI data setup time	5.00	—	ns
J86	TMS, TDI data hold time	25.00	_	ns
J87	TCK low to TDO data valid	—	27.00	ns
J88	TCK low to TDO data invalid	0.00	—	ns
J89	TCK low to TDO high impedance	—	20.00	ns
J90	TRST assert time	100.00	_	ns
J91	TRST setup time to TCK low	40.00	—	ns
J92	TCK falling edge to output valid	—	50.00	ns
J93	TCK falling edge to output valid out of high impedance	—	50.00	ns
J94	TCK falling edge to output high impedance	—	50.00	ns
J95	Boundary scan input valid to TCK rising edge	50.00	—	ns
J96	TCK rising edge to boundary scan input invalid	50.00		ns

Table 13. JTAG Timing



CPM Electrical Characteristics

11.4 Baud Rate Generator AC Electrical Specifications

Table 17 provides the baud rate generator timings as shown in Figure 49.

Table 17. Baud Rate Generator Timing

Num	Charactariatia	All Freq	Unit	
Nulli	Characteristic	Min	Мах	Unit
50	BRGO rise and fall time	—	10	ns
51	BRGO duty cycle	40	60	%
52	BRGO cycle	40	—	ns



Figure 49. Baud Rate Generator Timing Diagram

11.5 Timer AC Electrical Specifications

Table 18 provides the general-purpose timer timings as shown in Figure 50.

Table 18. Timer Timing

Num Characteristic 61 TIN/TGATE rise and fall time 62 TIN/TGATE low time	All Freq	Unit		
Num	Characteristic	Min	Мах	Unit
61	TIN/TGATE rise and fall time	10	—	ns
62	TIN/TGATE low time	1	—	CLK
63	TIN/TGATE high time	2	—	CLK
64	TIN/TGATE cycle time	3	—	CLK
65	CLKO low to TOUT valid	3	25	ns



SCC in NMSI Mode Electrical Specifications 11.7

Table 20 provides the NMSI external clock timing.

Num 100 101 102 103	Characteristic	All Freq	Unit	
Nulli	Characteristic	Min	Мах	Unit
100	RCLK1 and TCLK1 width high ¹	1/SYNCCLK	_	ns
101	RCLK1 and TCLK1 width low	1/SYNCCLK + 5		ns
102	RCLK1 and TCLK1 rise/fall time	—	15.00	ns
103	TXD1 active delay (from TCLK1 falling edge)	0.00	50.00	ns
104	RTS1 active/inactive delay (from TCLK1 falling edge)	0.00	50.00	ns
105	CTS1 setup time to TCLK1 rising edge	5.00	—	ns
106	RXD1 setup time to RCLK1 rising edge	5.00	_	ns
107	RXD1 hold time from RCLK1 rising edge ²	5.00	—	ns
108	CD1 setup Time to RCLK1 rising edge	5.00	_	ns

¹ The ratios SYNCCLK/RCLK1 and SYNCCLK/TCLK1 must be greater than or equal to 2.25/1.
 ² Also applies to CD and CTS hold time when they are used as external sync signals.

Table 21 provides the NMSI internal clock timing.

Table 21. NMSI Internal Clock Timing

Num	Jm Characteristic 00 RCLK1 and TCLK1 frequency ¹ 02 RCLK1 and TCLK1 rise/fall time 03 TXD1 active delay (from TCLK1 falling edge) 04 RTS1 active/inactive delay (from TCLK1 falling edge) 05 CTS1 setup time to TCLK1 rising edge 06 RXD1 setup time to RCLK1 rising edge ²	All Freq	Unit	
Num	Characteristic	Min	Мах	Unit
100	RCLK1 and TCLK1 frequency ¹	0.00	SYNCCLK/3	MHz
102	RCLK1 and TCLK1 rise/fall time	—	—	ns
103	TXD1 active delay (from TCLK1 falling edge)	0.00	30.00	ns
104	RTS1 active/inactive delay (from TCLK1 falling edge)	0.00	30.00	ns
105	CTS1 setup time to TCLK1 rising edge	40.00	—	ns
106	RXD1 setup time to RCLK1 rising edge	40.00	—	ns
107	RXD1 hold time from RCLK1 rising edge ²	0.00	—	ns
108	CD1 setup time to RCLK1 rising edge	40.00	_	ns

¹ The ratios SYNCCLK/RCLK1 and SYNCCLK/TCLK1 must be greater than or equal to 3/1.

² Also applies to \overline{CD} and \overline{CTS} hold time when they are used as external sync signals.



14.2 Pin Assignments

Figure 76 shows the top view pinout of the PBGA package. For additional information, see the MPC860 PowerQUICC User's Manual, or the MPC855T User's Manual.

	\sim	~	\sim	~	\sim	~	~	~	~	~	~	~	~	~	~	\sim	\sim		
	O PD10	O PD8	O PD3		O D0	O D4	() D1) D2	О D3	O D5		O D6	0 D7	0 D29	DP2		с IPA3		W
O PD14	O PD13	O PD9	O PD6	O M_Tx_I		O D13	() D27	〇 D10) D14	〇 D18	〇 D20	〇 D24	0 D28	O DP1	O DP3	O DP0	⊖ N/C		V 1
0 PA0	O PB14	O PD15	O PD4	O PD5		() D8	() D23) D11) D16) D19	0 D21	〇 D26) D30	O IPA5	O IPA4	O IPA2	O N/C	O VSSSYN	U N
O PA1	O PC5	O PC4	O PD11) 1 D12	() D17) D9) D15	0 D22) D25	〇 D31	O IPA6) IPA1	O IPA7	⊖ xfc		T N
O PC6	0 PA2	O PB15	O PD12	\bigcirc		0	0	\bigcirc	\bigcirc	0	0	0	0						R WR
0 PA4	O PB17	O PA3		\bigcirc	$\bigcap_{i=1}^{n}$		\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	GND					ET XTAL	Ρ
O PB19	O PA5	O PB18	O PB16	\bigcirc	0	\bigcirc	0					N							
O PA7	0 PC8	O PA6	O PC7	\bigcirc	\circ	\bigcirc	0) DR29 VDE	M							
O PB22	O PC9	O PA8	O PB20	\bigcirc	\circ	\bigcirc	0	О ОР0		O OP1		L 1							
O PC10	O PA9	O PB23	O PB21	\bigcirc	0	\bigcirc	\bigcirc	\bigcirc		\bigcirc	\bigcirc	\bigcirc	\bigcirc	0					к
O PC11	O PB24	O PA10	O PB25	\bigcirc	\circ	\bigcirc	0	O IPB5	O IPB1			J							
			О тск	\bigcirc	0	\bigcirc	0	О СО				н							
	_ ⊂ ™S		O PA11	\bigcirc	0	\bigcirc	0					G							
O PB26	O PC12	O PA12		\bigcirc			0	0	0	\bigcirc	0	\bigcirc							F
O PB27	O PC13	O PA13	O PB29	\bigcirc		0	0	0	0	0	0	0	0		$\frac{\bigcirc}{CS3}$	O BI			E
0	0	0	0	0	\bigcirc	\bigcirc	0	0	0	0	<u> </u>	0	0	<u> </u>	<u> </u>	0	0	<u> </u>	D
									A25						$\frac{0}{0}$				С
				A9															В
AU								A23							$\frac{1}{000}$			GPLB4	A
19	А2 18	н5 17	А7 16	ATT 15	A14 14	А27 13	A29 12	АЗО 11	A28 10	A31 9	8	в5А2 7	vv⊨1 6	vv⊨3 5	4	3 3	2	1	

NOTE: This is the top view of the device.

Figure 76. Pinout of the PBGA Package



Mechanical Data and Ordering Information

14.3 Mechanical Dimensions of the PBGA Package

Figure 77 shows the mechanical dimensions of the ZP PBGA package.



- 1. Dimensions and tolerance per ASME Y14.5M, 1994.
- 2. Dimensions in millimeters.
- 3. Dimension b is the maximum solder ball diameter measured parallel to data C.



22.40

E2

22.60