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#### Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

#### Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

#### Details

Obsolete
MPC8xx
1 Core, 32-Bit
50MHz
Communications; CPM
DRAM
No
-
10Mbps (2), 10/100Mbps (1)
-
-
3.3V
0°C ~ 95°C (TA)
-
357-BBGA
357-PBGA (25x25)
https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc860dpvr50d4r2

Email: info@E-XFL.COM

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Features

- System integration unit (SIU)
  - Bus monitor
  - Software watchdog
  - Periodic interrupt timer (PIT)
  - Low-power stop mode
  - Clock synthesizer
  - Decrementer, time base, and real-time clock (RTC)
  - Reset controller
  - IEEE 1149.1<sup>TM</sup> Std. test access port (JTAG)
- Interrupts
  - Seven external interrupt request (IRQ) lines
  - 12 port pins with interrupt capability
  - 23 internal interrupt sources
  - Programmable priority between SCCs
  - Programmable highest priority request
- 10/100 Mbps Ethernet support, fully compliant with the IEEE 802.3u® Standard (not available when using ATM over UTOPIA interface)
- ATM support compliant with ATM forum UNI 4.0 specification
  - Cell processing up to 50–70 Mbps at 50-MHz system clock
  - Cell multiplexing/demultiplexing
  - Support of AAL5 and AAL0 protocols on a per-VC basis. AAL0 support enables OAM and software implementation of other protocols.
  - ATM pace control (APC) scheduler, providing direct support for constant bit rate (CBR) and unspecified bit rate (UBR) and providing control mechanisms enabling software support of available bit rate (ABR)
  - Physical interface support for UTOPIA (10/100-Mbps is not supported with this interface) and byte-aligned serial (for example, T1/E1/ADSL)
  - UTOPIA-mode ATM supports level-1 master with cell-level handshake, multi-PHY (up to four physical layer devices), connection to 25-, 51-, or 155-Mbps framers, and UTOPIA/system clock ratios of 1/2 or 1/3.
  - Serial-mode ATM connection supports transmission convergence (TC) function for T1/E1/ADSL lines, cell delineation, cell payload scrambling/descrambling, automatic idle/unassigned cell insertion/stripping, header error control (HEC) generation, checking, and statistics.
- Communications processor module (CPM)
  - RISC communications processor (CP)
  - Communication-specific commands (for example, GRACEFUL STOP TRANSMIT, ENTER HUNT MODE, and RESTART TRANSMIT)
  - Supports continuous mode transmission and reception on all serial channels



## 3 Maximum Tolerated Ratings

This section provides the maximum tolerated voltage and temperature ranges for the MPC860. Table 2 provides the maximum ratings.

This device contains circuitry protecting against damage due to high-static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or  $V_{DD}$ ).

(GND = 0 V)

### Table 2. Maximum Tolerated Ratings

Rating	Symbol	Value	Unit
Supply voltage <sup>1</sup>	V <sub>DDH</sub>	-0.3 to 4.0	V
	V <sub>DDL</sub>	-0.3 to 4.0	V
	$\begin{tabular}{ c c c c c c c } \hline Symbol & Value & Unit \\ \hline V_{DDH} & -0.3 to 4.0 & V \\ \hline V_{DDL} & -0.3 to 4.0 & V \\ \hline V_{DDSYN} & -0.3 to 4.0 & V \\ \hline V_{DDSYN} & -0.3 to 4.0 & V \\ \hline V_{DDSYN} & -0.3 to V_{DDH} & V \\ \hline V_{in} & GND - 0.3 to V_{DDH} & V \\ \hline T_{A(min)} & 0 & ^{\circ}C \\ \hline T_{j(max)} & 95 & ^{\circ}C \\ \hline T_{max} & -55 to 150 & ^{\circ}C \\ \hline \end{tabular}$		
	V <sub>DDSYN</sub>	-0.3 to 4.0	V
Input voltage <sup>2</sup>	V <sub>in</sub>	GND – 0.3 to V <sub>DDH</sub>	V
Temperature <sup>3</sup> (standard)	T <sub>A(min)</sub>	0	°C
	T <sub>j(max)</sub>	95	°C
Temperature <sup>3</sup> (extended)	T <sub>A(min)</sub>	-40	°C
	T <sub>j(max)</sub>	95	°C
Storage temperature range	T <sub>stg</sub>	-55 to 150	°C

<sup>1</sup> The power supply of the device must start its ramp from 0.0 V.

<sup>2</sup> Functional operating conditions are provided with the DC electrical specifications in Table 6. Absolute maximum ratings are stress ratings only; functional operation at the maxima is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device.

**Caution**: All inputs that tolerate 5 V cannot be more than 2.5 V greater than the supply voltage. This restriction applies to power-up and normal operation (that is, if the MPC860 is unpowered, voltage greater than 2.5 V must not be applied to its inputs).

<sup>3</sup> Minimum temperatures are guaranteed as ambient temperature, T<sub>A</sub>. Maximum temperatures are guaranteed as junction temperature, T<sub>j</sub>.



### Table 4 shows the thermal characteristics for the MPC860.

### Table 4. MPC860 Thermal Resistance Data

Rating	Env	ironment	Symbol	ZP MPC860P	ZQ / VR MPC860P	Unit
Mold Compound Thicknes		0.85	1.15	mm		
Junction-to-ambient <sup>1</sup>	Natural convection	Single-layer board (1s)	$R_{\theta JA}^2$	34	34	°C/W
		Four-layer board (2s2p)	$R_{\theta JMA}^{3}$	22	22	
	Airflow (200 ft/min)	Single-layer board (1s)	$R_{\theta JMA}^{3}$	27	27	
		Four-layer board (2s2p)	$R_{\theta JMA}^{3}$	18	18	
Junction-to-board <sup>4</sup>			$R_{\theta JB}$	14	13	
Junction-to-case <sup>5</sup>			$R_{\thetaJC}$	6	8	
Junction-to-package top <sup>6</sup>	Natural convection		$\Psi_{JT}$	2	2	

<sup>1</sup> Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.

<sup>2</sup> Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.

<sup>3</sup> Per JEDEC JESD51-6 with the board horizontal.

<sup>4</sup> Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

- <sup>5</sup> Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature. For exposed pad packages where the pad would be expected to be soldered, junction-to-case thermal resistance is a simulated value from the junction to the exposed pad without contact resistance.
- <sup>6</sup> Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2.



Layout Practices

where:

 $\Psi_{JT}$  = thermal characterization parameter

 $T_T$  = thermocouple temperature on top of package

 $P_D$  = power dissipation in package

The thermal characterization parameter is measured per JEDEC JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

## 7.6 References

Semiconductor Equipment and Materials International	(415) 964-5111
805 East Middlefield Rd.	
Mountain View, CA 94043	
MIL-SPEC and EIA/JESD (JEDEC) Specifications	800-854-7179 or
(Available from Global Engineering Documents)	303-397-7956
JEDEC Specifications	http://www.jedec.org

- 1. C.E. Triplett and B. Joiner, "An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module," Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.
- B. Joiner and V. Adams, "Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling," Proceedings of SemiTherm, San Diego, 1999, pp. 212–220.

# 8 Layout Practices

Each  $V_{DD}$  pin on the MPC860 should be provided with a low-impedance path to the board's supply. Each GND pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on the chip. The  $V_{DD}$  power supply should be bypassed to ground using at least four 0.1 µF-bypass capacitors located as close as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to chip  $V_{DD}$  and GND should be kept to less than half an inch per capacitor lead. A four-layer board employing two inner layers as  $V_{CC}$  and GND planes is recommended.

All output pins on the MPC860 have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized in order to minimize undershoot and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data buses. Maximum PC trace lengths of 6 inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the  $V_{CC}$  and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.





Table 7 provides the bus operation timing for the MPC860 at 33, 40, 50, and 66 MHz.

The maximum bus speed supported by the MPC860 is 66 MHz. Higher-speed parts must be operated in half-speed bus mode (for example, an MPC860 used at 80 MHz must be configured for a 40-MHz bus).

The timing for the MPC860 bus shown assumes a 50-pF load for maximum delays and a 0-pF load for minimum delays.

NI	Chavastavistis	33 MHz		40 MHz		50 MHz		66 MHz		
NUM	Characteristic	Min	Max	Min	Max	Min	Max	Min	Max	Unit
B1	CLKOUT period	30.30	30.30	25.00	30.30	20.00	30.30	15.15	30.30	ns
B1a	EXTCLK to CLKOUT phase skew (EXTCLK > 15 MHz and MF <= 2)	-0.90	0.90	-0.90	0.90	-0.90	0.90	-0.90	0.90	ns
B1b	EXTCLK to CLKOUT phase skew (EXTCLK > 10 MHz and MF < 10)	-2.30	2.30	-2.30	2.30	-2.30	2.30	-2.30	2.30	ns
B1c	CLKOUT phase jitter (EXTCLK > 15 MHz and MF <= 2) <sup>1</sup>	-0.60	0.60	-0.60	0.60	-0.60	0.60	-0.60	0.60	ns
B1d	CLKOUT phase jitter <sup>1</sup>	-2.00	2.00	-2.00	2.00	-2.00	2.00	-2.00	2.00	ns
B1e	CLKOUT frequency jitter (MF < 10) <sup>1</sup>	_	0.50	_	0.50	_	0.50	_	0.50	%
B1f	CLKOUT frequency jitter (10 < MF < 500) <sup>1</sup>	_	2.00	_	2.00	_	2.00	_	2.00	%
B1g	CLKOUT frequency jitter (MF > 500) <sup>1</sup>	_	3.00	—	3.00	_	3.00	_	3.00	%
B1h	Frequency jitter on EXTCLK <sup>2</sup>	_	0.50	_	0.50	_	0.50	_	0.50	%
B2	CLKOUT pulse width low	12.12	—	10.00	_	8.00	—	6.06	_	ns
B3	CLKOUT width high	12.12	—	10.00	_	8.00	—	6.06	_	ns
B4	CLKOUT rise time <sup>3</sup>	_	4.00	—	4.00	—	4.00	—	4.00	ns
B5 <sup>33</sup>	CLKOUT fall time <sup>3</sup>	_	4.00	—	4.00	—	4.00	—	4.00	ns
B7	CLKOUT to A(0:31), BADDR(28:30), RD/WR, BURST, D(0:31), DP(0:3) invalid	7.58	—	6.25	—	5.00	—	3.80	—	ns
B7a	CLKOUT to TSIZ(0:1), REG, RSV, AT(0:3), BDIP, PTR invalid	7.58	—	6.25	—	5.00	—	3.80	—	ns
B7b	CLKOUT to BR, BG, FRZ, VFLS(0:1), VF(0:2) IWP(0:2), LWP(0:1), STS invalid <sup>4</sup>	7.58	—	6.25	—	5.00	—	3.80	—	ns
B8	CLKOUT to A(0:31), BADDR(28:30) RD/WR, BURST, D(0:31), DP(0:3) valid	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.04	ns
B8a	CLKOUT to TSIZ(0:1), REG, RSV, AT(0:3) BDIP, PTR valid	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.04	ns
B8b	CLKOUT to BR, BG, VFLS(0:1), VF(0:2), IWP(0:2), FRZ, LWP(0:1), STS valid <sup>4</sup>	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.04	ns

Table 7. Bus Operation Timings



		33	33 MHz		40 MHz		50 MHz		66 MHz	
Num	Characteristic	Min	Max	Min	Max	Min	Max	Min	Max	Unit
B9	CLKOUT to A(0:31), BADDR(28:30), RD/WR, BURST, D(0:31), DP(0:3), TSIZ(0:1), REG, RSV, AT(0:3), PTR High-Z	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.04	ns
B11	CLKOUT to $\overline{TS}$ , $\overline{BB}$ assertion	7.58	13.58	6.25	12.25	5.00	11.00	3.80	11.29	ns
B11a	CLKOUT to $\overline{TA}$ , $\overline{BI}$ assertion (when driven by the memory controller or PCMCIA interface)	2.50	9.25	2.50	9.25	2.50	9.25	2.50	9.75	ns
B12	CLKOUT to $\overline{TS}$ , $\overline{BB}$ negation	7.58	14.33	6.25	13.00	5.00	11.75	3.80	8.54	ns
B12a	CLKOUT to $\overline{TA}$ , $\overline{BI}$ negation (when driven by the memory controller or PCMCIA interface)	2.50	11.00	2.50	11.00	2.50	11.00	2.50	9.00	ns
B13	CLKOUT to TS, BB High-Z	7.58	21.58	6.25	20.25	5.00	19.00	3.80	14.04	ns
B13a	CLKOUT to $\overline{TA}$ , $\overline{BI}$ High-Z (when driven by the memory controller or PCMCIA interface)	2.50	15.00	2.50	15.00	2.50	15.00	2.50	15.00	ns
B14	CLKOUT to TEA assertion	2.50	10.00	2.50	10.00	2.50	10.00	2.50	9.00	ns
B15	CLKOUT to TEA High-Z	2.50	15.00	2.50	15.00	2.50	15.00	2.50	15.00	ns
B16	TA, BI valid to CLKOUT (setup time)	9.75		9.75		9.75	_	6.00	_	ns
B16a	TEA, KR, RETRY, CR valid to CLKOUT (setup time)	10.00	_	10.00	—	10.00	—	4.50	—	ns
B16b	$\overline{\text{BB}}, \overline{\text{BG}}, \overline{\text{BR}}, \text{ valid to CLKOUT (setup time)}^5$	8.50		8.50		8.50	_	4.00	_	ns
B17	CLKOUT to $\overline{TA}$ , $\overline{TEA}$ , $\overline{BI}$ , $\overline{BB}$ , $\overline{BG}$ , $\overline{BR}$ valid (hold time)	1.00	—	1.00	—	1.00	—	2.00	—	ns
B17a	CLKOUT to KR, RETRY, CR valid (hold time)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B18	D(0:31), DP(0:3) valid to CLKOUT rising edge (setup time) <sup>6</sup>	6.00	—	6.00	—	6.00	—	6.00	—	ns
B19	CLKOUT rising edge to D(0:31), DP(0:3) valid (hold time) <sup>6</sup>	1.00	—	1.00	—	1.00	—	2.00	—	ns
B20	D(0:31), DP(0:3) valid to CLKOUT falling edge (setup time) <sup>7</sup>	4.00	—	4.00	—	4.00	—	4.00	—	ns
B21	CLKOUT falling edge to D(0:31), DP(0:3) valid (hold time) <sup>7</sup>	2.00	—	2.00	—	2.00	—	2.00	—	ns
B22	CLKOUT rising edge to $\overline{CS}$ asserted GPCM ACS = 00	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.04	ns
B22a	CLKOUT falling edge to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 0		8.00		8.00		8.00		8.00	ns
B22b	CLKOUT falling edge to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 0, EBDF = 0	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.54	ns
B22c	CLKOUT falling edge to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 0, EBDF = 1	10.86	17.99	8.88	16.00	7.00	14.13	5.18	12.31	ns

## Table 7. Bus Operation Timings (continued)



		33	MHz	40 1	MHz	50 I	MHz	66 MHz		
Num	Characteristic	Min	Мах	Min	Мах	Min	Мах	Min	Max	Unit
B29d	$\overline{WE}$ (0:3) negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 0	43.45		35.5	_	28.00		20.73	_	ns
B29e	$\overline{\text{CS}}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 0	43.45		35.5		28.00		29.73	_	ns
B29f	$\overline{WE}$ (0:3) negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 1	8.86	_	6.88	_	5.00	_	3.18		ns
B29g	$\overline{\text{CS}}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 1	8.86	_	6.88	—	5.00	—	3.18	_	ns
B29h	$\overline{WE}(0:3)$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 1	38.67	—	31.38	—	24.50	—	17.83	_	ns
B29i	$\overline{\text{CS}}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 1	38.67		31.38		24.50		17.83	_	ns
B30	$\overline{CS}$ , $\overline{WE}$ (0:3) negated to A(0:31), BADDR(28:30) invalid GPCM write access <sup>8</sup>	5.58	—	4.25	—	3.00	—	1.79		ns
B30a	$\overline{\text{WE}}(0:3)$ negated to A(0:31), BADDR(28:30) invalid GPCM, write access, TRLX = 0, CSNT = 1, $\overline{\text{CS}}$ negated to A(0:31) invalid GPCM write access, TRLX = 0, CSNT = 1 ACS = 10, or ACS = 11, EBDF = 0	13.15	_	10.50	_	8.00	_	5.58		ns
B30b	$\label{eq:weighted} \hline WE(0:3) \ negated to \ A(0:31), \ invalid \ GPCM \\ BADDR(28:30) \ invalid \ GPCM \ write \ access, \\ TRLX = 1, \ CSNT = 1. \ \overline{CS} \ negated to \\ A(0:31), \ Invalid \ GPCM, \ write \ access, \\ TRLX = 1, \ CSNT = 1, \ ACS = 10, \ or \\ ACS = 11, \ EBDF = 0 \\ \hline \hline \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \$	43.45	_	35.50	_	28.00	_	20.73	_	ns
B30c	$\label{eq:weighted} \begin{array}{ c c c c } \hline WE(0:3) \mbox{ negated to } A(0:31), \mbox{ BADDR}(28:30) \\ \hline \mbox{ invalid GPCM write access, TRLX = 0, } \\ \hline CSNT = 1. \end{cmathcelline CS} \mbox{ negated to } A(0:31) \mbox{ invalid GPCM write access, TRLX = 0, } \\ \hline GPCM \mbox{ write access, TRLX = 0, } \\ \hline ACS = 10, \mbox{ ACS = 11, EBDF = 1} \end{array}$	8.36	_	6.38	_	4.50		2.68		ns
B30d	$\overline{WE}(0:3)$ negated to A(0:31), BADDR(28:30) invalid GPCM write access, TRLX = 1, CSNT =1. $\overline{CS}$ negated to A(0:31) invalid GPCM write access TRLX = 1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 1	38.67	_	31.38	_	24.50	_	17.83		ns
B31	CLKOUT falling edge to CS valid—as requested by control bit CST4 in the corresponding word in UPM	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns

## Table 7. Bus Operation Timings (continued)



	Characteristic	33	33 MHz		40 MHz		50 MHz		66 MHz	
Num	Characteristic	Min	Max	Min	Max	Min	Max	Min	Max	Unit
B31a	CLKOUT falling edge to CS valid—as requested by control bit CST1 in the corresponding word in UPM	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.54	ns
B31b	CLKOUT rising edge to $\overline{CS}$ valid—as requested by control bit CST2 in the corresponding word in UPM	1.50	8.00	1.50	8.00	1.50	8.00	1.50	8.00	ns
B31c	CLKOUT rising edge to $\overline{\text{CS}}$ valid—as requested by control bit CST3 in the corresponding word in UPM	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.04	ns
B31d	CLKOUT falling edge to $\overline{CS}$ valid—as requested by control bit CST1 in the corresponding word in UPM, EBDF = 1	13.26	17.99	11.28	16.00	9.40	14.13	7.58	12.31	ns
B32	CLKOUT falling edge to BS valid—as requested by control bit BST4 in the corresponding word in UPM	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns
B32a	CLKOUT falling edge to $\overline{BS}$ valid—as requested by control bit BST1 in the corresponding word in UPM, EBDF = 0	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.54	ns
B32b	CLKOUT rising edge to $\overline{\text{BS}}$ valid—as requested by control bit BST2 in the corresponding word in UPM	1.50	8.00	1.50	8.00	1.50	8.00	1.50	8.00	ns
B32c	CLKOUT rising edge to $\overline{\text{BS}}$ valid—as requested by control bit BST3 in the corresponding word in UPM	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.54	ns
B32d	CLKOUT falling edge to $\overline{BS}$ valid—as requested by control bit BST1 in the corresponding word in UPM, EBDF = 1	13.26	17.99	11.28	16.00	9.40	14.13	7.58	12.31	ns
B33	CLKOUT falling edge to GPL valid—as requested by control bit GxT4 in the corresponding word in UPM	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns
B33a	CLKOUT rising edge to GPL valid—as requested by control bit GxT3 in the corresponding word in UPM	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.54	ns
B34	A(0:31), BADDR(28:30), and D(0:31) to $\overline{CS}$ valid—as requested by control bit CST4 in the corresponding word in UPM	5.58	—	4.25	—	3.00	—	1.79	—	ns
B34a	A(0:31), BADDR(28:30), and D(0:31) to $\overline{CS}$ valid—as requested by control bit CST1 in the corresponding word in UPM	13.15		10.50		8.00		5.58	_	ns
B34b	A(0:31), BADDR(28:30), and D(0:31) to $\overline{CS}$ valid—as requested by control bit CST2 in the corresponding word in UPM	20.73	_	16.75		13.00		9.36	_	ns

## Table 7. Bus Operation Timings (continued)



Figure 3 is the control timing diagram.



Figure 4 provides the timing for the external clock.



Figure 4. External Clock Timing



Figure 9 provides the timing for the input data controlled by the UPM for data beats where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)



Figure 9. Input Data Timing when Controlled by UPM in the Memory Controller and DLT3 = 1

Figure 10 through Figure 13 provide the timing for the external bus read controlled by various GPCM factors.











Figure 12. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 11)



Figure 18 provides the timing for the asynchronous asserted UPWAIT signal controlled by the UPM.



Figure 18. Asynchronous UPWAIT Asserted Detection in UPM Handled Cycles Timing

Figure 19 provides the timing for the asynchronous negated UPWAIT signal controlled by the UPM.



Figure 19. Asynchronous UPWAIT Negated Detection in UPM Handled Cycles Timing





Figure 20 provides the timing for the synchronous external master access controlled by the GPCM.

Figure 20. Synchronous External Master Access Timing (GPCM Handled ACS = 00)

Figure 21 provides the timing for the asynchronous external master memory access controlled by the GPCM.





Figure 22 provides the timing for the asynchronous external master control signals negation.



Figure 22. Asynchronous External Master—Control Signals Negation Timing





Figure 25 provides the PCMCIA access cycle timing for the external bus read.

Figure 25. PCMCIA Access Cycle Timing External Bus Read







## Figure 26. PCMCIA Access Cycle Timing External Bus Write

Figure 27 provides the PCMCIA  $\overline{WAIT}$  signal detection timing.



Figure 27. PCMCIA WAIT Signal Detection Timing



Table 11 shows the debug port timing for the MPC860.

Table 11. Debug Port Timing

Num	Characteristic	All Freq	Unit	
Num	Characteristic	Min	Мах	Unit
P61	DSCK cycle time	3 × T <sub>CLOCKOUT</sub>	_	_
P62	DSCK clock pulse width	$1.25 \times T_{CLOCKOUT}$	—	—
P63	DSCK rise and fall times	0.00 3.00		ns
P64	DSDI input data setup time	8.00	—	ns
P65	DSDI data hold time	5.00	—	ns
P66	DSCK low to DSDO data valid	0.00	15.00	ns
P67	DSCK low to DSDO invalid	0.00	2.00	ns

Figure 30 provides the input timing for the debug port clock.



Figure 30. Debug Port Clock Input Timing

Figure 31 provides the timing for the debug port.



Figure 31. Debug Port Timings

**CPM Electrical Characteristics** 



## **11 CPM Electrical Characteristics**

This section provides the AC and DC electrical specifications for the communications processor module (CPM) of the MPC860.

## 11.1 PIP/PIO AC Electrical Specifications

Table 14 provides the PIP/PIO AC timings as shown in Figure 39 through Figure 43.

## Table 14. PIP/PIO Timing

Num	Characteristic	All Freq	uencies	Unit
Num	Onardetensite	Min	Max	Onit
21	Data-in setup time to STBI low	0	_	ns
22	Data-in hold time to STBI high	2.5 – t3 <sup>1</sup>	_	CLK
23	STBI pulse width	1.5	_	CLK
24	STBO pulse width	1 CLK – 5 ns	_	ns
25	Data-out setup time to STBO low	2	_	CLK
26	Data-out hold time from STBO high	5	_	CLK
27	STBI low to STBO low (Rx interlock)	_	2	CLK
28	STBI low to STBO high (Tx interlock)	2	_	CLK
29	Data-in setup time to clock high	15	_	ns
30	Data-in hold time from clock high	7.5	_	ns
31	Clock low to data-out valid (CPU writes data, control, or direction)		25	ns

<sup>1</sup> t3 = Specification 23.



Figure 39. PIP Rx (Interlock Mode) Timing Diagram



**CPM Electrical Characteristics** 

Num	Chavastavistia	All Freq	Unit	
Num	Characteristic	Min	Мах	Unit
135	RSTRT active delay (from TCLK1 falling edge)	10	50	ns
136	RSTRT inactive delay (from TCLK1 falling edge)	10	50	ns
137	REJECT width low	1	—	CLK
138	CLKO1 low to SDACK asserted <sup>2</sup>		20	ns
139	CLKO1 low to SDACK negated <sup>2</sup>	_	20	ns

### Table 22. Ethernet Timing (continued)

<sup>1</sup> The ratios SYNCCLK/RCLK1 and SYNCCLK/TCLK1 must be greater than or equal to 2/1.

<sup>2</sup> SDACK is asserted whenever the SDMA writes the incoming frame DA into memory.



Figure 59. Ethernet Collision Timing Diagram



Figure 60. Ethernet Receive Timing Diagram



**CPM Electrical Characteristics** 

## 11.12 I<sup>2</sup>C AC Electrical Specifications

Table 26 provides the  $I^2C$  (SCL < 100 kHz) timings.

## Table 26. I<sup>2</sup>C Timing (SCL < 100 kHz)

Num	Characteristic	All Freq	uencies	Unit
Nulli		Min	Мах	Unit
200	SCL clock frequency (slave)	0	100	kHz
200	SCL clock frequency (master) <sup>1</sup>	1.5	100	kHz
202	Bus free time between transmissions	4.7	—	μS
203	Low period of SCL	4.7	—	μS
204	High period of SCL	4.0	—	μS
205	Start condition setup time	4.7	—	μS
206	Start condition hold time	4.0	—	μS
207	Data hold time	0	—	μS
208	Data setup time	250	—	ns
209	SDL/SCL rise time	—	1	μS
210	SDL/SCL fall time	—	300	ns
211	Stop condition setup time	4.7	—	μS

SCL frequency is given by SCL = BRGCLK\_frequency / ((BRG register + 3 × pre\_scaler × 2). The ratio SYNCCLK/(BRGCLK/pre\_scaler) must be greater than or equal to 4/1.

## Table 27 provides the $I^2C$ (SCL > 100 kHz) timings.

## Table 27. . I<sup>2</sup>C Timing (SCL > 100 kHz)

Num	Characteristic	Expression	All Freq	Unit	
Num			Min	Мах	Unit
200	SCL clock frequency (slave)	fSCL	0	BRGCLK/48	Hz
200	SCL clock frequency (master) <sup>1</sup>	fSCL	BRGCLK/16512	BRGCLK/48	Hz
202	Bus free time between transmissions		1/(2.2 * fSCL)	—	S
203	Low period of SCL		1/(2.2 * fSCL)	—	S
204	High period of SCL		1/(2.2 * fSCL)	—	S
205	Start condition setup time		1/(2.2 * fSCL)	—	S
206	Start condition hold time		1/(2.2 * fSCL)	—	S
207	Data hold time		0	—	S
208	Data setup time		1/(40 * fSCL)	—	S
209	SDL/SCL rise time		—	1/(10 * fSCL)	S
210	SDL/SCL fall time		—	1/(33 * fSCL)	S
211	Stop condition setup time		1/2(2.2 * fSCL)	—	s

SCL frequency is given by SCL = BRGCLK\_frequency / ((BRG register + 3) × pre\_scaler × 2). The ratio SYNCCLK/(BRGCLK / pre\_scaler) must be greater than or equal to 4/1.



Figure 69 shows the  $I^2C$  bus timing.



Figure 69. I<sup>2</sup>C Bus Timing Diagram

## **12 UTOPIA AC Electrical Specifications**

Table 28 shows the AC electrical specifications for the UTOPIA interface.

Num	Signal Characteristic	Direction	Min	Max	Unit
U1	UtpClk rise/fall time (Internal clock option)	Output	—	3.5	ns
	Duty cycle		50	50	%
	Frequency		—	50	MHz
U1a	UtpClk rise/fall time (external clock option)	Input	—	3.5	ns
	Duty cycle		40	60	%
	Frequency		—	50	MHz
U2	RxEnb and TxEnb active delay	Output	2	16	ns
U3	UTPB, SOC, Rxclav and Txclav setup time	Input	8	—	ns
U4	UTPB, SOC, Rxclav and Txclav hold time	Input	1	—	ns
U5	UTPB, SOC active delay (and PHREQ and PHSEL active delay in MPHY mode)	Output	2	16	ns

## Table 28. UTOPIA AC Electrical Specifications