NXP USA Inc. - MPC860DPVR66D4 Datasheet



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Details

Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	66MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (2), 10/100Mbps (1)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 95°C (TA)
Security Features	-
Package / Case	357-BBGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc860dpvr66d4

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Thermal Characteristics

Figure 1 shows the undershoot and overshoot voltages at the interface of the MPC860.



1. t_{interface} refers to the clock period associated with the bus clock interface.

Figure 1. Undershoot/Overshoot Voltage for V_{DDH} and V_{DDL}

4 Thermal Characteristics

Table 3. Package Description

Package Designator	Package Code (Case No.)	Package Description
ZP	5050 (1103-01)	PBGA 357 25*25*0.9P1.27
ZQ/VR	5058 (1103D-02)	PBGA 357 25*25*1.2P1.27



Characteristic	Symbol	Min	Max	Unit
Input leakage current, V_{in} = 3.6 V (except TMS, TRST, DSCK, and DSDI pins)	l _{in}	—	10	μA
Input leakage current, V _{in} = 0 V (except TMS, TRST, DSCK, and DSDI pins)	l _{in}	—	10	μA
Input capacitance ²	C _{in}	—	20	pF
Output high voltage, $I_{OH} = -2.0$ mA, $V_{DDH} = 3.0$ V (except XTAL, XFC, and open-drain pins)	V _{OH}	2.4	—	V
$\label{eq:IDE_Interm} \begin{array}{ c c c c c } \hline Output low voltage \\ I_{OL} = 2.0 \text{ mA, CLKOUT} \\ I_{OL} = 3.2 \text{ mA}^3 \\ I_{OL} = 5.3 \text{ mA}^4 \\ I_{OL} = 7.0 \text{ mA, TXD1/PA14, TXD2/PA12} \\ I_{OL} = 8.9 \text{ mA, TS, TA, TEA, BI, BB, HRESET, SRESET} \end{array}$	V _{OL}		0.5	V

Table 6. DC Electrical Specifications (continued)

 1 V_{IL}(max) for the I²C interface is 0.8 V rather than the 1.5 V as specified in the I²C standard.

² Input capacitance is periodically sampled.

- ³ A(0:31), TSIZ0/REG, TSIZ1, D(0:31), DP(0:3)/IRQ(3:6), RD/WR, BURST, RSV/IRQ2, IP_B(0:1)/IWP(0:1)/VFLS(0:1), IP_B2/IOIS16_B/AT2, IP_B3/IWP2/VF2, IP_B4/LWP0/VF0, IP_B5/LWP1/VF1, IP_B6/DSDI/AT0, IP_B7/PTR/AT3, RXD1/PA15, RXD2/PA13, L1TXDB/PA11, L1RXDB/PA10, L1TXDA/PA9, L1RXDA/PA8, TIN1/L1RCLKA/BRGO1/CLK1/PA7, BRGCLK1/TOUT1/CLK2/PA6, TIN2/L1TCLKA/BRGO2/CLK3/PA5, TOUT2/CLK4/PA4, TIN3/BRGO3/CLK5/PA3, BRGCLK2/ L1RCLKB/TOUT3/CLK6/PA2, TIN4/BRGO4/CLK7/PA1, L1TCLKB/TOUT4/CLK8/PA0, REJCT1/SPISEL/PB31, SPICLK/ PB30,SPIMOSI/PB29, BRGO4/SPIMISO/PB28, BRGO1/I2CSDA/PB27, BRGO2/I2CSCL/PB26, SMTXD1/PB25, SMRXD1/ PB24, SMSYN1/SDACK1/PB23, SMSYN2/SDACK2/PB22, SMTXD2/L1CLKOB/PB21, SMRXD2/L1CLKOA/PB20, L1ST1/ RTS1/PB19, L1ST2/RTS2/PB18, L1ST3/L1RQB/PB17, L1ST4/L1RQA/PB16, BRGO3/PB15, RSTRT1/PB14, L1ST1/RTS1/ DREQ0/PC15, L1ST2/RTS2/DREQ1/PC14, L1ST3/L1RQB/PC13, L1ST4/L1RQA/PC12, CTS1/PC11, TGATE1/CD1/PC10, CTS2/PC9, TGATE2/CD2/PC8, SDACK2/L1TSYNCB/PC7, L1RSYNCB/PC6, SDACK1/L1TSYNCA/PC5, L1RSYNCA/PC4, PD15, PD14, PD13, PD12, PD11, PD10, PD9, PD8, PD5, PD6, PD7, PD4, PD3, MII_MDC, MII_TX_ER, MII_EN, MII_MDIO, and MII_TXD[0:3]
- ⁴ BDIP/GPL_B(5), BR, BG, FRZ/IRQ6, CS(0:5), CS(6)/CE(1)_B, CS(7)/CE(2)_B, WE0/BS_B0/IORD, WE1/BS_B1/IOWR, WE2/BS_B2/PCOE, WE3/BS_B3/PCWE, BS_A(0:3), GPL_A0/GPL_B0, OE/GPL_A1/GPL_B1, GPL_A(2:3)/GPL_B(2:3)/ CS(2:3), UPWAITA/GPL_A4, UPWAITB/GPL_B4, GPL_A5, ALE_A, CE1_A, CE2_A, ALE_B/DSCK/AT1, OP(0:1), OP2/MODCK1/STS, OP3/MODCK2/DSDO, and BADDR(28:30)



Thermal Calculation and Measurement

7 Thermal Calculation and Measurement

For the following discussions, $P_D = (V_{DD} \times I_{DD}) + PI/O$, where PI/O is the power dissipation of the I/O drivers.

7.1 Estimation with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J, in °C can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

 T_A = ambient temperature (°C)

 $R_{\theta JA}$ = package junction-to-ambient thermal resistance (°C/W)

 P_D = power dissipation in package

The junction-to-ambient thermal resistance is an industry standard value which provides a quick and easy estimation of thermal performance. However, the answer is only an estimate; test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

7.2 Estimation with Junction-to-Case Thermal Resistance

Historically, the thermal resistance has frequently been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

 $R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

where:

 $R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

 $R_{\theta IC}$ = junction-to-case thermal resistance (°C/W)

 $R_{\theta CA}$ = case-to-ambient thermal resistance (°C/W)

 $R_{\theta JC}$ is device related and cannot be influenced by the user. The user adjusts the thermal environment to affect the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the airflow around the device, add a heat sink, change the mounting arrangement on the printed-circuit board, or change the thermal dissipation on the printed-circuit board surrounding the device. This thermal model is most useful for ceramic packages with heat sinks where some 90% of the heat flows through the case and the heat sink to the ambient environment. For most packages, a better model is required.

7.3 Estimation with Junction-to-Board Thermal Resistance

A simple package thermal model which has demonstrated reasonable accuracy (about 20%) is a two-resistor model consisting of a junction-to-board and a junction-to-case thermal resistance. The junction-to-case thermal resistance covers the situation where a heat sink is used or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed-circuit board. It has been observed that the thermal performance of most plastic packages, especially PBGA packages, is strongly dependent on the board temperature; see Figure 2.



		33	MHz	40	MHz	50 I	MHz	66 I	MHz	
Num	Characteristic	Min	Мах	Min	Max	Min	Мах	Min	Max	Unit
B23	CLKOUT rising edge to \overline{CS} negated GPCM read access, GPCM write access ACS = 00, TRLX = 0, and CSNT = 0	2.00	8.00	2.00	8.00	2.00	8.00	2.00	8.00	ns
B24	A(0:31) and BADDR(28:30) to \overline{CS} asserted GPCM ACS = 10, TRLX = 0	5.58	—	4.25	_	3.00	_	1.79	—	ns
B24a	A(0:31) and BADDR(28:30) to \overline{CS} asserted GPCM ACS = 11, TRLX = 0	13.15	—	10.50	—	8.00	—	5.58	—	ns
B25	CLKOUT rising edge to \overline{OE} , \overline{WE} (0:3) asserted	—	9.00	—	9.00	—	9.00	—	9.00	ns
B26	CLKOUT rising edge to OE negated	2.00	9.00	2.00	9.00	2.00	9.00	2.00	9.00	ns
B27	A(0:31) and BADDR(28:30) to \overline{CS} asserted GPCM ACS = 10, TRLX = 1	35.88	_	29.25	_	23.00	_	16.94	_	ns
B27a	A(0:31) and BADDR(28:30) to \overline{CS} asserted GPCM ACS = 11, TRLX = 1	43.45	—	35.50	—	28.00	—	20.73	—	ns
B28	CLKOUT rising edge to $\overline{WE}(0:3)$ negated GPCM write access CSNT = 0	—	9.00	—	9.00	—	9.00	—	9.00	ns
B28a	CLKOUT falling edge to $\overline{WE}(0:3)$ negated GPCM write access TRLX = 0, 1, CSNT = 1, EBDF = 0	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.54	ns
B28b	CLKOUT falling edge to \overline{CS} negated GPCM write access TRLX = 0, 1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 0	—	14.33	—	13.00		11.75		10.54	ns
B28c	CLKOUT falling edge to \overline{WE} (0:3) negated GPCM write access TRLX = 0, 1, CSNT = 1 write access TRLX = 0, CSNT = 1, EBDF = 1	10.86	17.99	8.88	16.00	7.00	14.13	5.18	12.31	ns
B28d	CLKOUT falling edge to \overline{CS} negated GPCM write access TRLX = 0, 1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 1	_	17.99	_	16.00		14.13		12.31	ns
B29	$\overline{WE}(0:3)$ negated to D(0:31), DP(0:3) High-Z GPCM write access CSNT = 0, EBDF = 0	5.58	_	4.25	—	3.00	—	1.79	—	ns
B29a	$\overline{WE}(0:3)$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 0	13.15	—	10.5	—	8.00		5.58	—	ns
B29b	$\overline{\text{CS}}$ negated to D(0:31), DP(0:3), High-Z GPCM write access, ACS = 00, TRLX = 0, 1, and CSNT = 0	5.58		4.25		3.00		1.79		ns
B29c	$\overline{\text{CS}}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 0	13.15		10.5		8.00		5.58		ns

Table 7. Bus Operation Timings (continued)



Figure 3 is the control timing diagram.



Figure 4 provides the timing for the external clock.



Figure 4. External Clock Timing



Bus Signal Timing

Figure 5 provides the timing for the synchronous output signals.



Figure 5. Synchronous Output Signals Timing

Figure 6 provides the timing for the synchronous active pull-up and open-drain output signals.



Figure 6. Synchronous Active Pull-Up Resistor and Open-Drain Outputs Signals Timing



Bus Signal Timing



Figure 15. External Bus Write Timing (GPCM Controlled—TRLX = 0 or 1, CSNT = 1)



Bus Signal Timing

Table 9 shows the PCMCIA timing for the MPC860.

Table 9. PCMCIA Timing

Num	Obevectovictic	33	MHz	40 I	MHz	50 I	MHz	66 I	MHz	11
Num	Characteristic	Min	Max	Min	Max	Min	Max	Min	Max	Unit
P44	A(0:31), REG valid to PCMCIA Strobe asserted ¹	20.73	—	16.75	—	13.00	—	9.36	—	ns
P45	A(0:31), $\overline{\text{REG}}$ valid to ALE negation ¹	28.30	—	23.00	—	18.00	—	13.15	_	ns
P46	CLKOUT to REG valid	7.58	15.58	6.25	14.25	5.00	13.00	3.79	11.84	ns
P47	CLKOUT to REG invalid	8.58	—	7.25	—	6.00	—	4.84	_	ns
P48	CLKOUT to $\overline{CE1}$, $\overline{CE2}$ asserted	7.58	15.58	6.25	14.25	5.00	13.00	3.79	11.84	ns
P49	CLKOUT to $\overline{CE1}$, $\overline{CE2}$ negated	7.58	15.58	6.25	14.25	5.00	13.00	3.79	11.84	ns
P50	CLKOUT to PCOE, IORD, PCWE, IOWR assert time	—	11.00		11.00	—	11.00	—	11.00	ns
P51	CLKOUT to PCOE, IORD, PCWE, IOWR negate time	2.00	11.00	2.00	11.00	2.00	11.00	2.00	11.00	ns
P52	CLKOUT to ALE assert time	7.58	15.58	6.25	14.25	5.00	13.00	3.79	10.04	ns
P53	CLKOUT to ALE negate time	—	15.58		14.25	_	13.00	—	11.84	ns
P54	PCWE, IOWR negated to D(0:31) invalid ¹	5.58	—	4.25	—	3.00	—	1.79	_	ns
P55	WAITA and WAITB valid to CLKOUT rising edge ¹		—	8.00	—	8.00	—	8.00	—	ns
P56	CLKOUT rising edge to WAITA and WAITB invalid ¹	2.00	—	2.00	—	2.00	—	2.00	—	ns

¹ PSST = 1. Otherwise add PSST times cycle time.

PSHT = 0. Otherwise add PSHT times cycle time.

These synchronous timings define when the WAITx signals are detected in order to freeze (or relieve) the PCMCIA current cycle. The WAITx assertion will be effective only if it is detected 2 cycles before the PSL timer expiration. See Chapter 16, "PCMCIA Interface," in the *MPC860 PowerQUICCTM Family User's Manual*.



Table 10 shows the PCMCIA port timing for the MPC860.

Table 10. PCMCIA Port Timing

Num	Characteristic	33	MHz	40 I	ИНz	50 MHz		66 MHz		Unit
	Characteristic	Min	Max	Min	Max	Min	Max	Min	Max	0.int
P57	CLKOUT to OPx valid	—	19.00	_	19.00	_	19.00	_	19.00	ns
P58	HRESET negated to OPx drive ¹	25.73		21.75		18.00		14.36	_	ns
P59	IP_Xx valid to CLKOUT rising edge	5.00		5.00		5.00		5.00	_	ns
P60	CLKOUT rising edge to IP_Xx invalid	1.00		1.00		1.00		1.00	-	ns

¹ OP2 and OP3 only.

Figure 28 provides the PCMCIA output port timing for the MPC860.



Figure 28. PCMCIA Output Port Timing

Figure 29 provides the PCMCIA output port timing for the MPC860.



Figure 29. PCMCIA Input Port Timing



IEEE 1149.1 Electrical Specifications



Figure 35. JTAG Test Clock Input Timing



Figure 36. JTAG Test Access Port Timing Diagram



Figure 37. JTAG TRST Timing Diagram







Figure 42. PIP TX (Pulse Mode) Timing Diagram





Figure 47. SDACK Timing Diagram—Peripheral Write, Internally-Generated TA



Figure 48. SDACK Timing Diagram—Peripheral Read, Internally-Generated TA



Num	Characteristic	All Freq	- Unit	
Nulli	Characteristic	Min		
84	L1CLK edge to L1CLKO valid (DSC = 1)	—	30.00	ns
85	L1RQ valid before falling edge of L1TSYNC ⁴	1.00	—	L1TCL K
86	L1GR setup time ²	42.00	—	ns
87	L1GR hold time	42.00	—	ns
88	L1CLK edge to L1SYNC valid (FSD = 00) CNT = 0000, BYT = 0, DSC = 0)	—	0.00	ns

Table 19. SI Timing (continued)

¹ The ratio SYNCCLK/L1RCLK must be greater than 2.5/1.

² These specs are valid for IDL mode only.

³ Where P = 1/CLKOUT. Thus, for a 25-MHz CLKO1 rate, P = 40 ns.

⁴ These strobes and TxD on the first bit of the frame become valid after L1CLK edge or L1SYNC, whichever comes later.



Figure 51. SI Receive Timing Diagram with Normal Clocking (DSC = 0)





MPC860 PowerQUICC Family Hardware Specifications, Rev. 10



Figure 56 through Figure 58 show the NMSI timings.





CPM Electrical Characteristics









11.12 I²C AC Electrical Specifications

Table 26 provides the I^2C (SCL < 100 kHz) timings.

Table 26. I²C Timing (SCL < 100 kHz)

Num	n Characteristic 0 SCL clock frequency (slave) 0 SCL clock frequency (master) ¹ 2 Bus free time between transmissions 3 Low period of SCL 4 High period of SCL 5 Start condition setup time 6 Start condition hold time 7 Data hold time	All Freq	All Frequencies				
Nulli		Min	encies Max 100 100 	Unit			
200	SCL clock frequency (slave)	0	100	kHz			
200	SCL clock frequency (master) ¹	1.5	100	kHz			
202	Bus free time between transmissions	4.7	—	μS			
203	Low period of SCL	4.7	—	μS			
204	High period of SCL	4.0	—	μS			
205	Start condition setup time	4.7	—	μS			
206	Start condition hold time	4.0	—	μS			
207	Data hold time	0	—	μS			
208	Data setup time	250	—	ns			
209	SDL/SCL rise time	—	1	μS			
210	SDL/SCL fall time	—	300	ns			
211	Stop condition setup time	4.7	—	μS			

SCL frequency is given by SCL = BRGCLK_frequency / ((BRG register + 3 × pre_scaler × 2). The ratio SYNCCLK/(BRGCLK/pre_scaler) must be greater than or equal to 4/1.

Table 27 provides the I^2C (SCL > 100 kHz) timings.

Table 27. . I²C Timing (SCL > 100 kHz)

Num	Characteristic	Expression	All Freq	uencies	Unit
Num	Characteristic	$\begin{tabular}{ c c c c } \hline HI Frequencies & HI Freque$	Unit		
200	SCL clock frequency (slave)	fSCL	0	BRGCLK/48	Hz
200	SCL clock frequency (master) ¹	fSCL	BRGCLK/16512	BRGCLK/48	Hz
202	Bus free time between transmissions		1/(2.2 * fSCL)	—	S
203	Low period of SCL		1/(2.2 * fSCL)	—	S
204	High period of SCL		1/(2.2 * fSCL)	_	S
205	Start condition setup time		1/(2.2 * fSCL)	—	S
206	Start condition hold time		1/(2.2 * fSCL)	—	S
207	Data hold time		0	_	S
208	Data setup time		1/(40 * fSCL)	—	S
209	SDL/SCL rise time		—	1/(10 * fSCL)	S
210	SDL/SCL fall time		—	1/(33 * fSCL)	S
211	Stop condition setup time		1/2(2.2 * fSCL)	—	s

SCL frequency is given by SCL = BRGCLK_frequency / ((BRG register + 3) × pre_scaler × 2). The ratio SYNCCLK/(BRGCLK / pre_scaler) must be greater than or equal to 4/1.



13.3 MII Async Inputs Signal Timing (MII_CRS, MII_COL)

Table 31 provides information on the MII async inputs signal timing.

Table 31. MII Async Inputs Signal Timing

Num	Characteristic	Min	Мах	Unit
M9	MII_CRS, MII_COL minimum pulse width	1.5		MII_TX_CLK period

Figure 74 shows the MII asynchronous inputs signal timing diagram.



13.4 MII Serial Management Channel Timing (MII_MDIO, MII_MDC)

Table 32 provides information on the MII serial management channel signal timing. The FEC functions correctly with a maximum MDC frequency in excess of 2.5 MHz. The exact upper bound is under investigation.

Num	Characteristic	Min	Мах	Unit
M10	MII_MDC falling edge to MII_MDIO output invalid (minimum propagation delay)	0	_	ns
M11	MII_MDC falling edge to MII_MDIO output valid (max prop delay)	_	25	ns
M12	MII_MDIO (input) to MII_MDC rising edge setup	10	—	ns
M13	MII_MDIO (input) to MII_MDC rising edge hold	0	—	ns
M14	MII_MDC pulse width high	40%	60%	MII_MDC period
M15	MII_MDC pulse width low	40%	60%	MII_MDC period

Table 32. MII Serial Management Channel Timing



14.2 Pin Assignments

Figure 76 shows the top view pinout of the PBGA package. For additional information, see the MPC860 PowerQUICC User's Manual, or the MPC855T User's Manual.

	\sim	~	\sim	\sim	\sim	~	~	~	~	~	~	~	~	~	~	\sim	\sim		
	O PD10	O PD8	O PD3		O D0	O D4	⊖ D1	() D2	О D3	O D5		O D6	0 D7	0 D29	DP2		с IPA3		W
O PD14	O PD13	O PD9	O PD6	O M_Tx_I		0 D13	() D27	〇 D10) D14	〇 D18	0 D20	〇 D24	() D28	O DP1	O DP3	O DP0	O N/C		V 1
0 PA0	O PB14	O PD15	O PD4	O PD5		() D8	() D23) D11) D16) D19	0 D21	〇 D26) D30	O IPA5	O IPA4	O IPA2	O N/C	O VSSSYN	U N
O PA1	O PC5	O PC4	O PD11) 1 D12	() D17) D9) D15	0 D22) D25	〇 D31	O IPA6) IPA1	O IPA7	⊖ xfc		T N
O PC6	0 PA2	O PB15	O PD12	\bigcirc		0	0	0	\bigcirc	0	0	0	0						R WR
O PA4	O PB17	O PA3		\bigcirc	$\bigcap_{i=1}^{n}$		\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	GND						Ρ
O PB19	O PA5	O PB18	O PB16	\bigcirc	0	\bigcirc	0					N							
O PA7	0 PC8	O PA6	O PC7	\bigcirc	\circ	\bigcirc	0) DR29 VDE	M							
O PB22	O PC9	O PA8	O PB20	\bigcirc	\circ	\bigcirc	0	О ОР0		O OP1		L 1							
O PC10	O PA9	O PB23	O PB21	\bigcirc	0	\bigcirc	\bigcirc	\bigcirc		\bigcirc	\bigcirc	\bigcirc	\bigcirc	0					к
O PC11	O PB24	O PA10	O PB25	\bigcirc	\circ	\bigcirc	0	O IPB5	O IPB1			J							
			О тск	\bigcirc	0	\bigcirc	0	О СО				н							
	_ ⊂ ™S		O PA11	\bigcirc	0	\bigcirc	0					G							
O PB26	O PC12	O PA12		\bigcirc			0	\bigcirc	0	\bigcirc	0	\bigcirc							F
O PB27	O PC13	O PA13	O PB29	\bigcirc		0	0	0	0	0	0	0	0		$\frac{\bigcirc}{CS3}$	O BI			E
0	0	0	0	0	\bigcirc	\bigcirc	0	0	0	0	<u> </u>	0	0	<u> </u>	<u> </u>	0	0	<u> </u>	D
									A25						$\frac{O}{O}$				С
				A9															В
AU								A23							$\frac{1}{000}$			GPLB4	A
19	А2 18	н5 17	А7 16	ATT 15	A14 14	А27 13	A29 12	АЗО 11	A28 10	A31 9	8	в5А2 7	vv⊨1 6	vv⊨3 5	4	3 3	2	1	

NOTE: This is the top view of the device.

Figure 76. Pinout of the PBGA Package