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Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	50MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	
Ethernet	10Mbps (2), 10/100Mbps (1)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 95°C (TA)
Security Features	-
Package / Case	357-BBGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc860dpzq50d4

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Overview

1 Overview

The MPC860 power quad integrated communications controller (PowerQUICCTM) is a versatile one-chip integrated microprocessor and peripheral combination designed for a variety of controller applications. It particularly excels in communications and networking systems. The PowerQUICC unit is referred to as the MPC860 in this hardware specification.

The MPC860 implements Power ArchitectureTM technology and contains a superset of Freescale's MC68360 quad integrated communications controller (QUICC), referred to here as the QUICC, RISC communications proceessor module (CPM). The CPU on the MPC860 is a 32-bit core built on Power Architecture technology that incorporates memory management units (MMUs) and instruction and data caches.. The CPM from the MC68360 QUICC has been enhanced by the addition of the inter-integrated controller (I²C) channel. The memory controller has been enhanced, enabling the MPC860 to support any type of memory, including high-performance memories and new types of DRAMs. A PCMCIA socket controller supports up to two sockets. A real-time clock has also been integrated.

Table 1 shows the functionality supported by the MPC860 family.

	Cache (Kbytes)		Ethernet					
Part	Instruction Cache	Data Cache	10T	10/100	ΑΤΜ	SCC	Reference ¹	
MPC860DE	4	4	Up to 2	_	_	2	1	
MPC860DT	4	4	Up to 2	1	Yes	2	1	
MPC860DP	16	8	Up to 2	1	Yes	2	1	
MPC860EN	4	4	Up to 4	—	—	4	1	
MPC860SR	4	4	Up to 4	—	Yes	4	1	
MPC860T	4	4	Up to 4	1	Yes	4	1	
MPC860P	16	8	Up to 4	1	Yes	4	1	
MPC855T	4	4	1	1	Yes	1	2	

Table 1. MPC860 Family Functionality

Supporting documentation for these devices refers to the following:

1. MPC860 PowerQUICC Family User's Manual (MPC860UM, Rev. 3)

2. MPC855T User's Manual (MPC855TUM, Rev. 1)



Features

- System integration unit (SIU)
 - Bus monitor
 - Software watchdog
 - Periodic interrupt timer (PIT)
 - Low-power stop mode
 - Clock synthesizer
 - Decrementer, time base, and real-time clock (RTC)
 - Reset controller
 - IEEE 1149.1TM Std. test access port (JTAG)
- Interrupts
 - Seven external interrupt request (IRQ) lines
 - 12 port pins with interrupt capability
 - 23 internal interrupt sources
 - Programmable priority between SCCs
 - Programmable highest priority request
- 10/100 Mbps Ethernet support, fully compliant with the IEEE 802.3u® Standard (not available when using ATM over UTOPIA interface)
- ATM support compliant with ATM forum UNI 4.0 specification
 - Cell processing up to 50–70 Mbps at 50-MHz system clock
 - Cell multiplexing/demultiplexing
 - Support of AAL5 and AAL0 protocols on a per-VC basis. AAL0 support enables OAM and software implementation of other protocols.
 - ATM pace control (APC) scheduler, providing direct support for constant bit rate (CBR) and unspecified bit rate (UBR) and providing control mechanisms enabling software support of available bit rate (ABR)
 - Physical interface support for UTOPIA (10/100-Mbps is not supported with this interface) and byte-aligned serial (for example, T1/E1/ADSL)
 - UTOPIA-mode ATM supports level-1 master with cell-level handshake, multi-PHY (up to four physical layer devices), connection to 25-, 51-, or 155-Mbps framers, and UTOPIA/system clock ratios of 1/2 or 1/3.
 - Serial-mode ATM connection supports transmission convergence (TC) function for T1/E1/ADSL lines, cell delineation, cell payload scrambling/descrambling, automatic idle/unassigned cell insertion/stripping, header error control (HEC) generation, checking, and statistics.
- Communications processor module (CPM)
 - RISC communications processor (CP)
 - Communication-specific commands (for example, GRACEFUL STOP TRANSMIT, ENTER HUNT MODE, and RESTART TRANSMIT)
 - Supports continuous mode transmission and reception on all serial channels



Table 4 shows the thermal characteristics for the MPC860.

Table 4. MPC860 Thermal Resistance Data

Rating	Env	Environment		ZP MPC860P	ZQ / VR MPC860P	Unit
Mold Compound Thicknes	s		0.85	1.15	mm	
Junction-to-ambient ¹	Natural convection	Single-layer board (1s)	$R_{\theta JA}^2$	34	34	°C/W
		Four-layer board (2s2p)	$R_{\theta JMA}^{3}$	22	22	
	Airflow (200 ft/min)	Single-layer board (1s)	$R_{\theta JMA}^{3}$	27	27	
		Four-layer board (2s2p)	$R_{\theta JMA}^{3}$	18	18	
Junction-to-board ⁴			$R_{\theta JB}$	14	13	
Junction-to-case ⁵			R_{\thetaJC}	6	8	
Junction-to-package top ⁶	Natural convection		Ψ_{JT}	2	2	

¹ Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.

² Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.

³ Per JEDEC JESD51-6 with the board horizontal.

⁴ Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

- ⁵ Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature. For exposed pad packages where the pad would be expected to be soldered, junction-to-case thermal resistance is a simulated value from the junction to the exposed pad without contact resistance.
- ⁶ Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2.



Thermal Calculation and Measurement



Figure 2. Effect of Board Temperature Rise on Thermal Behavior

If the board temperature is known, an estimate of the junction temperature in the environment can be made using the following equation:

$$T_{J} = T_{B} + (R_{\theta JB} \times P_{D})$$

where:

 $R_{\theta JB}$ = junction-to-board thermal resistance (°C/W)

 $T_B =$ board temperature (°C)

 P_D = power dissipation in package

If the board temperature is known and the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. For this method to work, the board and board mounting must be similar to the test board used to determine the junction-to-board thermal resistance, namely a 2s2p (board with a power and a ground plane) and by attaching the thermal balls to the ground plane.

7.4 Estimation Using Simulation

When the board temperature is not known, a thermal simulation of the application is needed. The simple two-resistor model can be used with the thermal simulation of the application [2], or a more accurate and complex model of the package can be used in the thermal simulation.

7.5 Experimental Determination

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$





Table 7 provides the bus operation timing for the MPC860 at 33, 40, 50, and 66 MHz.

The maximum bus speed supported by the MPC860 is 66 MHz. Higher-speed parts must be operated in half-speed bus mode (for example, an MPC860 used at 80 MHz must be configured for a 40-MHz bus).

The timing for the MPC860 bus shown assumes a 50-pF load for maximum delays and a 0-pF load for minimum delays.

NI	Oh ann at an i a tio	33 MHz		40 MHz		50 MHz		66 MHz		11
NUM	Characteristic	Min	Max	Min	Max	Min	Max	Min	Max	Unit
B1	CLKOUT period	30.30	30.30	25.00	30.30	20.00	30.30	15.15	30.30	ns
B1a	EXTCLK to CLKOUT phase skew (EXTCLK > 15 MHz and MF <= 2)	-0.90	0.90	-0.90	0.90	-0.90	0.90	-0.90	0.90	ns
B1b	EXTCLK to CLKOUT phase skew (EXTCLK > 10 MHz and MF < 10)	-2.30	2.30	-2.30	2.30	-2.30	2.30	-2.30	2.30	ns
B1c	CLKOUT phase jitter (EXTCLK > 15 MHz and MF <= 2) ¹	-0.60	0.60	-0.60	0.60	-0.60	0.60	-0.60	0.60	ns
B1d	CLKOUT phase jitter ¹	-2.00	2.00	-2.00	2.00	-2.00	2.00	-2.00	2.00	ns
B1e	CLKOUT frequency jitter (MF < 10) ¹	_	0.50	_	0.50	_	0.50	_	0.50	%
B1f	CLKOUT frequency jitter (10 < MF < 500) ¹	_	2.00	_	2.00	_	2.00	_	2.00	%
B1g	CLKOUT frequency jitter (MF > 500) ¹	_	3.00	—	3.00	_	3.00	_	3.00	%
B1h	Frequency jitter on EXTCLK ²	_	0.50	_	0.50	_	0.50	_	0.50	%
B2	CLKOUT pulse width low	12.12	—	10.00	_	8.00	—	6.06	_	ns
B3	CLKOUT width high	12.12	—	10.00	_	8.00	—	6.06	_	ns
B4	CLKOUT rise time ³	_	4.00	—	4.00	—	4.00	—	4.00	ns
B5 ³³	CLKOUT fall time ³	_	4.00	—	4.00	—	4.00	—	4.00	ns
B7	CLKOUT to A(0:31), BADDR(28:30), RD/WR, BURST, D(0:31), DP(0:3) invalid	7.58	—	6.25	—	5.00	—	3.80	—	ns
B7a	CLKOUT to TSIZ(0:1), $\overline{\text{REG}}$, $\overline{\text{RSV}}$, AT(0:3), $\overline{\text{BDIP}}$, PTR invalid	7.58	—	6.25	—	5.00	—	3.80	—	ns
B7b	CLKOUT to BR, BG, FRZ, VFLS(0:1), VF(0:2) IWP(0:2), LWP(0:1), STS invalid ⁴	7.58	—	6.25	—	5.00	—	3.80	—	ns
B8	CLKOUT to A(0:31), BADDR(28:30) RD/WR, BURST, D(0:31), DP(0:3) valid	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.04	ns
B8a	CLKOUT to TSIZ(0:1), REG, RSV, AT(0:3) BDIP, PTR valid	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.04	ns
B8b	CLKOUT to BR, BG, VFLS(0:1), VF(0:2), IWP(0:2), FRZ, LWP(0:1), STS valid ⁴	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.04	ns

Table 7. Bus Operation Timings



		33	MHz	40 MHz		50 MHz		66 MHz		
Num	Characteristic	Min	Max	Min	Max	Min	Max	Min	Max	Unit
B9	CLKOUT to A(0:31), BADDR(28:30), RD/WR, BURST, D(0:31), DP(0:3), TSIZ(0:1), REG, RSV, AT(0:3), PTR High-Z	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.04	ns
B11	CLKOUT to \overline{TS} , \overline{BB} assertion	7.58	13.58	6.25	12.25	5.00	11.00	3.80	11.29	ns
B11a	CLKOUT to \overline{TA} , \overline{BI} assertion (when driven by the memory controller or PCMCIA interface)	2.50	9.25	2.50	9.25	2.50	9.25	2.50	9.75	ns
B12	CLKOUT to \overline{TS} , \overline{BB} negation	7.58	14.33	6.25	13.00	5.00	11.75	3.80	8.54	ns
B12a	CLKOUT to \overline{TA} , \overline{BI} negation (when driven by the memory controller or PCMCIA interface)	2.50	11.00	2.50	11.00	2.50	11.00	2.50	9.00	ns
B13	CLKOUT to TS, BB High-Z	7.58	21.58	6.25	20.25	5.00	19.00	3.80	14.04	ns
B13a	CLKOUT to \overline{TA} , \overline{BI} High-Z (when driven by the memory controller or PCMCIA interface)	2.50	15.00	2.50	15.00	2.50	15.00	2.50	15.00	ns
B14	CLKOUT to TEA assertion	2.50	10.00	2.50	10.00	2.50	10.00	2.50	9.00	ns
B15	CLKOUT to TEA High-Z	2.50	15.00	2.50	15.00	2.50	15.00	2.50	15.00	ns
B16	TA, BI valid to CLKOUT (setup time)	9.75		9.75		9.75	_	6.00	_	ns
B16a	TEA, KR, RETRY, CR valid to CLKOUT (setup time)	10.00	_	10.00	—	10.00	—	4.50	—	ns
B16b	$\overline{\text{BB}}, \overline{\text{BG}}, \overline{\text{BR}}, \text{ valid to CLKOUT (setup time)}^5$	8.50		8.50		8.50	_	4.00	_	ns
B17	CLKOUT to \overline{TA} , \overline{TEA} , \overline{BI} , \overline{BB} , \overline{BG} , \overline{BR} valid (hold time)	1.00	—	1.00	—	1.00	—	2.00	—	ns
B17a	CLKOUT to KR, RETRY, CR valid (hold time)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B18	D(0:31), DP(0:3) valid to CLKOUT rising edge (setup time) ⁶	6.00	—	6.00	—	6.00	—	6.00	—	ns
B19	CLKOUT rising edge to D(0:31), DP(0:3) valid (hold time) ⁶	1.00	—	1.00	—	1.00	—	2.00	—	ns
B20	D(0:31), DP(0:3) valid to CLKOUT falling edge (setup time) ⁷	4.00	—	4.00	—	4.00	—	4.00	—	ns
B21	CLKOUT falling edge to D(0:31), DP(0:3) valid (hold time) ⁷	2.00	—	2.00	—	2.00	—	2.00	—	ns
B22	CLKOUT rising edge to \overline{CS} asserted GPCM ACS = 00	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.04	ns
B22a	CLKOUT falling edge to \overline{CS} asserted GPCM ACS = 10, TRLX = 0		8.00		8.00		8.00		8.00	ns
B22b	CLKOUT falling edge to \overline{CS} asserted GPCM ACS = 11, TRLX = 0, EBDF = 0	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.54	ns
B22c	CLKOUT falling edge to \overline{CS} asserted GPCM ACS = 11, TRLX = 0, EBDF = 1	10.86	17.99	8.88	16.00	7.00	14.13	5.18	12.31	ns

Table 7. Bus Operation Timings (continued)





Figure 20 provides the timing for the synchronous external master access controlled by the GPCM.

Figure 20. Synchronous External Master Access Timing (GPCM Handled ACS = 00)

Figure 21 provides the timing for the asynchronous external master memory access controlled by the GPCM.





Figure 22 provides the timing for the asynchronous external master control signals negation.



Figure 22. Asynchronous External Master—Control Signals Negation Timing



1

Table 8 provides interrupt timing for the MPC860.

Table 8. Interrupt Timing

Num	Characteristic1	All Freq	Unit	
Num	Characteristic	Min	Мах	Unit
139	IRQx valid to CLKOUT rising edge (setup time)	6.00	_	ns
140	IRQx hold time after CLKOUT	2.00	_	ns
141	IRQx pulse width low	3.00	—	ns
142	IRQx pulse width high	3.00	_	ns
143	IRQx edge-to-edge time	$4 \times T_{CLOCKOUT}$	—	—

The timings I39 and I40 describe the testing conditions under which the IRQ lines are tested when being defined as level-sensitive. The IRQ lines are synchronized internally and do not have to be asserted or negated with reference to the CLKOUT.

The timings I41, I42, and I43 are specified to allow the correct function of the IRQ lines detection circuitry and have no direct relation with the total system interrupt latency that the MPC860 is able to support.

Figure 23 provides the interrupt detection timing for the external level-sensitive lines.



Figure 23. Interrupt Detection Timing for External Level Sensitive Lines

Figure 24 provides the interrupt detection timing for the external edge-sensitive lines.



Figure 24. Interrupt Detection Timing for External Edge Sensitive Lines



Table 9 shows the PCMCIA timing for the MPC860.

Table 9. PCMCIA Timing

Num	Oberneterietie	33	MHz	40 MHz		50 MHz		66 MHz		Unit
Num	Characteristic	Min	Max	Min	Max	Min	Max	Min	Max	Unit
P44	A(0:31), REG valid to PCMCIA Strobe asserted ¹	20.73	—	16.75	—	13.00	—	9.36	—	ns
P45	A(0:31), $\overline{\text{REG}}$ valid to ALE negation ¹	28.30	—	23.00	—	18.00	—	13.15	_	ns
P46	CLKOUT to REG valid	7.58	15.58	6.25	14.25	5.00	13.00	3.79	11.84	ns
P47	CLKOUT to REG invalid	8.58	—	7.25	—	6.00	—	4.84	_	ns
P48	CLKOUT to $\overline{CE1}$, $\overline{CE2}$ asserted	7.58	15.58	6.25	14.25	5.00	13.00	3.79	11.84	ns
P49	CLKOUT to $\overline{CE1}$, $\overline{CE2}$ negated	7.58	15.58	6.25	14.25	5.00	13.00	3.79	11.84	ns
P50	CLKOUT to PCOE, IORD, PCWE, IOWR assert time	—	11.00		11.00	—	11.00	—	11.00	ns
P51	CLKOUT to PCOE, IORD, PCWE, IOWR negate time	2.00	11.00	2.00	11.00	2.00	11.00	2.00	11.00	ns
P52	CLKOUT to ALE assert time	7.58	15.58	6.25	14.25	5.00	13.00	3.79	10.04	ns
P53	CLKOUT to ALE negate time	—	15.58		14.25	_	13.00	—	11.84	ns
P54	PCWE, IOWR negated to D(0:31) invalid ¹	5.58	—	4.25	—	3.00	—	1.79	_	ns
P55	WAITA and WAITB valid to CLKOUT rising edge ¹	8.00	—	8.00	—	8.00	—	8.00	—	ns
P56	CLKOUT rising edge to WAITA and WAITB invalid ¹	2.00	—	2.00	—	2.00	—	2.00	—	ns

¹ PSST = 1. Otherwise add PSST times cycle time.

PSHT = 0. Otherwise add PSHT times cycle time.

These synchronous timings define when the WAITx signals are detected in order to freeze (or relieve) the PCMCIA current cycle. The WAITx assertion will be effective only if it is detected 2 cycles before the PSL timer expiration. See Chapter 16, "PCMCIA Interface," in the *MPC860 PowerQUICCTM Family User's Manual*.





Figure 25 provides the PCMCIA access cycle timing for the external bus read.

Figure 25. PCMCIA Access Cycle Timing External Bus Read







Figure 26. PCMCIA Access Cycle Timing External Bus Write

Figure 27 provides the PCMCIA \overline{WAIT} signal detection timing.



Figure 27. PCMCIA WAIT Signal Detection Timing



CPM Electrical Characteristics

Num	Charactariatia	All Freq	Unit	
Nulli	Characteristic	Min	Мах	Unit
42	SDACK assertion delay from clock high	—	12	ns
43	SDACK negation delay from clock low	—	12	ns
44	SDACK negation delay from TA low	—	20	ns
45	SDACK negation delay from clock high	_	15	ns
46	\overline{TA} assertion to rising edge of the clock setup time (applies to external \overline{TA})	7		ns

Table 16. IDMA Controller Timing (continued)



Figure 45. IDMA External Requests Timing Diagram



Figure 46. SDACK Timing Diagram—Peripheral Write, Externally-Generated TA



CPM Electrical Characteristics



Figure 47. SDACK Timing Diagram—Peripheral Write, Internally-Generated TA



Figure 48. SDACK Timing Diagram—Peripheral Read, Internally-Generated TA





Figure 50. CPM General-Purpose Timers Timing Diagram

11.6 Serial Interface AC Electrical Specifications

Table 19 provides the serial interface timings as shown in Figure 51 through Figure 55.

Num	Obevectovictie	All Frec	Unit	
NUM	Characteristic	Min	Max	Unit
70	L1RCLK, L1TCLK frequency (DSC = 0) ^{1, 2}	—	SYNCCLK/2.5	MHz
71	L1RCLK, L1TCLK width low $(DSC = 0)^2$	P + 10	—	ns
71a	L1RCLK, L1TCLK width high $(DSC = 0)^3$	P + 10	—	ns
72	L1TXD, L1ST(1–4), L1RQ, L1CLKO rise/fall time	—	15.00	ns
73	L1RSYNC, L1TSYNC valid to L1CLK edge (SYNC setup time)	20.00	—	ns
74	L1CLK edge to L1RSYNC, L1TSYNC, invalid (SYNC hold time)	35.00	—	ns
75	L1RSYNC, L1TSYNC rise/fall time	—	15.00	ns
76	L1RXD valid to L1CLK edge (L1RXD setup time)	17.00	—	ns
77	L1CLK edge to L1RXD invalid (L1RXD hold time)	13.00	—	ns
78	L1CLK edge to L1ST(1-4) valid ⁴	10.00	45.00	ns
78A	L1SYNC valid to L1ST(1-4) valid	10.00	45.00	ns
79	L1CLK edge to L1ST(1-4) invalid	10.00	45.00	ns
80	L1CLK edge to L1TXD valid	10.00	55.00	ns
80A	L1TSYNC valid to L1TXD valid ⁴	10.00	55.00	ns
81	L1CLK edge to L1TXD high impedance	0.00	42.00	ns
82	L1RCLK, L1TCLK frequency (DSC =1)	—	16.00 or SYNCCLK/2	MHz
83	L1RCLK, L1TCLK width low (DSC = 1)	P + 10	_	ns
83a	L1RCLK, L1TCLK width high $(DSC = 1)^3$	P + 10	—	ns

Table 19. SI Timing



CPM Electrical Characteristics

Num	Characteristic	All Freq	Unit	
Nulli	Characteristic	Min	Мах	Onit
84	L1CLK edge to L1CLKO valid (DSC = 1)	—	30.00	ns
85	L1RQ valid before falling edge of L1TSYNC ⁴	1.00	—	L1TCL K
86	L1GR setup time ²	42.00	—	ns
87	L1GR hold time	42.00	—	ns
88	L1CLK edge to L1SYNC valid (FSD = 00) CNT = 0000, BYT = 0, DSC = 0)	—	0.00	ns

Table 19. SI Timing (continued)

¹ The ratio SYNCCLK/L1RCLK must be greater than 2.5/1.

² These specs are valid for IDL mode only.

³ Where P = 1/CLKOUT. Thus, for a 25-MHz CLKO1 rate, P = 40 ns.

⁴ These strobes and TxD on the first bit of the frame become valid after L1CLK edge or L1SYNC, whichever comes later.



Figure 51. SI Receive Timing Diagram with Normal Clocking (DSC = 0)



SCC in NMSI Mode Electrical Specifications 11.7

Table 20 provides the NMSI external clock timing.

Table 2	20. NMSI	External	Clock	Timing
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Num	Characteristic	All Freq	Unit	
Nulli	Characteristic	Min	Мах	Unit
100	RCLK1 and TCLK1 width high ¹	1/SYNCCLK	_	ns
101	RCLK1 and TCLK1 width low	1/SYNCCLK + 5		ns
102	RCLK1 and TCLK1 rise/fall time	—	15.00	ns
103	TXD1 active delay (from TCLK1 falling edge)	0.00	50.00	ns
104	RTS1 active/inactive delay (from TCLK1 falling edge)	0.00	50.00	ns
105	CTS1 setup time to TCLK1 rising edge	5.00	—	ns
106	RXD1 setup time to RCLK1 rising edge	5.00	_	ns
107	RXD1 hold time from RCLK1 rising edge ²	5.00	—	ns
108	CD1 setup Time to RCLK1 rising edge	5.00	_	ns

¹ The ratios SYNCCLK/RCLK1 and SYNCCLK/TCLK1 must be greater than or equal to 2.25/1.
 ² Also applies to CD and CTS hold time when they are used as external sync signals.

Table 21 provides the NMSI internal clock timing.

Table 21. NMSI Internal Clock Timing

Num	Characteristic	All Freq	11	
		Min	Мах	Unit
100	RCLK1 and TCLK1 frequency ¹	0.00	SYNCCLK/3	MHz
102	RCLK1 and TCLK1 rise/fall time	—	—	ns
103	TXD1 active delay (from TCLK1 falling edge)	0.00	30.00	ns
104	RTS1 active/inactive delay (from TCLK1 falling edge)	0.00	30.00	ns
105	CTS1 setup time to TCLK1 rising edge	40.00	—	ns
106	RXD1 setup time to RCLK1 rising edge	40.00	—	ns
107	RXD1 hold time from RCLK1 rising edge ²	0.00	—	ns
108	CD1 setup time to RCLK1 rising edge	40.00	_	ns

¹ The ratios SYNCCLK/RCLK1 and SYNCCLK/TCLK1 must be greater than or equal to 3/1.

² Also applies to \overline{CD} and \overline{CTS} hold time when they are used as external sync signals.



13 FEC Electrical Characteristics

This section provides the AC electrical specifications for the Fast Ethernet controller (FEC). Note that the timing specifications for the MII signals are independent of system clock frequency (part speed designation). Also, MII signals use TTL signal levels compatible with devices operating at either 5.0 V or 3.3 V.

13.1 MII Receive Signal Timing (MII_RXD[3:0], MII_RX_DV, MII_RX_ER, MII_RX_CLK)

The receiver functions correctly up to a MII_RX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed the MII_RX_CLK frequency - 1%.

Table 29 provides information on the MII receive signal timing.

Num	Characteristic	Min	Max	Unit
M1	MII_RXD[3:0], MII_RX_DV, MII_RX_ER to MII_RX_CLK setup	5		ns
M2	MII_RX_CLK to MII_RXD[3:0], MII_RX_DV, MII_RX_ER hold	5		ns
МЗ	MII_RX_CLK pulse width high	35%	65%	MII_RX_CLK period
M4	MII_RX_CLK pulse width low	35%	65%	MII_RX_CLK period

Table 29. Mll Receive Signal Timing

Figure 72 shows MII receive signal timing.



Figure 72. MII Receive Signal Timing Diagram



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Figure 75 shows the MII serial management channel timing diagram.



Figure 75. MII Serial Management Channel Timing Diagram

14 Mechanical Data and Ordering Information

14.1 Ordering Information

Table 33 provides information on the MPC860 Revision D.4 derivative devices.

Device	Number of SCCs ¹	Ethernet Support ² (Mbps)	Multichannel HDLC Support	ATM Support
MPC855T	1	10/100	Yes	Yes
MPC860DE	2	10	N/A	N/A
MPC860DT		10/100	Yes	Yes
MPC860DP		10/100	Yes	Yes
MPC860EN	4	10	N/A	N/A
MPC860SR		10	Yes	Yes
MPC860T		10/100	Yes	Yes
MPC860P		10/100	Yes	Yes

Table 33. MPC860 Family Revision D.4 Derivatives

¹ Serial communications controller (SCC)

² Up to 4 channels at 40 MHz or 2 channels at 25 MHz



Mechanical Data and Ordering Information

Package Type	Freq. (MHz) / Temp. (Tj)	Package	Order Number
Ball grid array <i>(continued)</i> ZP suffix—leaded ZQ suffix—leaded VR suffix—lead-free	80 0° to 95°C	ZP/ZQ ¹	MPC855TZQ80D4 MPC860DEZQ80D4 MPC860DTZQ80D4 MPC860ENZQ80D4 MPC860SRZQ80D4 MPC860TZQ80D4 MPC860DPZQ80D4 MPC860PZQ80D4
		Tape and Reel	MPC860PZQ80D4R2 MPC860PVR80D4R2
		VR	MPC855TVR80D4 MPC860DEVR80D4 MPC860DPVR80D4 MPC860ENVR80D4 MPC860PVR80D4 MPC860SRVR80D4 MPC860SRVR80D4
Ball grid array (CZP suffix) CZP suffix—leaded CZQ suffix—leaded CVR suffix—lead-free	50 –40° to 95°C	ZP/ZQ ¹	MPC855TCZQ50D4 MPC855TCVR50D4 MPC860DECZQ50D4 MPC860DTCZQ50D4 MPC860ENCZQ50D4 MPC860SRCZQ50D4 MPC860TCZQ50D4 MPC860DPCZQ50D4 MPC860PCZQ50D4
		Tape and Reel	MPC855TCZQ50D4R2 MC860ENCVR50D4R2
		CVR	MPC860DECVR50D4 MPC860DTCVR50D4 MPC860ENCVR50D4 MPC860PCVR50D4 MPC860SRCVR50D4 MPC860TCVR50D4
	66 –40° to 95°C	ZP/ZQ ¹	MPC855TCZQ66D4 MPC855TCVR66D4 MPC860ENCZQ66D4 MPC860SRCZQ66D4 MPC860TCZQ66D4 MPC860DPCZQ66D4 MPC860PCZQ66D4
		CVR	MPC860DTCVR66D4 MPC860ENCVR66D4 MPC860PCVR66D4 MPC860SRCVR66D4 MPC860TCVR66D4

Table 34. MPC860 Family Package/Frequency Availability (continued)

¹ The ZP package is no longer recommended for use. The ZQ package replaces the ZP package.



Mechanical Data and Ordering Information

14.3 Mechanical Dimensions of the PBGA Package

Figure 77 shows the mechanical dimensions of the ZP PBGA package.



- 1. Dimensions and tolerance per ASME Y14.5M, 1994.
- 2. Dimensions in millimeters.
- 3. Dimension b is the maximum solder ball diameter measured parallel to data C.



22.40

E2

22.60