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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	80MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (2), 10/100Mbps (1)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 95°C (TA)
Security Features	-
Package / Case	357-BBGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc860dpzq80d4

1 Overview

The MPC860 power quad integrated communications controller (PowerQUICC™) is a versatile one-chip integrated microprocessor and peripheral combination designed for a variety of controller applications. It particularly excels in communications and networking systems. The PowerQUICC unit is referred to as the MPC860 in this hardware specification.

The MPC860 implements Power Architecture™ technology and contains a superset of Freescale's MC68360 quad integrated communications controller (QUICC), referred to here as the QUICC, RISC communications proccessor module (CPM). The CPU on the MPC860 is a 32-bit core built on Power Architecture technology that incorporates memory management units (MMUs) and instruction and data caches.. The CPM from the MC68360 QUICC has been enhanced by the addition of the inter-integrated controller (I^2C) channel. The memory controller has been enhanced, enabling the MPC860 to support any type of memory, including high-performance memories and new types of DRAMs. A PCMCIA socket controller supports up to two sockets. A real-time clock has also been integrated.

Table 1 shows the functionality supported by the MPC860 family.

Table 1. MPC860 Family Functionality

Part	Cache (Kbytes)		Ethernet		ATM	SCC	Reference[1]
	Instruction Cache	Data Cache	10T	10/100			
MPC860DE	4	4	Up to 2	—	—	2	1
MPC860DT	4	4	Up to 2	1	Yes	2	1
MPC860DP	16	8	Up to 2	1	Yes	2	1
MPC860EN	4	4	Up to 4	—	—	4	1
MPC860SR	4	4	Up to 4	—	Yes	4	1
MPC860T	4	4	Up to 4	1	Yes	4	1
MPC860P	16	8	Up to 4	1	Yes	4	1
MPC855T	4	4	1	1	Yes	1	2

[1] Supporting documentation for these devices refers to the following:
1. MPC860 PowerQUICC Family User's Manual (MPC860UM, Rev. 3)
2. MPC855T User's Manual (MPC855TUM, Rev. 1)

3 Maximum Tolerated Ratings

This section provides the maximum tolerated voltage and temperature ranges for the MPC860. Table 2 provides the maximum ratings.

This device contains circuitry protecting against damage due to high-static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or V_{DD}).

Table 2. Maximum Tolerated Ratings

(GND = 0 V)

Rating	Symbol	Value	Unit
Supply voltage[1]	V_{DDH}	–0.3 to 4.0	V
	V_{DDL}	–0.3 to 4.0	V
	KAPWR	–0.3 to 4.0	V
	V_{DDSYN}	–0.3 to 4.0	V
Input voltage[2]	V_{in}	GND – 0.3 to V_{DDH}	V
Temperature[3] (standard)	$T_{A(min)}$	0	°C
	$T_{j(max)}$	95	°C
Temperature[3] (extended)	$T_{A(min)}$	–40	°C
	$T_{j(max)}$	95	°C
Storage temperature range	T_{stg}	–55 to 150	°C

1 The power supply of the device must start its ramp from 0.0 V.

2 Functional operating conditions are provided with the DC electrical specifications in Table 6. Absolute maximum ratings are stress ratings only; functional operation at the maxima is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device.
Caution: All inputs that tolerate 5 V cannot be more than 2.5 V greater than the supply voltage. This restriction applies to power-up and normal operation (that is, if the MPC860 is unpowered, voltage greater than 2.5 V must not be applied to its inputs).

3 Minimum temperatures are guaranteed as ambient temperature, T_A. Maximum temperatures are guaranteed as junction temperature, T_j.

5 Power Dissipation

Table 5 provides power dissipation information. The modes are 1:1, where CPU and bus speeds are equal, and 2:1, where CPU frequency is twice the bus speed.

Table 5. Power Dissipation (P_D)

Die Revision	Frequency (MHz)	Typical [1]	Maximum [2]	Unit
D.4 (1:1 mode)	50	656	735	mW
	66	TBD	TBD	mW
D.4 (2:1 mode)	66	722	762	mW
	80	851	909	mW

1 Typical power dissipation is measured at 3.3 V.
2 Maximum power dissipation is measured at 3.5 V.

NOTE

Values in Table 5 represent V_{DDL}-based power dissipation and do not include I/O power dissipation over V_{DDH}. I/O power dissipation varies widely by application due to buffer current, depending on external circuitry.

6 DC Characteristics

Table 6 provides the DC electrical characteristics for the MPC860.

Table 6. DC Electrical Specifications

Characteristic	Symbol	Min	Max	Unit
Operating voltage at 40 MHz or less	V_{DDH}, V_{DDL}, V_{DDSYN}	3.0	3.6	V
	KAPWR (power-down mode)	2.0	3.6	V
	KAPWR (all other operating modes)	V_{DDH} – 0.4	V_{DDH}	V
Operating voltage greater than 40 MHz	V_{DDH}, V_{DDL}, KAPWR, V_{DDSYN}	3.135	3.465	V
	KAPWR (power-down mode)	2.0	3.6	V
	KAPWR (all other operating modes)	V_{DDH} – 0.4	V_{DDH}	V
Input high voltage (all inputs except EXTAL and EXTCLK)	V_{IH}	2.0	5.5	V
Input low voltage[1]	V_{IL}	GND	0.8	V
EXTAL, EXTCLK input high voltage	V_{IHC}	0.7 × (V_{DDH})	V_{DDH} + 0.3	V
Input leakage current, V_{in} = 5.5 V (except TMS, $\overline{TRST}$, DSCK, and DSDI pins)	I_{in}	—	100	µA

Table 6. DC Electrical Specifications (continued)

Characteristic	Symbol	Min	Max	Unit
Input leakage current, V_{in} = 3.6 V (except TMS, $\overline{\text{TRST}}$, DSCK, and DSDI pins)	I_{In}	—	10	µA
Input leakage current, V_{in} = 0 V (except TMS, $\overline{\text{TRST}}$, DSCK, and DSDI pins)	I_{In}	—	10	µA
Input capacitance[2]	C_{in}	—	20	pF
Output high voltage, I_{OH} = –2.0 mA, V_{DDH} = 3.0 V (except XTAL, XFC, and open-drain pins)	V_{OH}	2.4	—	V
Output low voltage I_{OL} = 2.0 mA, CLKOUT I_{OL} = 3.2 mA [3] I_{OL} = 5.3 mA [4] I_{OL} = 7.0 mA, TXD1/PA14, TXD2/PA12 I_{OL} = 8.9 mA, $\overline{\text{TS}}$, $\overline{\text{TA}}$, $\overline{\text{TEA}}$, $\overline{\text{BI}}$, $\overline{\text{BB}}$, $\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$	V_{OL}	—	0.5	V

1 V_{IL}(max) for the I^2C interface is 0.8 V rather than the 1.5 V as specified in the I^2C standard.

2 Input capacitance is periodically sampled.

3 A(0:31), TSIZ0/$\overline{\text{REG}}$, TSIZ1, D(0:31), DP(0:3)/$\overline{\text{IRQ}}$(3:6), RD/$\overline{\text{WR}}$, $\overline{\text{BURST}}$, $\overline{\text{RSV}}$/$\overline{\text{IRQ2}}$, IP_B(0:1)/IWP(0:1)/VFLS(0:1), IP_B2/IOIS16_B/AT2, IP_B3/IWP2/VF2, IP_B4/LWP0/VF0, IP_B5/LWP1/VF1, IP_B6/DSDI/AT0, IP_B7/PTR/AT3, RXD1/PA15, RXD2/PA13, L1TXDB/PA11, L1RXDB/PA10, L1TXDA/PA9, L1RXDA/PA8, TIN1/L1RCLKA/BRGO1/CLK1/PA7, BRGCLK1/$\overline{\text{TOUT1}}$/CLK2/PA6, TIN2/L1TCLKA/BRGO2/CLK3/PA5, $\overline{\text{TOUT2}}$/CLK4/PA4, TIN3/BRGO3/CLK5/PA3, BRGCLK2/L1RCLKB/$\overline{\text{TOUT3}}$/CLK6/PA2, TIN4/BRGO4/CLK7/PA1, L1TCLKB/$\overline{\text{TOUT4}}$/CLK8/PA0, $\overline{\text{REJCT1}}$/$\overline{\text{SPISEL}}$/PB31, SPICLK/PB30,SPIMOSI/PB29, BRGO4/SPIMISO/PB28, BRGO1/I2CSDA/PB27, BRGO2/I2CSCL/PB26, SMTXD1/PB25, SMRXD1/PB24, $\overline{\text{SMSYN1}}$/$\overline{\text{SDACK1}}$/PB23, $\overline{\text{SMSYN2}}$/$\overline{\text{SDACK2}}$/PB22, SMTXD2/L1CLKOB/PB21, SMRXD2/L1CLKOA/PB20, L1ST1/$\overline{\text{RTS1}}$/PB19, L1ST2/$\overline{\text{RTS2}}$/PB18, L1ST3/$\overline{\text{L1RQB}}$/PB17, L1ST4/$\overline{\text{L1RQA}}$/PB16, BRGO3/PB15, $\overline{\text{RSTRT1}}$/PB14, L1ST1/$\overline{\text{RTS1}}$/$\overline{\text{DREQ0}}$/PC15, L1ST2/$\overline{\text{RTS2}}$/$\overline{\text{DREQ1}}$/PC14, L1ST3/$\overline{\text{L1RQB}}$/PC13, L1ST4/$\overline{\text{L1RQA}}$/PC12, $\overline{\text{CTS1}}$/PC11, $\overline{\text{TGATE1}}$/$\overline{\text{CD1}}$/PC10, $\overline{\text{CTS2}}$/PC9, $\overline{\text{TGATE2}}$/$\overline{\text{CD2}}$/PC8, $\overline{\text{SDACK2}}$/L1TSYNCB/PC7, L1RSYNCB/PC6, $\overline{\text{SDACK1}}$/L1TSYNCA/PC5, L1RSYNCA/PC4, PD15, PD14, PD13, PD12, PD11, PD10, PD9, PD8, PD5, PD6, PD7, PD4, PD3, MII_MDC, MII_TX_ER, MII_EN, MII_MDIO, and MII_TXD[0:3]

4 $\overline{\text{BDIP}}$/$\overline{\text{GPL_B}}$(5), $\overline{\text{BR}}$, $\overline{\text{BG}}$, FRZ/$\overline{\text{IRQ6}}$, $\overline{\text{CS}}$(0:5), $\overline{\text{CS}}$(6)/$\overline{\text{CE}}$(1)_B, $\overline{\text{CS}}$(7)/$\overline{\text{CE}}$(2)_B, $\overline{\text{WE0}}$/$\overline{\text{BS_B0}}$/$\overline{\text{IORD}}$, $\overline{\text{WE1}}$/$\overline{\text{BS_B1}}$/$\overline{\text{IOWR}}$, $\overline{\text{WE2}}$/$\overline{\text{BS_B2}}$/$\overline{\text{PCOE}}$, $\overline{\text{WE3}}$/$\overline{\text{BS_B3}}$/$\overline{\text{PCWE}}$, $\overline{\text{BS_A}}$(0:3), $\overline{\text{GPL_A0}}$/$\overline{\text{GPL_B0}}$, $\overline{\text{OE}}$/$\overline{\text{GPL_A1}}$/$\overline{\text{GPL_B1}}$, $\overline{\text{GPL_A}}$(2:3)/$\overline{\text{GPL_B}}$(2:3)/$\overline{\text{CS}}$(2:3), UPWAITA/$\overline{\text{GPL_A4}}$, UPWAITB/$\overline{\text{GPL_B4}}$, $\overline{\text{GPL_A5}}$, ALE_A, $\overline{\text{CE}}$1_A, $\overline{\text{CE}}$2_A, ALE_B/DSCK/AT1, OP(0:1), OP2/MODCK1/$\overline{\text{STS}}$, OP3/MODCK2/DSDO, and BADDR(28:30)

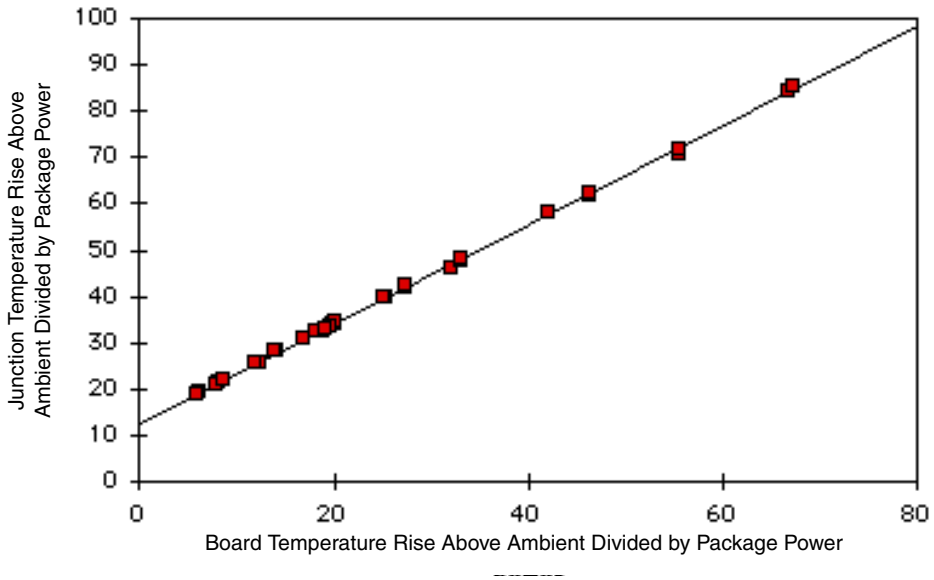

Figure 2. Effect of Board Temperature Rise on Thermal Behavior

If the board temperature is known, an estimate of the junction temperature in the environment can be made using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

$R_{\theta JB}$ = junction-to-board thermal resistance (ºC/W)

T_B = board temperature (ºC)

P_D = power dissipation in package

If the board temperature is known and the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. For this method to work, the board and board mounting must be similar to the test board used to determine the junction-to-board thermal resistance, namely a 2s2p (board with a power and a ground plane) and by attaching the thermal balls to the ground plane.

7.4 Estimation Using Simulation

When the board temperature is not known, a thermal simulation of the application is needed. The simple two-resistor model can be used with the thermal simulation of the application [2], or a more accurate and complex model of the package can be used in the thermal simulation.

7.5 Experimental Determination

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

Table 7. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B23	CLKOUT rising edge to $\overline{CS}$ negated GPCM read access, GPCM write access ACS = 00, TRLX = 0, and CSNT = 0	2.00	8.00	2.00	8.00	2.00	8.00	2.00	8.00	ns
B24	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 0	5.58	—	4.25	—	3.00	—	1.79	—	ns
B24a	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 0	13.15	—	10.50	—	8.00	—	5.58	—	ns
B25	CLKOUT rising edge to $\overline{OE}$, $\overline{WE}$(0:3) asserted	—	9.00	—	9.00	—	9.00	—	9.00	ns
B26	CLKOUT rising edge to $\overline{OE}$ negated	2.00	9.00	2.00	9.00	2.00	9.00	2.00	9.00	ns
B27	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 1	35.88	—	29.25	—	23.00	—	16.94	—	ns
B27a	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 1	43.45	—	35.50	—	28.00	—	20.73	—	ns
B28	CLKOUT rising edge to $\overline{WE}$(0:3) negated GPCM write access CSNT = 0	—	9.00	—	9.00	—	9.00	—	9.00	ns
B28a	CLKOUT falling edge to $\overline{WE}$(0:3) negated GPCM write access TRLX = 0, 1, CSNT = 1, EBDF = 0	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.54	ns
B28b	CLKOUT falling edge to $\overline{CS}$ negated GPCM write access TRLX = 0, 1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 0	—	14.33	—	13.00	—	11.75	—	10.54	ns
B28c	CLKOUT falling edge to $\overline{WE}$(0:3) negated GPCM write access TRLX = 0, 1, CSNT = 1 write access TRLX = 0, CSNT = 1, EBDF = 1	10.86	17.99	8.88	16.00	7.00	14.13	5.18	12.31	ns
B28d	CLKOUT falling edge to $\overline{CS}$ negated GPCM write access TRLX = 0, 1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 1	—	17.99	—	16.00	—	14.13	—	12.31	ns
B29	$\overline{WE}$(0:3) negated to D(0:31), DP(0:3) High-Z GPCM write access CSNT = 0, EBDF = 0	5.58	—	4.25	—	3.00	—	1.79	—	ns
B29a	$\overline{WE}$(0:3) negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 0	13.15	—	10.5	—	8.00	—	5.58	—	ns
B29b	$\overline{CS}$ negated to D(0:31), DP(0:3), High-Z GPCM write access, ACS = 00, TRLX = 0, 1, and CSNT = 0	5.58	—	4.25	—	3.00	—	1.79	—	ns
B29c	$\overline{CS}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 0	13.15	—	10.5	—	8.00	—	5.58	—	ns

Table 7. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B29d	$\overline{WE}$(0:3) negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 0	43.45	—	35.5	—	28.00	—	20.73	—	ns
B29e	$\overline{CS}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 0	43.45	—	35.5	—	28.00	—	29.73	—	ns
B29f	$\overline{WE}$(0:3) negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 1	8.86	—	6.88	—	5.00	—	3.18	—	ns
B29g	$\overline{CS}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 1	8.86	—	6.88	—	5.00	—	3.18	—	ns
B29h	$\overline{WE}$(0:3) negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 1	38.67	—	31.38	—	24.50	—	17.83	—	ns
B29i	$\overline{CS}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 1	38.67	—	31.38	—	24.50	—	17.83	—	ns
B30	$\overline{CS}$, $\overline{WE}$(0:3) negated to A(0:31), BADDR(28:30) invalid GPCM write access [8]	5.58	—	4.25	—	3.00	—	1.79	—	ns
B30a	$\overline{WE}$(0:3) negated to A(0:31), BADDR(28:30) invalid GPCM, write access, TRLX = 0, CSNT = 1, $\overline{CS}$ negated to A(0:31) invalid GPCM write access, TRLX = 0, CSNT = 1 ACS = 10, or ACS = 11, EBDF = 0	13.15	—	10.50	—	8.00	—	5.58	—	ns
B30b	$\overline{WE}$(0:3) negated to A(0:31), invalid GPCM BADDR(28:30) invalid GPCM write access, TRLX = 1, CSNT = 1. $\overline{CS}$ negated to A(0:31), Invalid GPCM, write access, TRLX = 1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 0	43.45	—	35.50	—	28.00	—	20.73	—	ns
B30c	$\overline{WE}$(0:3) negated to A(0:31), BADDR(28:30) invalid GPCM write access, TRLX = 0, CSNT = 1. $\overline{CS}$ negated to A(0:31) invalid GPCM write access, TRLX = 0, CSNT = 1, ACS = 10, ACS = 11, EBDF = 1	8.36	—	6.38	—	4.50	—	2.68	—	ns
B30d	$\overline{WE}$(0:3) negated to A(0:31), BADDR(28:30) invalid GPCM write access, TRLX = 1, CSNT =1. $\overline{CS}$ negated to A(0:31) invalid GPCM write access TRLX = 1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 1	38.67	—	31.38	—	24.50	—	17.83	—	ns
B31	CLKOUT falling edge to $\overline{CS}$ valid—as requested by control bit CST4 in the corresponding word in UPM	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns

Figure 7 provides the timing for the synchronous input signals.

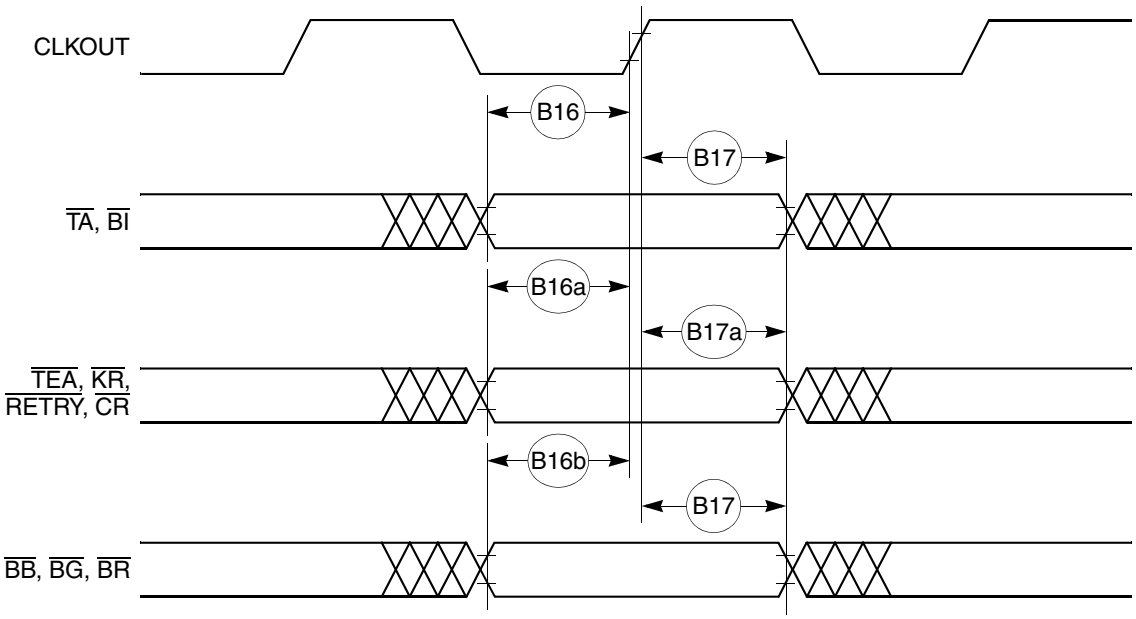

Figure 7. Synchronous Input Signals Timing

Figure 8 provides normal case timing for input data. It also applies to normal read accesses under the control of the UPM in the memory controller.

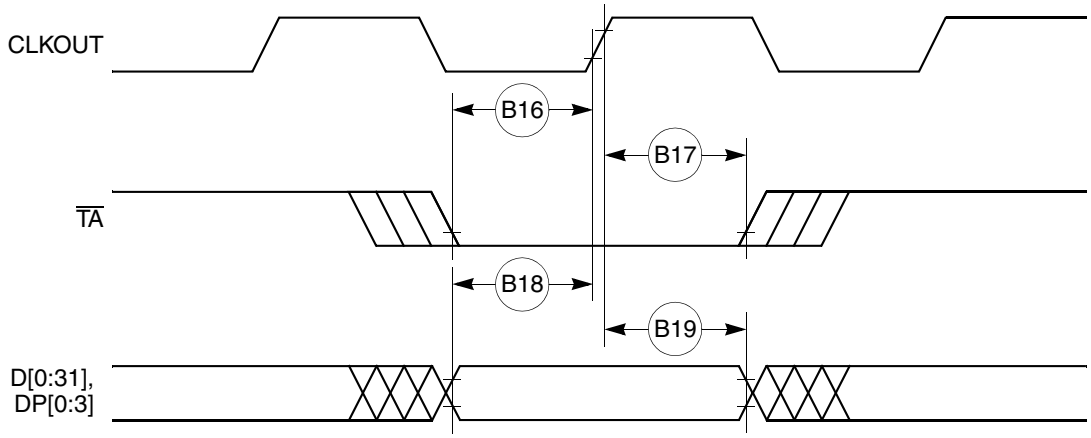

Figure 8. Input Data Timing in Normal Case

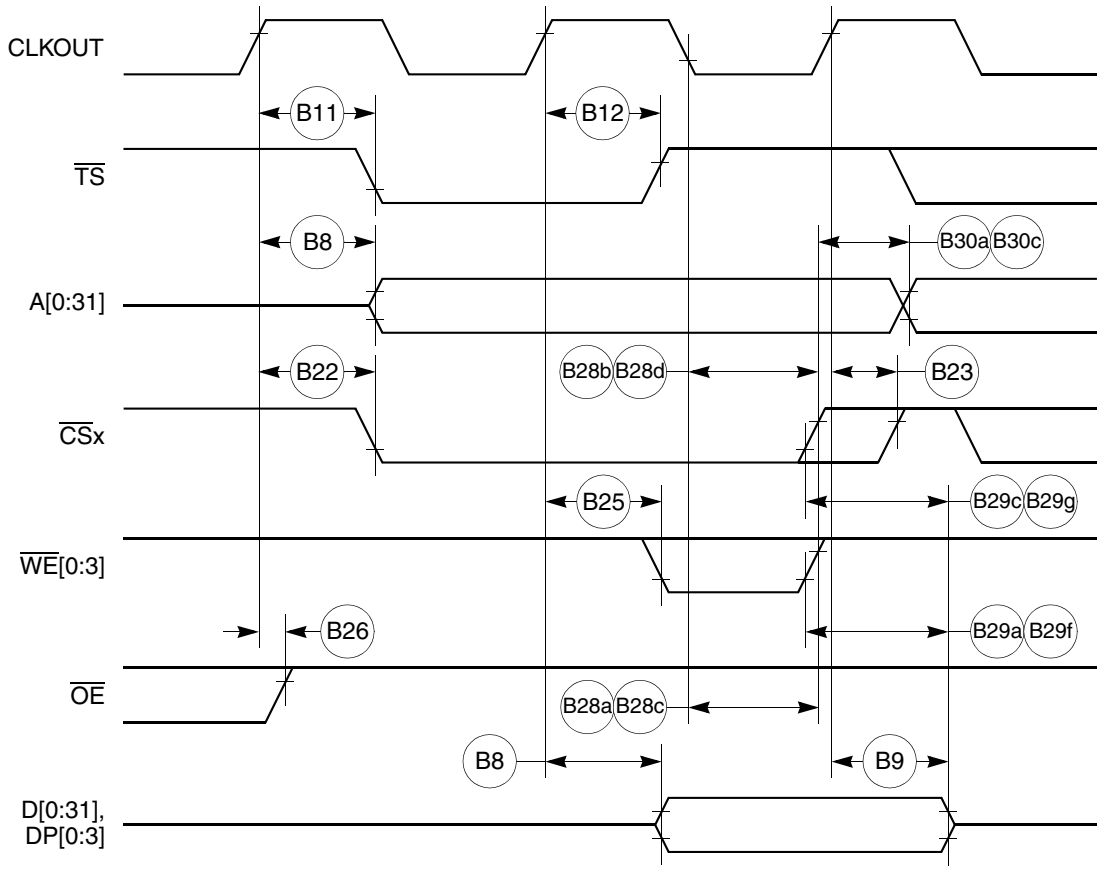

Figure 15. External Bus Write Timing (GPCM Controlled—TRLX = 0 or 1, CSNT = 1)

Figure 17 provides the timing for the external bus controlled by the UPM.

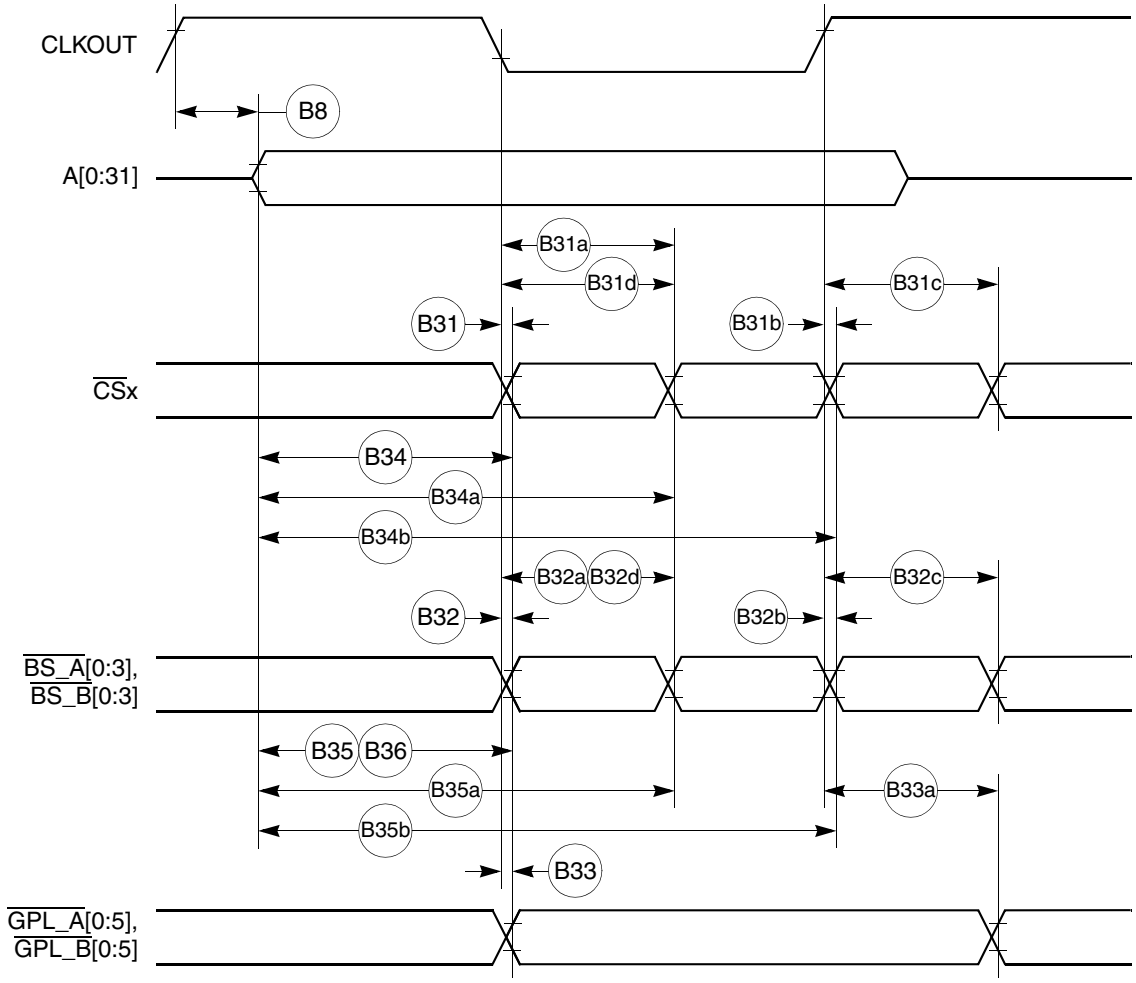

Figure 17. External Bus Timing (UPM Controlled Signals)

11 CPM Electrical Characteristics

This section provides the AC and DC electrical specifications for the communications processor module (CPM) of the MPC860.

11.1 PIP/PIO AC Electrical Specifications

Table 14 provides the PIP/PIO AC timings as shown in Figure 39 through Figure 43.

Table 14. PIP/PIO Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
21	Data-in setup time to STBI low	0	—	ns
22	Data-in hold time to STBI high	2.5 – t3[1]	—	CLK
23	STBI pulse width	1.5	—	CLK
24	STBO pulse width	1 CLK – 5 ns	—	ns
25	Data-out setup time to STBO low	2	—	CLK
26	Data-out hold time from STBO high	5	—	CLK
27	STBI low to STBO low (Rx interlock)	—	2	CLK
28	STBI low to STBO high (Tx interlock)	2	—	CLK
29	Data-in setup time to clock high	15	—	ns
30	Data-in hold time from clock high	7.5	—	ns
31	Clock low to data-out valid (CPU writes data, control, or direction)	—	25	ns

[1] t3 = Specification 23.

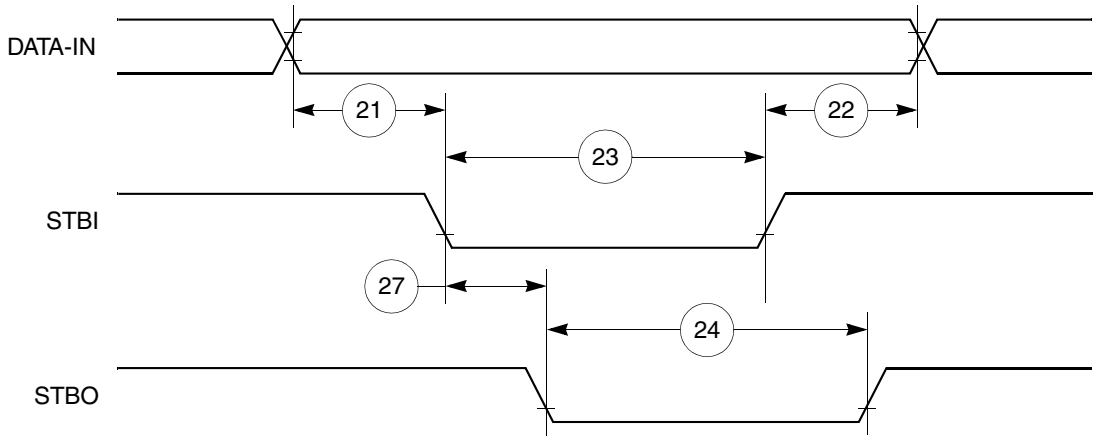

Figure 39. PIP Rx (Interlock Mode) Timing Diagram

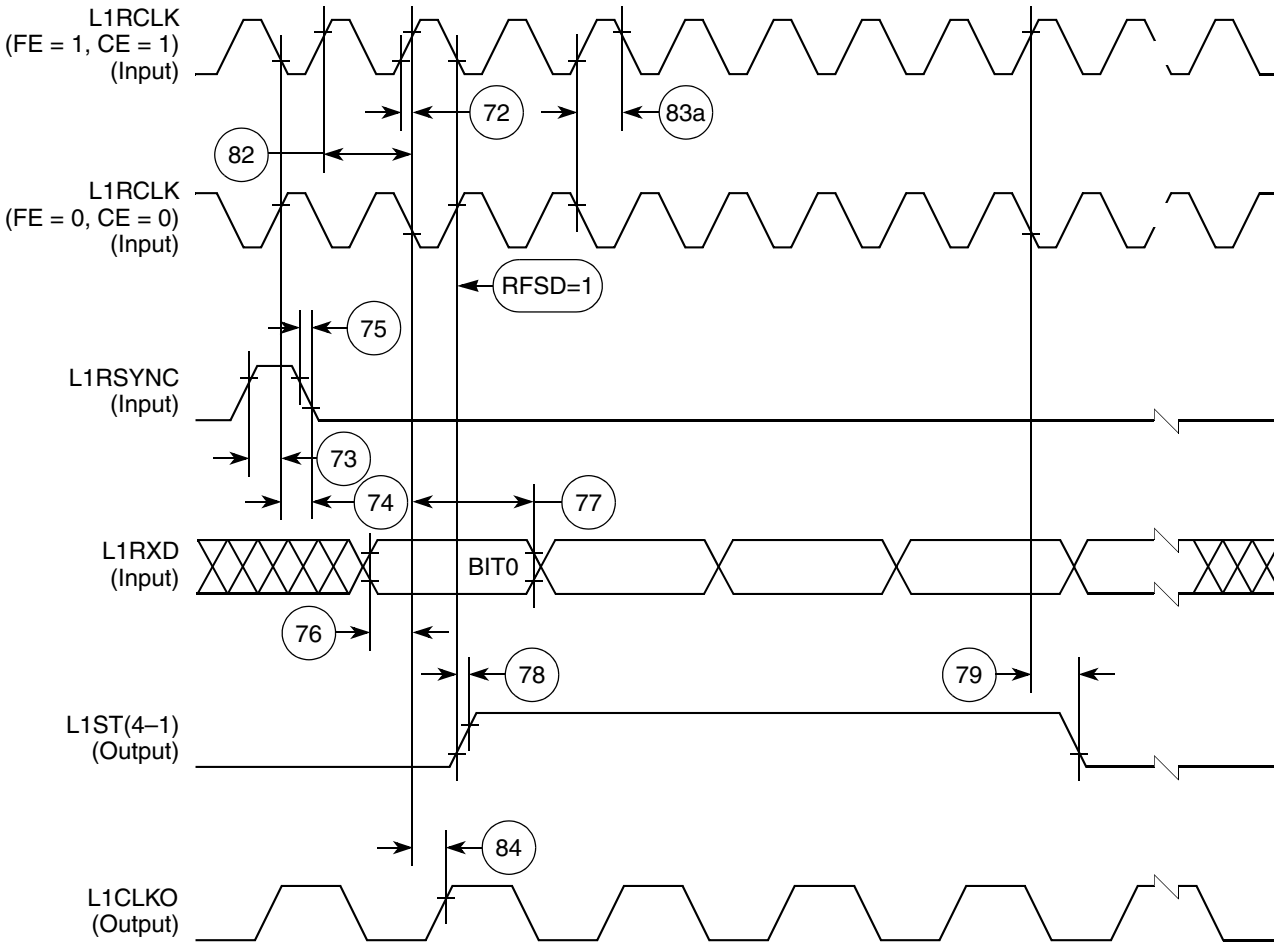

Figure 52. SI Receive Timing with Double-Speed Clocking (DSC = 1)

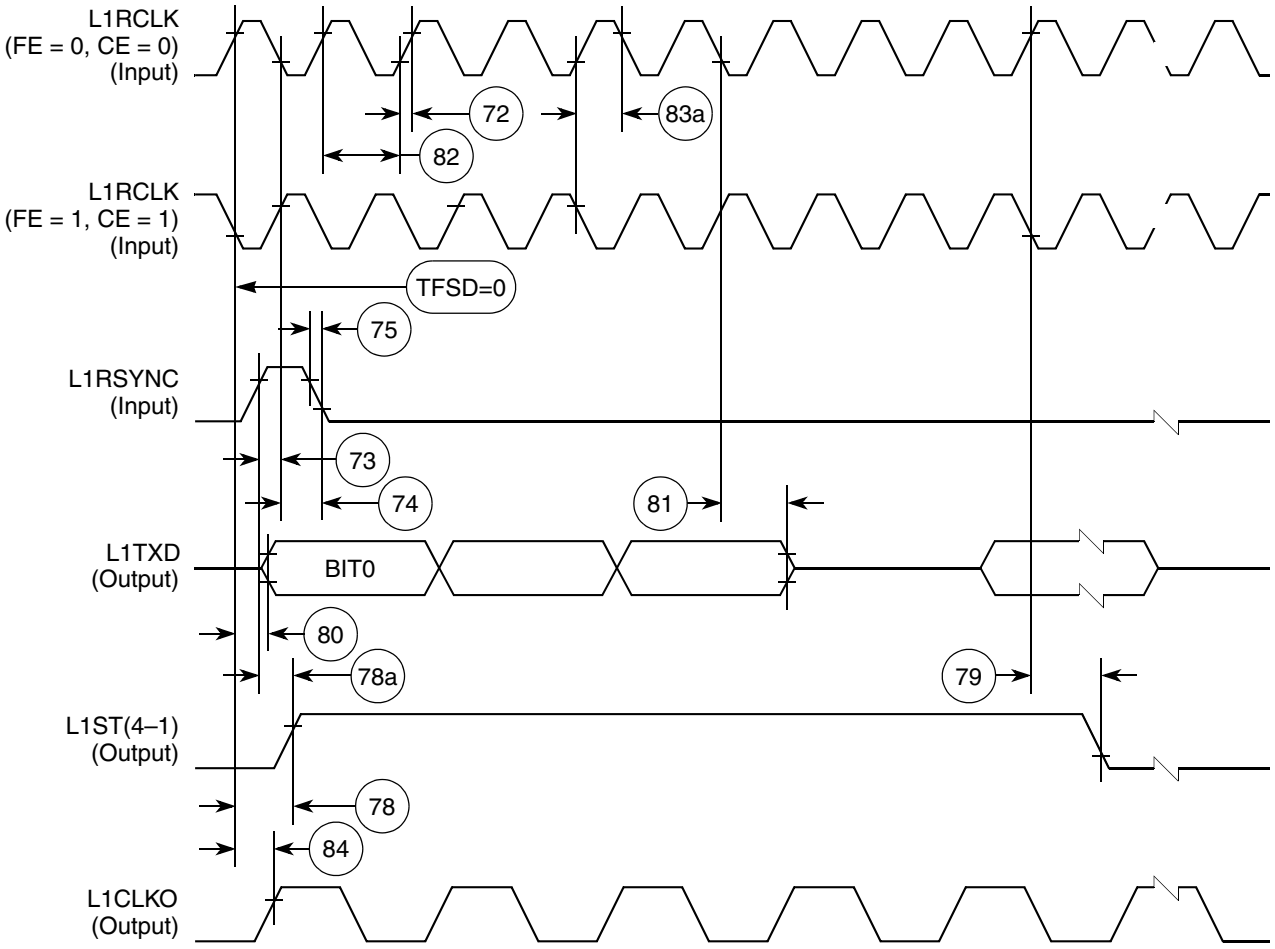

Figure 54. SI Transmit Timing with Double Speed Clocking (DSC = 1)

11.7 SCC in NMSI Mode Electrical Specifications

Table 20 provides the NMSI external clock timing.

Table 20. NMSI External Clock Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
100	RCLK1 and TCLK1 width high[1]	1/SYNCCLK	—	ns
101	RCLK1 and TCLK1 width low	1/SYNCCLK + 5	—	ns
102	RCLK1 and TCLK1 rise/fall time	—	15.00	ns
103	TXD1 active delay (from TCLK1 falling edge)	0.00	50.00	ns
104	$\overline{\text{RTS1}}$ active/inactive delay (from TCLK1 falling edge)	0.00	50.00	ns
105	$\overline{\text{CTS1}}$ setup time to TCLK1 rising edge	5.00	—	ns
106	RXD1 setup time to RCLK1 rising edge	5.00	—	ns
107	RXD1 hold time from RCLK1 rising edge[2]	5.00	—	ns
108	$\overline{\text{CD1}}$ setup Time to RCLK1 rising edge	5.00	—	ns

1 The ratios SYNCCLK/RCLK1 and SYNCCLK/TCLK1 must be greater than or equal to 2.25/1.
2 Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as external sync signals.

Table 21 provides the NMSI internal clock timing.

Table 21. NMSI Internal Clock Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
100	RCLK1 and TCLK1 frequency[1]	0.00	SYNCCLK/3	MHz
102	RCLK1 and TCLK1 rise/fall time	—	—	ns
103	TXD1 active delay (from TCLK1 falling edge)	0.00	30.00	ns
104	$\overline{\text{RTS1}}$ active/inactive delay (from TCLK1 falling edge)	0.00	30.00	ns
105	$\overline{\text{CTS1}}$ setup time to TCLK1 rising edge	40.00	—	ns
106	RXD1 setup time to RCLK1 rising edge	40.00	—	ns
107	RXD1 hold time from RCLK1 rising edge[2]	0.00	—	ns
108	$\overline{\text{CD1}}$ setup time to RCLK1 rising edge	40.00	—	ns

1 The ratios SYNCCLK/RCLK1 and SYNCCLK/TCLK1 must be greater than or equal to 3/1.
2 Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as external sync signals.

11.10 SPI Master AC Electrical Specifications

Table 24 provides the SPI master timings as shown in Figure 65 and Figure 66.

Table 24. SPI Master Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
160	MASTER cycle time	4	1024	t_{cyc}
161	MASTER clock (SCK) high or low time	2	512	t_{cyc}
162	MASTER data setup time (inputs)	50	—	ns
163	Master data hold time (inputs)	0	—	ns
164	Master data valid (after SCK edge)	—	20	ns
165	Master data hold time (outputs)	0	—	ns
166	Rise time output	—	15	ns
167	Fall time output	—	15	ns

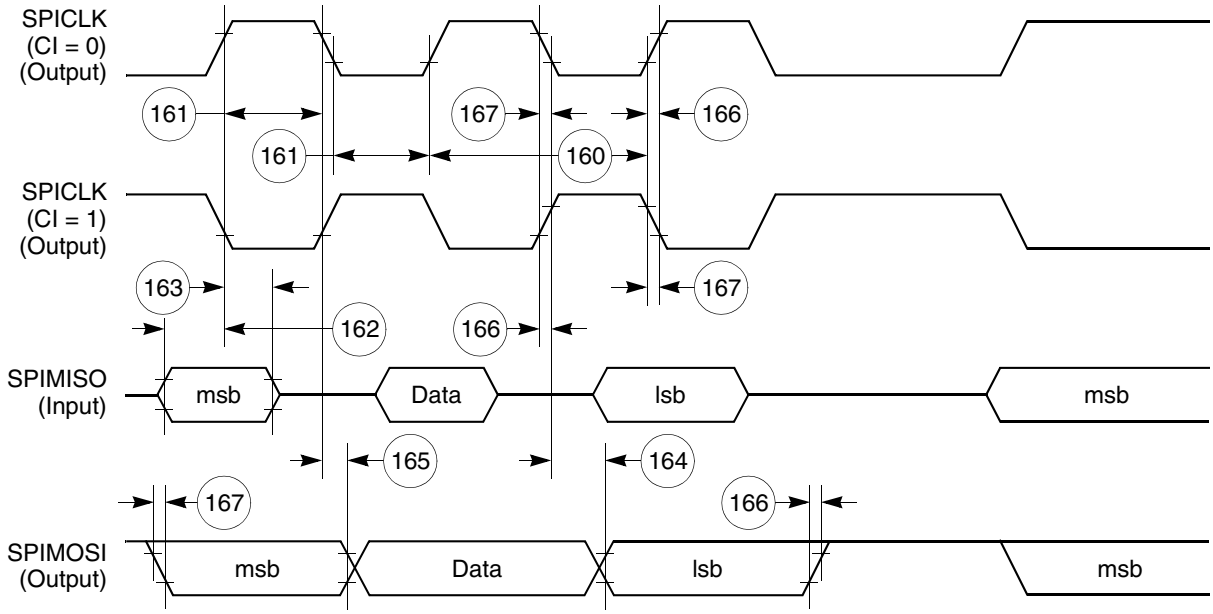

Figure 65. SPI Master (CP = 0) Timing Diagram

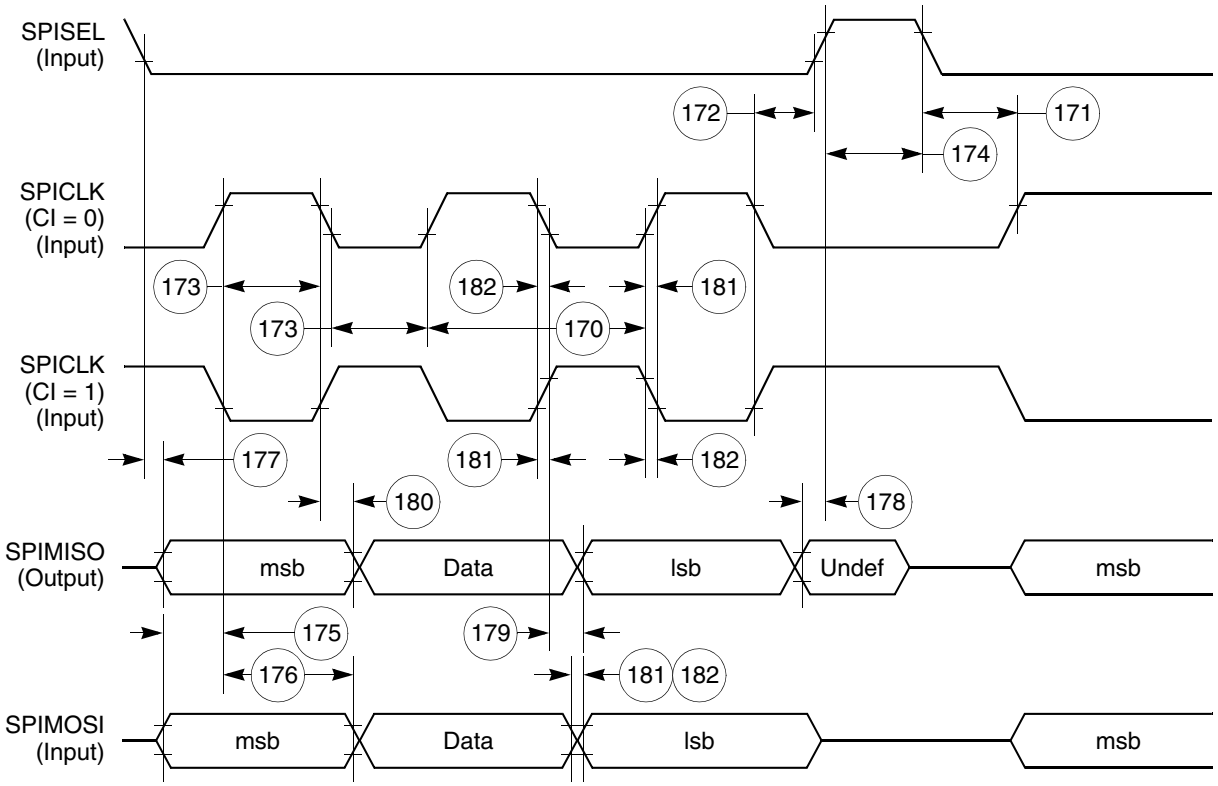

Figure 67. SPI Slave (CP = 0) Timing Diagram

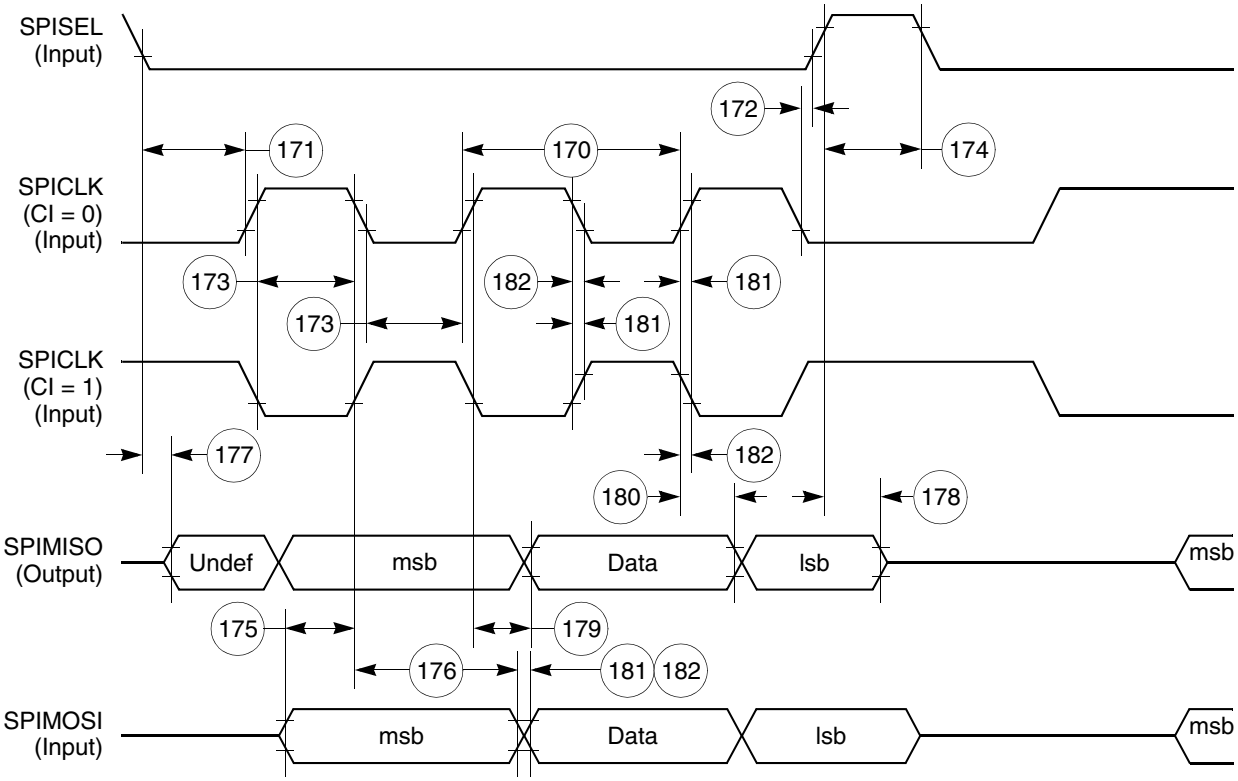

Figure 68. SPI Slave (CP = 1) Timing Diagram

11.12 I²C AC Electrical Specifications

Table 26 provides the I²C (SCL < 100 kHz) timings.

Table 26. I²C Timing (SCL < 100 kHz)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
200	SCL clock frequency (slave)	0	100	kHz
200	SCL clock frequency (master)[1]	1.5	100	kHz
202	Bus free time between transmissions	4.7	—	µs
203	Low period of SCL	4.7	—	µs
204	High period of SCL	4.0	—	µs
205	Start condition setup time	4.7	—	µs
206	Start condition hold time	4.0	—	µs
207	Data hold time	0	—	µs
208	Data setup time	250	—	ns
209	SDL/SCL rise time	—	1	µs
210	SDL/SCL fall time	—	300	ns
211	Stop condition setup time	4.7	—	µs

1 SCL frequency is given by SCL = BRGCLK_frequency / ((BRG register + 3 × pre_scaler × 2).
The ratio SYNCCLK/(BRGCLK/pre_scaler) must be greater than or equal to 4/1.

Table 27 provides the I²C (SCL > 100 kHz) timings.

Table 27. . I²C Timing (SCL > 100 kHz)

Num	Characteristic	Expression	All Frequencies		Unit
			Min	Max	
200	SCL clock frequency (slave)	fSCL	0	BRGCLK/48	Hz
200	SCL clock frequency (master)[1]	fSCL	BRGCLK/16512	BRGCLK/48	Hz
202	Bus free time between transmissions		1/(2.2 * fSCL)	—	s
203	Low period of SCL		1/(2.2 * fSCL)	—	s
204	High period of SCL		1/(2.2 * fSCL)	—	s
205	Start condition setup time		1/(2.2 * fSCL)	—	s
206	Start condition hold time		1/(2.2 * fSCL)	—	s
207	Data hold time		0	—	s
208	Data setup time		1/(40 * fSCL)	—	s
209	SDL/SCL rise time		—	1/(10 * fSCL)	s
210	SDL/SCL fall time		—	1/(33 * fSCL)	s
211	Stop condition setup time		1/2(2.2 * fSCL)	—	s

1 SCL frequency is given by SCL = BRGCLK_frequency / ((BRG register + 3) × pre_scaler × 2).
The ratio SYNCCLK/(BRGCLK / pre_scaler) must be greater than or equal to 4/1.

13 FEC Electrical Characteristics

This section provides the AC electrical specifications for the Fast Ethernet controller (FEC). Note that the timing specifications for the MII signals are independent of system clock frequency (part speed designation). Also, MII signals use TTL signal levels compatible with devices operating at either 5.0 V or 3.3 V.

13.1 MII Receive Signal Timing (MII_RXD[3:0], MII_RX_DV, MII_RX_ER, MII_RX_CLK)

The receiver functions correctly up to a MII_RX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed the MII_RX_CLK frequency – 1%.

Table 29 provides information on the MII receive signal timing.

Table 29. MII Receive Signal Timing

Num	Characteristic	Min	Max	Unit
M1	MII_RXD[3:0], MII_RX_DV, MII_RX_ER to MII_RX_CLK setup	5	—	ns
M2	MII_RX_CLK to MII_RXD[3:0], MII_RX_DV, MII_RX_ER hold	5	—	ns
M3	MII_RX_CLK pulse width high	35%	65%	MII_RX_CLK period
M4	MII_RX_CLK pulse width low	35%	65%	MII_RX_CLK period

Figure 72 shows MII receive signal timing.

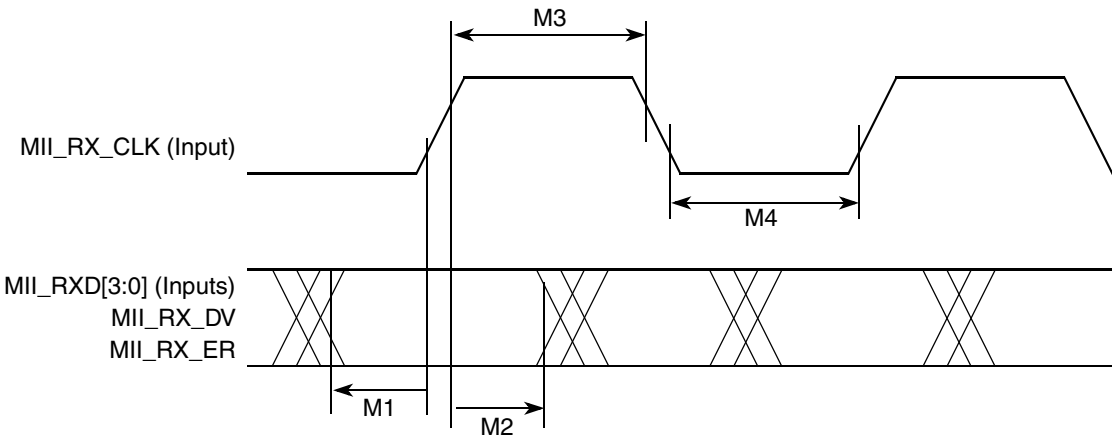

Figure 72. MII Receive Signal Timing Diagram

Table 34 identifies the packages and operating frequencies available for the MPC860.

Table 34. MPC860 Family Package/Frequency Availability

Package Type	Freq. (MHz) / Temp. (Tj)	Package	Order Number
Ball grid array ZP suffix—leaded ZQ suffix—leaded VR suffix—lead-free	50 0° to 95°C	ZP/ZQ[1]	MPC855TZQ50D4 MPC860DEZQ50D4 MPC860DTZQ50D4 MPC860ENZQ50D4 MPC860SRZQ50D4 MPC860TZQ50D4 MPC860DPZQ50D4 MPC860PZQ50D4
		Tape and Reel	MPC855TZQ50D4R2 MPC860DEZQ50D4R2 MPC860ENZQ50D4R2 MPC860SRZQ50D4R2 MPC860TZQ50D4R2 MPC860DPZQ50D4R2 MPC855TVR50D4R2 MPC860ENVR50D4R2 MPC860SRVR50D4R2 MPC860TVR50D4R2
		VR	MPC855TVR50D4 MPC860DEVR50D4 MPC860DPVR50D4 MPC860DTVR50D4 MPC860ENVR50D4 MPC860PVR50D4 MPC860SRVR50D4 MPC860TVR50D4
	66 0° to 95°C	ZP/ZQ[1]	MPC855TZQ66D4 MPC860DEZQ66D4 MPC860DTZQ66D4 MPC860ENZQ66D4 MPC860SRZQ66D4 MPC860TZQ66D4 MPC860DPZQ66D4 MPC860PZQ66D4
		Tape and Reel	MPC860SRZQ66D4R2 MPC860PZQ66D4R2
		VR	MPC855TVR66D4 MPC860DEVR66D4 MPC860DPVR66D4 MPC860DTVR66D4 MPC860ENVR66D4 MPC860PVR66D4 MPC860SRVR66D4 MPC860TVR66D4

15 Document Revision History

Table 35 lists significant changes between revisions of this hardware specification.

Table 35. Document Revision History

Revision	Date	Changes
10	09/2015	In Table 34, moved MPC855TCVR50D4 and MPC855TCVR66D4 under the extended temperature (–40° to 95°C) and removed MC860ENCVR50D4R2 from the normal temperature Tape and Reel.
9	10/2011	Updated orderable part numbers in Table 34, “MPC860 Family Package/Frequency Availability.”
8	08/2007	• Updated template. • On page 1, added a second paragraph. • After Table 2, inserted a new figure showing the undershoot/overshoot voltage (Figure 1) and renumbered the rest of the figures. • In Figure 3, changed all reference voltage measurement points from 0.2 and 0.8 V to 50% level. • In Table 16, changed num 46 description to read, “$\overline{TA}$ assertion to rising edge ...” • In Figure 46, changed $\overline{TA}$ to reflect the rising edge of the clock.
7.0	9/2004	• Added a tablefootnote to Table 6 DC Electrical Specifications about meeting the VIL Max of the I2C Standard • Replaced the thermal characteristics in Table 4 by the ZQ package • Add the new parts to the Ordering and Availablity Chart in Table 34 • Added the mechanical spec of the ZQ package in Figure 78 • Removed all of the old revisions from Table 5
6.3	9/2003	• Added Section 11.2 on the Port C interrupt pins • Nontechnical reformatting
6.2	8/2003	• Changed B28a through B28d and B29d to show that TRLX can be 0 or 1 • Changed reference documentation to reflect the Rev 2 MPC860 PowerQUICC Family Users Manual • Nontechnical reformatting
6.1	11/2002	• Corrected UTOPIA RXenb* and TXenb* timing values • Changed incorrect usage of Vcc to Vdd • Corrected dual port RAM to 8 Kbytes
6	10/2002	• Added the MPC855T. Corrected Figure 26 on page -36.
5.1	11/2001	• Revised template format, removed references to MAC functionality, changed Table 7 B23 max value @ 66 MHz from 2ns to 8ns, added this revision history table