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Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	50MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (2), 10/100Mbps (1)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 95°C (TA)
Security Features	-
Package / Case	357-BBGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc860dtczq50d4

2 Features

The following list summarizes the key MPC860 features:

- Embedded single-issue, 32-bit core (implementing the Power Architecture technology) with thirty-two 32-bit general-purpose registers (GPRs)
 - The core performs branch prediction with conditional prefetch without conditional execution.
 - 4- or 8-Kbyte data cache and 4- or 16-Kbyte instruction cache (see [Table 1](#))
 - 16-Kbyte instruction caches are four-way, set-associative with 256 sets; 4-Kbyte instruction caches are two-way, set-associative with 128 sets.
 - 8-Kbyte data caches are two-way, set-associative with 256 sets; 4-Kbyte data caches are two-way, set-associative with 128 sets.
 - Cache coherency for both instruction and data caches is maintained on 128-bit (4-word) cache blocks.
 - Caches are physically addressed, implement a least recently used (LRU) replacement algorithm, and are lockable on a cache block basis.
 - MMUs with 32-entry TLB, fully-associative instruction, and data TLBs
 - MMUs support multiple page sizes of 4-, 16-, and 512-Kbytes, and 8-Mbytes; 16 virtual address spaces and 16 protection groups
 - Advanced on-chip-emulation debug mode
- Up to 32-bit data bus (dynamic bus sizing for 8, 16, and 32 bits)
- 32 address lines
- Operates at up to 80 MHz
- Memory controller (eight banks)
 - Contains complete dynamic RAM (DRAM) controller
 - Each bank can be a chip select or $\overline{\text{RAS}}$ to support a DRAM bank.
 - Up to 15 wait states programmable per memory bank
 - Glueless interface to DRAM, SIMMS, SRAM, EPROM, Flash EPROM, and other memory devices
 - DRAM controller programmable to support most size and speed memory interfaces
 - Four $\overline{\text{CAS}}$ lines, four $\overline{\text{WE}}$ lines, and one $\overline{\text{OE}}$ line
 - Boot chip-select available at reset (options for 8-, 16-, or 32-bit memory)
 - Variable block sizes (32 Kbytes to 256 Mbytes)
 - Selectable write protection
 - On-chip bus arbitration logic
- General-purpose timers
 - Four 16-bit timers or two 32-bit timers
 - Gate mode can enable/disable counting
 - Interrupt can be masked on reference match and event capture.

3 Maximum Tolerated Ratings

This section provides the maximum tolerated voltage and temperature ranges for the MPC860. [Table 2](#) provides the maximum ratings.

This device contains circuitry protecting against damage due to high-static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or V_{DD}).

Table 2. Maximum Tolerated Ratings

(GND = 0 V)

Rating	Symbol	Value	Unit
Supply voltage ¹	V_{DDH}	-0.3 to 4.0	V
	V_{DDL}	-0.3 to 4.0	V
	KAPWR	-0.3 to 4.0	V
	V_{DDSYN}	-0.3 to 4.0	V
Input voltage ²	V_{in}	GND – 0.3 to V_{DDH}	V
Temperature ³ (standard)	$T_{A(min)}$	0	°C
	$T_{j(max)}$	95	°C
Temperature ³ (extended)	$T_{A(min)}$	-40	°C
	$T_{j(max)}$	95	°C
Storage temperature range	T_{stg}	-55 to 150	°C

¹ The power supply of the device must start its ramp from 0.0 V.

² Functional operating conditions are provided with the DC electrical specifications in [Table 6](#). Absolute maximum ratings are stress ratings only; functional operation at the maxima is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device.

Caution: All inputs that tolerate 5 V cannot be more than 2.5 V greater than the supply voltage. This restriction applies to power-up and normal operation (that is, if the MPC860 is unpowered, voltage greater than 2.5 V must not be applied to its inputs).

³ Minimum temperatures are guaranteed as ambient temperature, T_A . Maximum temperatures are guaranteed as junction temperature, T_j .

where:

Ψ_{JT} = thermal characterization parameter

T_T = thermocouple temperature on top of package

P_D = power dissipation in package

The thermal characterization parameter is measured per JEDEC JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

7.6 References

Semiconductor Equipment and Materials International (415) 964-5111
 805 East Middlefield Rd.
 Mountain View, CA 94043

MIL-SPEC and EIA/JESD (JEDEC) Specifications 800-854-7179 or
 (Available from Global Engineering Documents) 303-397-7956

JEDEC Specifications <http://www.jedec.org>

1. C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.
2. B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212–220.

8 Layout Practices

Each V_{DD} pin on the MPC860 should be provided with a low-impedance path to the board’s supply. Each GND pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on the chip. The V_{DD} power supply should be bypassed to ground using at least four 0.1 μ F-bypass capacitors located as close as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to chip V_{DD} and GND should be kept to less than half an inch per capacitor lead. A four-layer board employing two inner layers as V_{CC} and GND planes is recommended.

All output pins on the MPC860 have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized in order to minimize undershoot and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data buses. Maximum PC trace lengths of 6 inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the V_{CC} and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.

9 Bus Signal Timing

Table 7 provides the bus operation timing for the MPC860 at 33, 40, 50, and 66 MHz.

The maximum bus speed supported by the MPC860 is 66 MHz. Higher-speed parts must be operated in half-speed bus mode (for example, an MPC860 used at 80 MHz must be configured for a 40-MHz bus).

The timing for the MPC860 bus shown assumes a 50-pF load for maximum delays and a 0-pF load for minimum delays.

Table 7. Bus Operation Timings

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B1	CLKOUT period	30.30	30.30	25.00	30.30	20.00	30.30	15.15	30.30	ns
B1a	EXTCLK to CLKOUT phase skew (EXTCLK > 15 MHz and MF <= 2)	-0.90	0.90	-0.90	0.90	-0.90	0.90	-0.90	0.90	ns
B1b	EXTCLK to CLKOUT phase skew (EXTCLK > 10 MHz and MF < 10)	-2.30	2.30	-2.30	2.30	-2.30	2.30	-2.30	2.30	ns
B1c	CLKOUT phase jitter (EXTCLK > 15 MHz and MF <= 2) ¹	-0.60	0.60	-0.60	0.60	-0.60	0.60	-0.60	0.60	ns
B1d	CLKOUT phase jitter ¹	-2.00	2.00	-2.00	2.00	-2.00	2.00	-2.00	2.00	ns
B1e	CLKOUT frequency jitter (MF < 10) ¹	—	0.50	—	0.50	—	0.50	—	0.50	%
B1f	CLKOUT frequency jitter (10 < MF < 500) ¹	—	2.00	—	2.00	—	2.00	—	2.00	%
B1g	CLKOUT frequency jitter (MF > 500) ¹	—	3.00	—	3.00	—	3.00	—	3.00	%
B1h	Frequency jitter on EXTCLK ²	—	0.50	—	0.50	—	0.50	—	0.50	%
B2	CLKOUT pulse width low	12.12	—	10.00	—	8.00	—	6.06	—	ns
B3	CLKOUT width high	12.12	—	10.00	—	8.00	—	6.06	—	ns
B4	CLKOUT rise time ³	—	4.00	—	4.00	—	4.00	—	4.00	ns
B5 ³³	CLKOUT fall time ³	—	4.00	—	4.00	—	4.00	—	4.00	ns
B7	CLKOUT to A(0:31), BADDR(28:30), RD/WR, BURST, D(0:31), DP(0:3) invalid	7.58	—	6.25	—	5.00	—	3.80	—	ns
B7a	CLKOUT to TSIZ(0:1), REG, RSV, AT(0:3), BDIP, PTR invalid	7.58	—	6.25	—	5.00	—	3.80	—	ns
B7b	CLKOUT to BR, BG, FRZ, VFLS(0:1), VF(0:2) IWP(0:2), LWP(0:1), STS invalid ⁴	7.58	—	6.25	—	5.00	—	3.80	—	ns
B8	CLKOUT to A(0:31), BADDR(28:30) RD/WR, BURST, D(0:31), DP(0:3) valid	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.04	ns
B8a	CLKOUT to TSIZ(0:1), REG, RSV, AT(0:3) BDIP, PTR valid	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.04	ns
B8b	CLKOUT to BR, BG, VFLS(0:1), VF(0:2), IWP(0:2), FRZ, LWP(0:1), STS valid ⁴	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.04	ns

Table 7. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B31a	CLKOUT falling edge to \overline{CS} valid—as requested by control bit CST1 in the corresponding word in UPM	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.54	ns
B31b	CLKOUT rising edge to \overline{CS} valid—as requested by control bit CST2 in the corresponding word in UPM	1.50	8.00	1.50	8.00	1.50	8.00	1.50	8.00	ns
B31c	CLKOUT rising edge to \overline{CS} valid—as requested by control bit CST3 in the corresponding word in UPM	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.04	ns
B31d	CLKOUT falling edge to \overline{CS} valid—as requested by control bit CST1 in the corresponding word in UPM, EBDF = 1	13.26	17.99	11.28	16.00	9.40	14.13	7.58	12.31	ns
B32	CLKOUT falling edge to \overline{BS} valid—as requested by control bit BST4 in the corresponding word in UPM	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns
B32a	CLKOUT falling edge to \overline{BS} valid—as requested by control bit BST1 in the corresponding word in UPM, EBDF = 0	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.54	ns
B32b	CLKOUT rising edge to \overline{BS} valid—as requested by control bit BST2 in the corresponding word in UPM	1.50	8.00	1.50	8.00	1.50	8.00	1.50	8.00	ns
B32c	CLKOUT rising edge to \overline{BS} valid—as requested by control bit BST3 in the corresponding word in UPM	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.54	ns
B32d	CLKOUT falling edge to \overline{BS} valid—as requested by control bit BST1 in the corresponding word in UPM, EBDF = 1	13.26	17.99	11.28	16.00	9.40	14.13	7.58	12.31	ns
B33	CLKOUT falling edge to \overline{GPL} valid—as requested by control bit GxT4 in the corresponding word in UPM	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns
B33a	CLKOUT rising edge to \overline{GPL} valid—as requested by control bit GxT3 in the corresponding word in UPM	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.54	ns
B34	A(0:31), BADDR(28:30), and D(0:31) to \overline{CS} valid—as requested by control bit CST4 in the corresponding word in UPM	5.58	—	4.25	—	3.00	—	1.79	—	ns
B34a	A(0:31), BADDR(28:30), and D(0:31) to \overline{CS} valid—as requested by control bit CST1 in the corresponding word in UPM	13.15	—	10.50	—	8.00	—	5.58	—	ns
B34b	A(0:31), BADDR(28:30), and D(0:31) to \overline{CS} valid—as requested by control bit CST2 in the corresponding word in UPM	20.73	—	16.75	—	13.00	—	9.36	—	ns

Figure 9 provides the timing for the input data controlled by the UPM for data beats where $DLT3 = 1$ in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

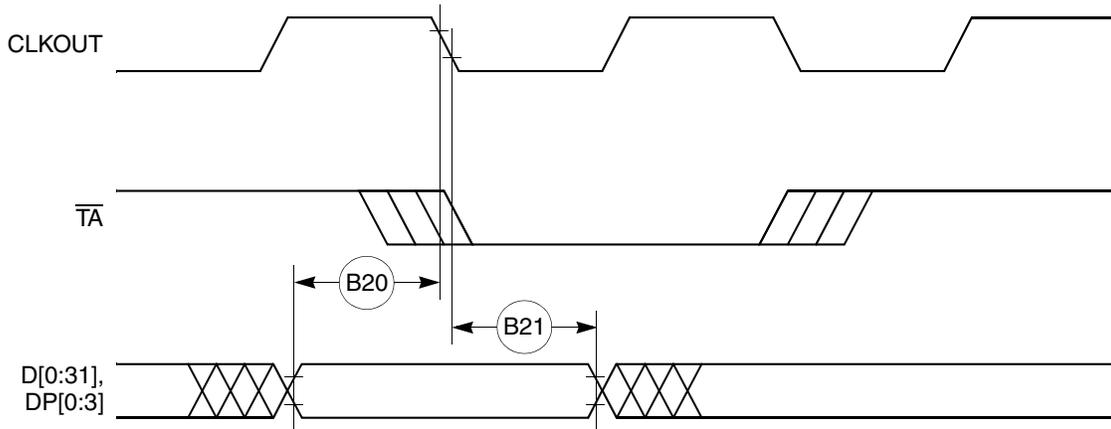


Figure 9. Input Data Timing when Controlled by UPM in the Memory Controller and $DLT3 = 1$

Figure 10 through Figure 13 provide the timing for the external bus read controlled by various GPCM factors.

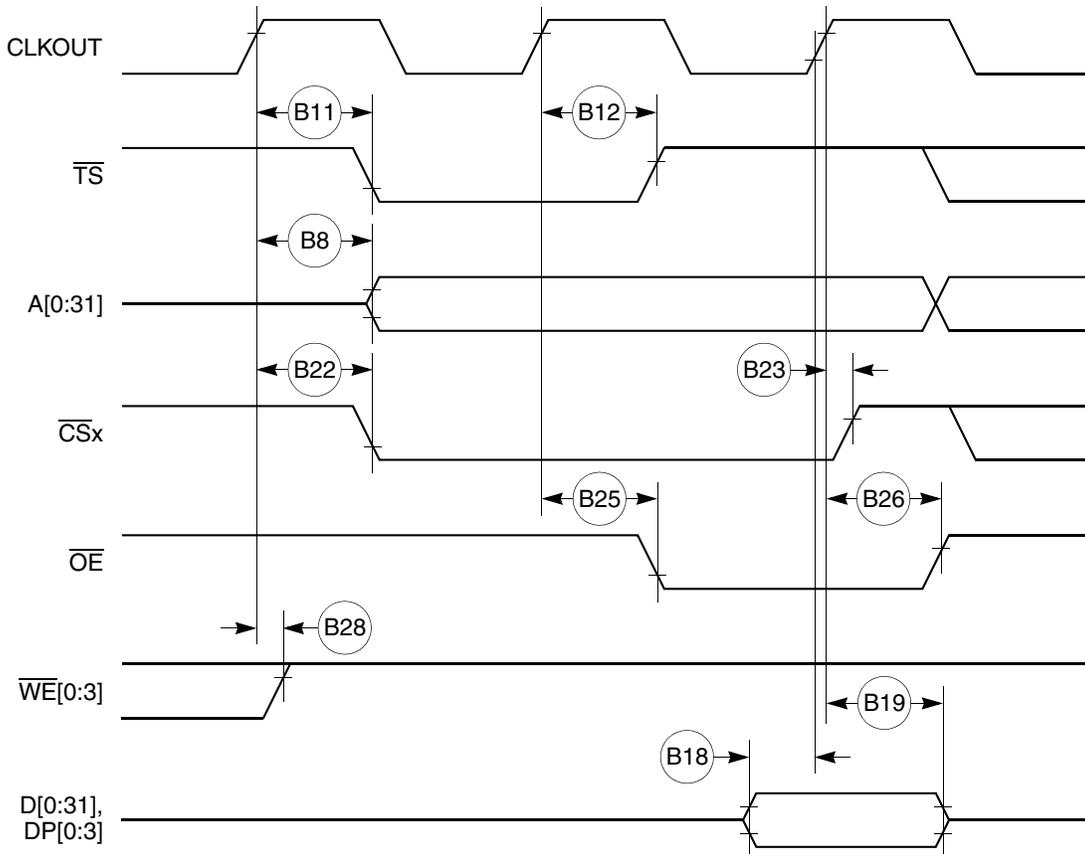


Figure 10. External Bus Read Timing (GPCM Controlled— $ACS = 00$)

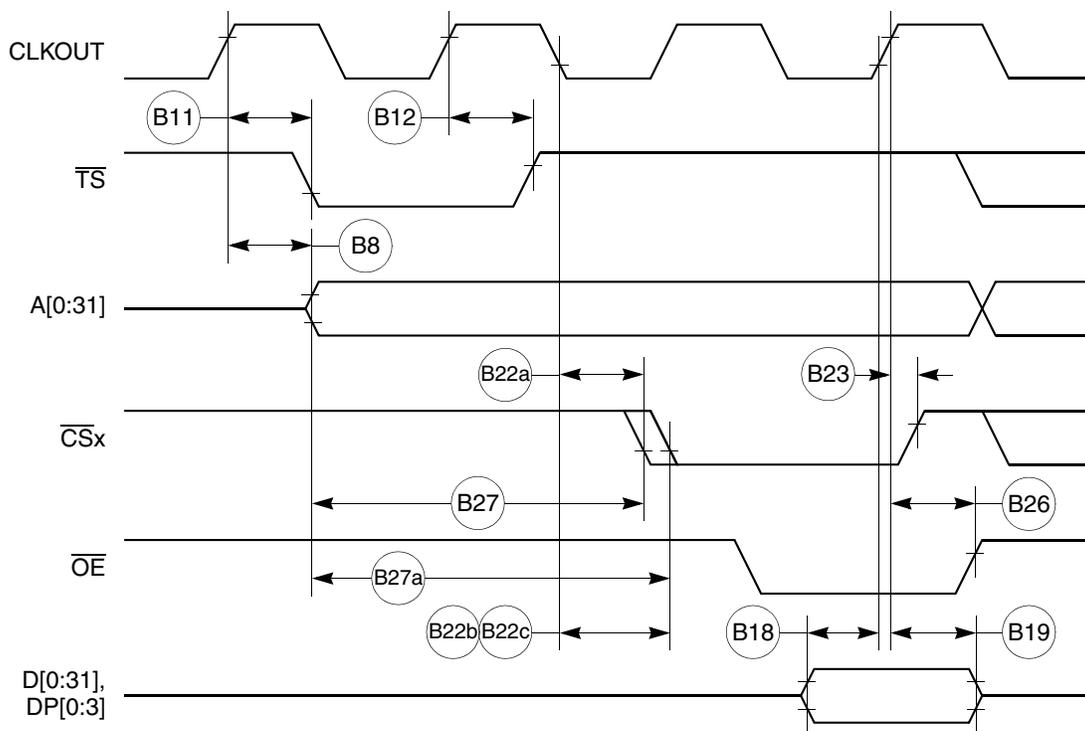


Figure 13. External Bus Read Timing (GPCM Controlled—TRLX = 0 or 1, ACS = 10, ACS = 11)

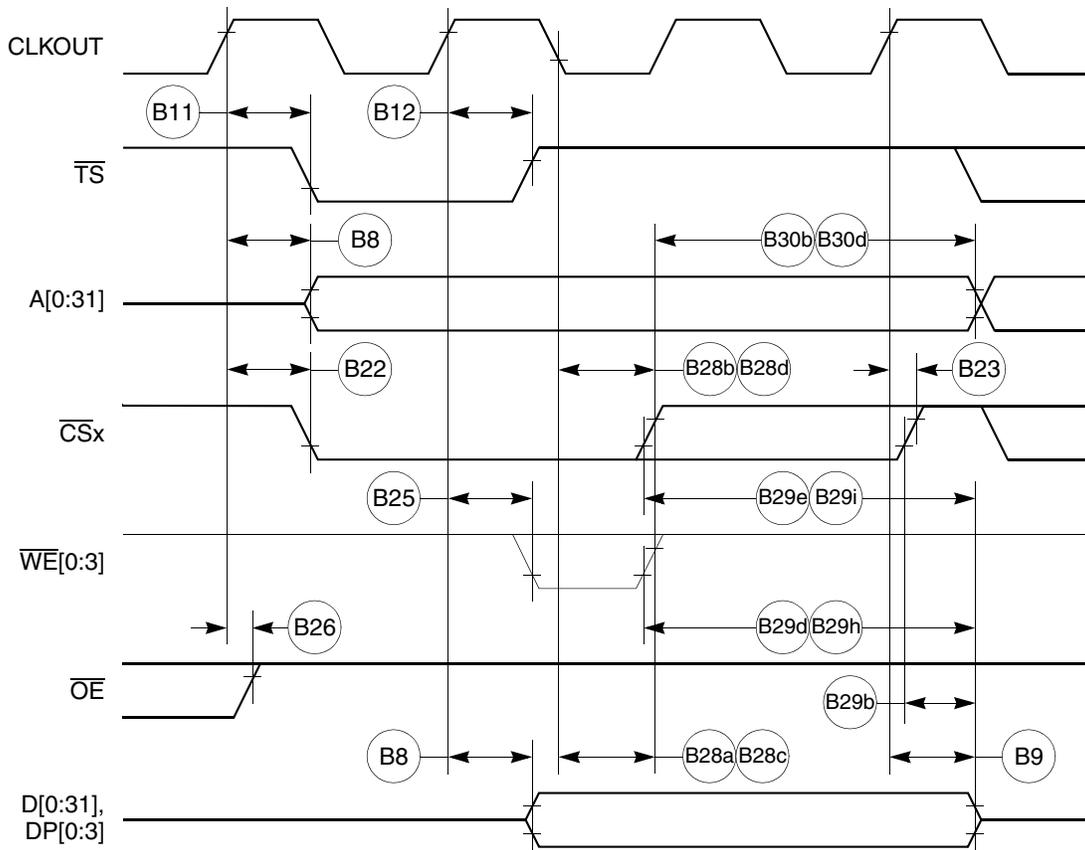


Figure 16. External Bus Write Timing (GPCM Controlled—TRLX = 0 or 1, CSNT = 1)

Figure 17 provides the timing for the external bus controlled by the UPM.

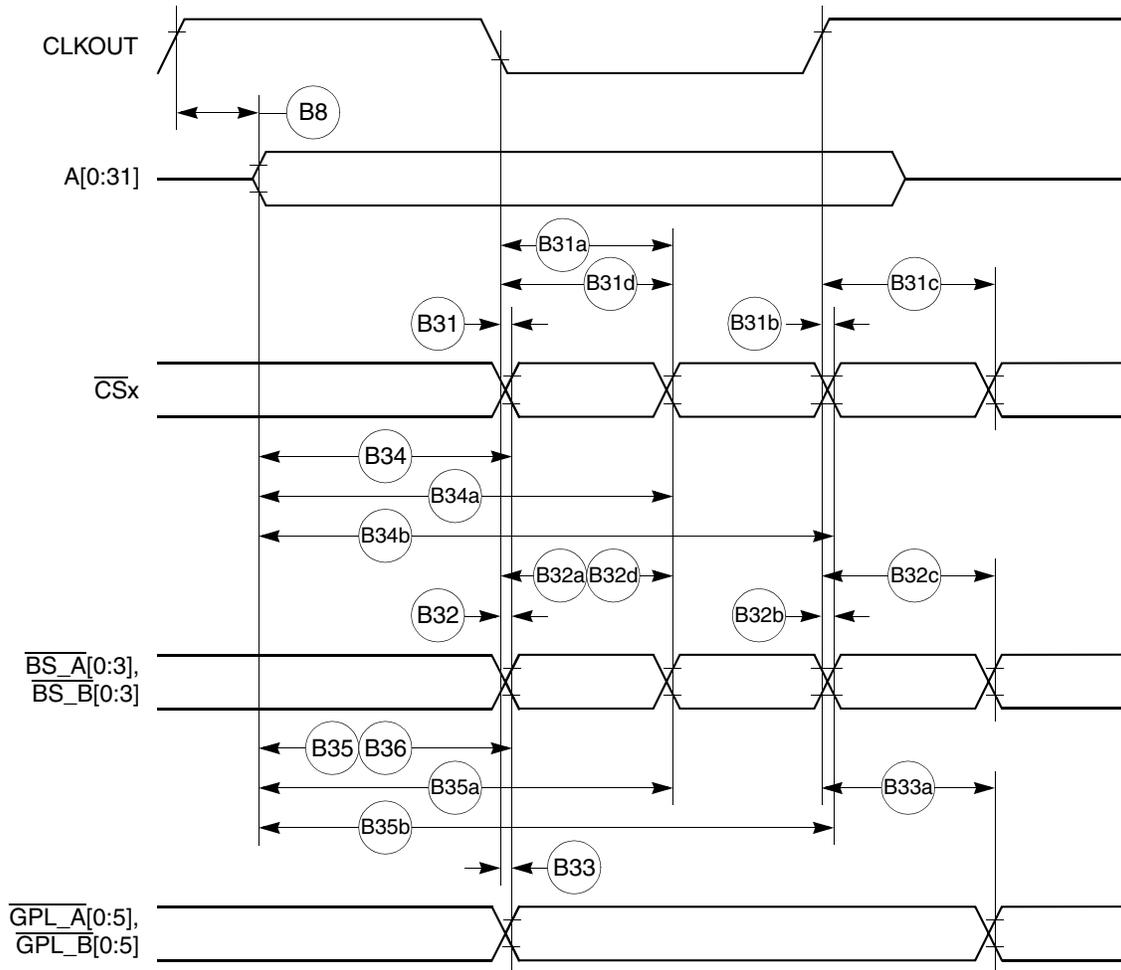


Figure 17. External Bus Timing (UPM Controlled Signals)

Table 12 shows the reset timing for the MPC860.

Table 12. Reset Timing

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
R69	CLKOUT to $\overline{\text{HRESET}}$ high impedance	—	20.00	—	20.00	—	20.00	—	20.00	ns
R70	CLKOUT to $\overline{\text{SRESET}}$ high impedance	—	20.00	—	20.00	—	20.00	—	20.00	ns
R71	$\overline{\text{RSTCONF}}$ pulse width	515.15	—	425.00	—	340.00	—	257.58	—	ns
R72	—	—	—	—	—	—	—	—	—	
R73	Configuration data to HRESET rising edge setup time	504.55	—	425.00	—	350.00	—	277.27	—	ns
R74	Configuration data to $\overline{\text{RSTCONF}}$ rising edge setup time	350.00	—	350.00	—	350.00	—	350.00	—	ns
R75	Configuration data hold time after $\overline{\text{RSTCONF}}$ negation	0.00	—	0.00	—	0.00	—	0.00	—	ns
R76	Configuration data hold time after HRESET negation	0.00	—	0.00	—	0.00	—	0.00	—	ns
R77	$\overline{\text{HRESET}}$ and $\overline{\text{RSTCONF}}$ asserted to data out drive	—	25.00	—	25.00	—	25.00	—	25.00	ns
R78	$\overline{\text{RSTCONF}}$ negated to data out high impedance	—	25.00	—	25.00	—	25.00	—	25.00	ns
R79	CLKOUT of last rising edge before chip three-state $\overline{\text{HRESET}}$ to data out high impedance	—	25.00	—	25.00	—	25.00	—	25.00	ns
R80	DSDI, DSCK setup	90.91	—	75.00	—	60.00	—	45.45	—	ns
R81	DSDI, DSCK hold time	0.00	—	0.00	—	0.00	—	0.00	—	ns
R82	$\overline{\text{SRESET}}$ negated to CLKOUT rising edge for DSDI and DSCK sample	242.42	—	200.00	—	160.00	—	121.21	—	ns

Table 16. IDMA Controller Timing (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
42	\overline{SDACK} assertion delay from clock high	—	12	ns
43	\overline{SDACK} negation delay from clock low	—	12	ns
44	\overline{SDACK} negation delay from \overline{TA} low	—	20	ns
45	\overline{SDACK} negation delay from clock high	—	15	ns
46	\overline{TA} assertion to rising edge of the clock setup time (applies to external \overline{TA})	7	—	ns

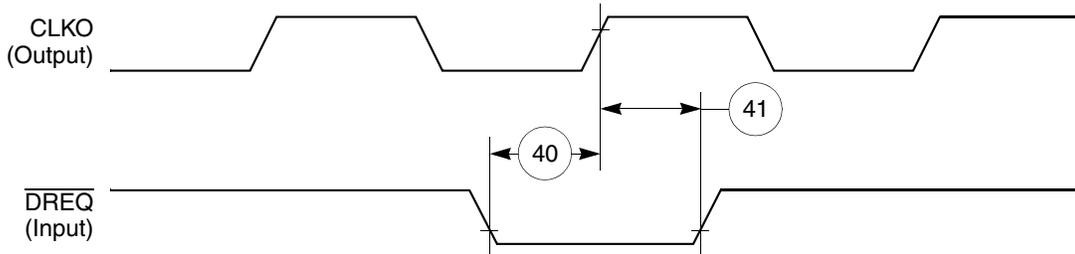


Figure 45. IDMA External Requests Timing Diagram

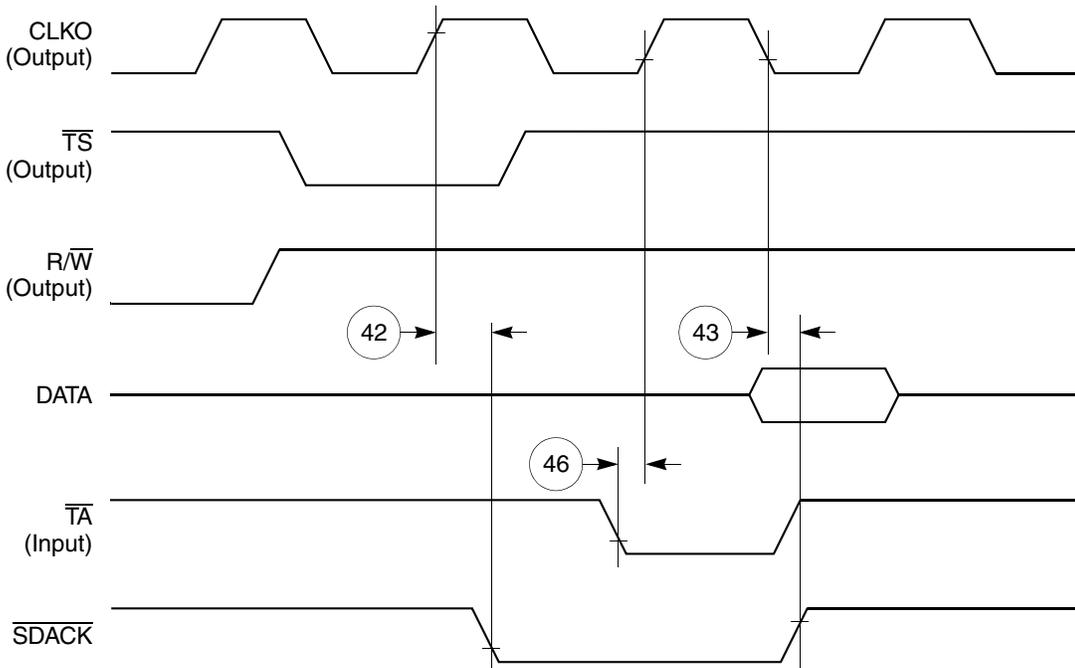


Figure 46. \overline{SDACK} Timing Diagram—Peripheral Write, Externally-Generated \overline{TA}

11.4 Baud Rate Generator AC Electrical Specifications

Table 17 provides the baud rate generator timings as shown in Figure 49.

Table 17. Baud Rate Generator Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
50	BRGO rise and fall time	—	10	ns
51	BRGO duty cycle	40	60	%
52	BRGO cycle	40	—	ns

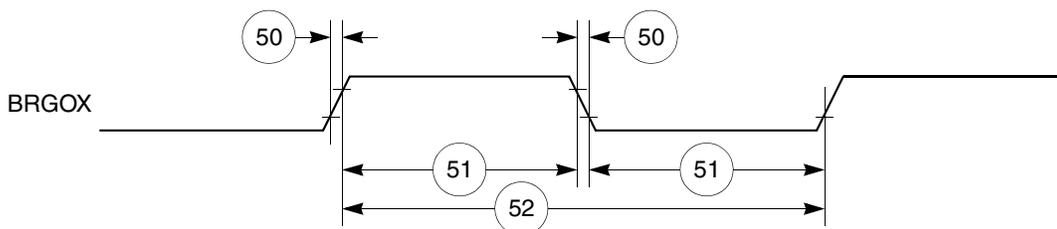


Figure 49. Baud Rate Generator Timing Diagram

11.5 Timer AC Electrical Specifications

Table 18 provides the general-purpose timer timings as shown in Figure 50.

Table 18. Timer Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
61	TIN/ $\overline{\text{TGATE}}$ rise and fall time	10	—	ns
62	TIN/ $\overline{\text{TGATE}}$ low time	1	—	CLK
63	TIN/ $\overline{\text{TGATE}}$ high time	2	—	CLK
64	TIN/ $\overline{\text{TGATE}}$ cycle time	3	—	CLK
65	CLKO low to $\overline{\text{TOUT}}$ valid	3	25	ns

Table 19. SI Timing (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
84	L1CLK edge to L1CLKO valid (DSC = 1)	—	30.00	ns
85	$\overline{L1RQ}$ valid before falling edge of L1TSYNC ⁴	1.00	—	L1TCLK
86	L1GR setup time ²	42.00	—	ns
87	L1GR hold time	42.00	—	ns
88	L1CLK edge to L1SYNC valid (FSD = 00) CNT = 0000, BYT = 0, DSC = 0)	—	0.00	ns

¹ The ratio SYNCCLK/L1RCLK must be greater than 2.5/1.

² These specs are valid for IDL mode only.

³ Where $P = 1/CLKOUT$. Thus, for a 25-MHz CLK01 rate, $P = 40$ ns.

⁴ These strobes and TxD on the first bit of the frame become valid after L1CLK edge or L1SYNC, whichever comes later.

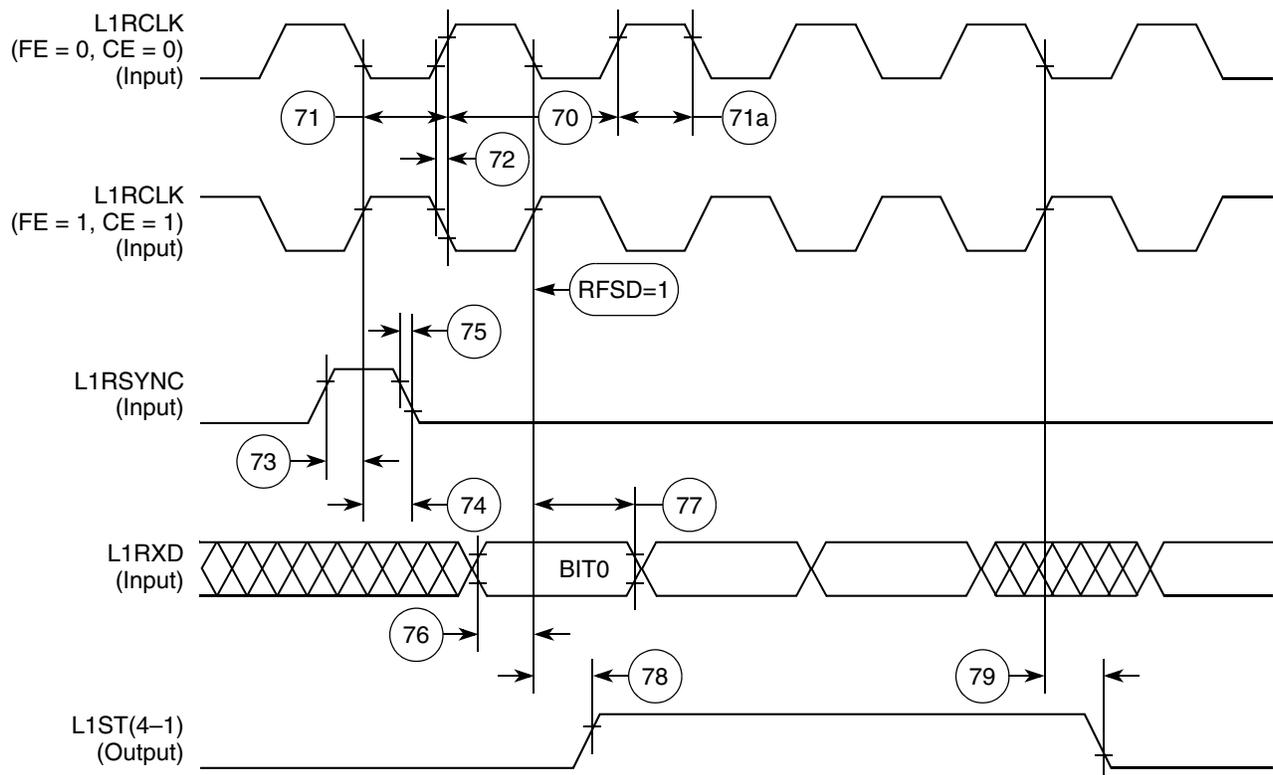


Figure 51. SI Receive Timing Diagram with Normal Clocking (DSC = 0)

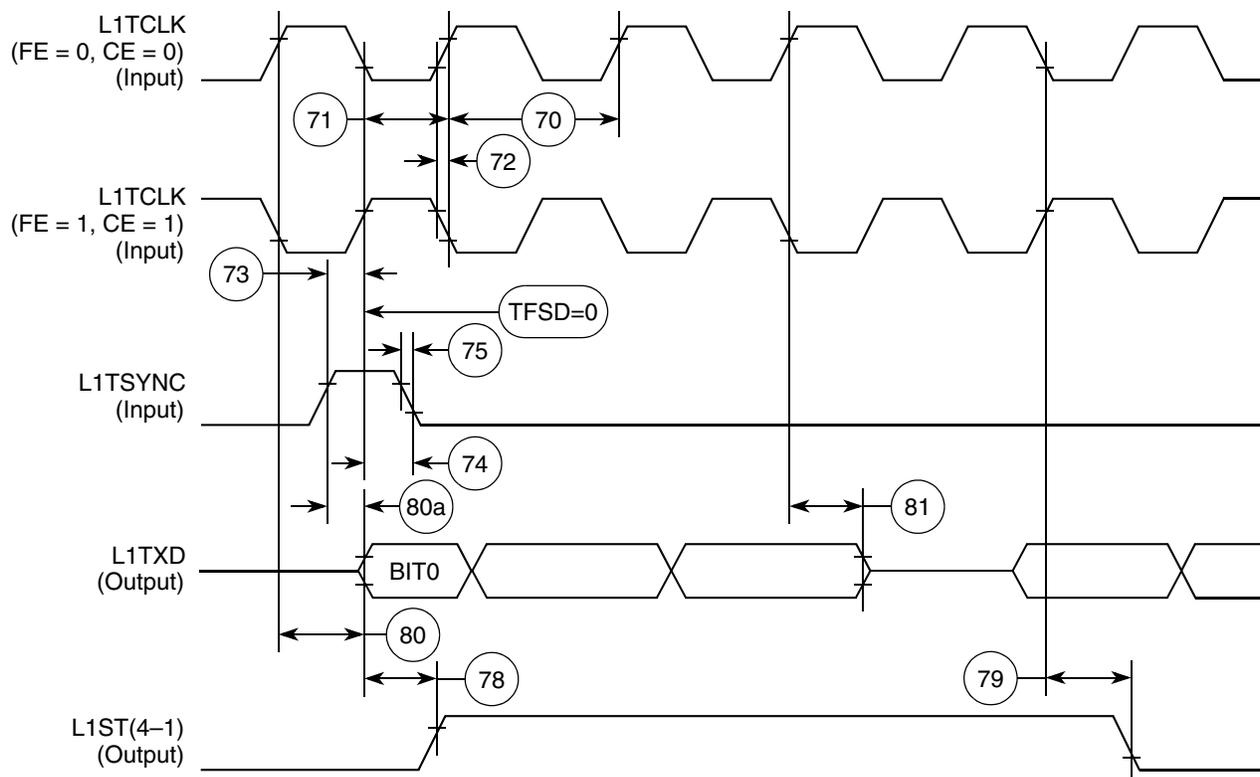


Figure 53. SI Transmit Timing Diagram (DSC = 0)

Table 22. Ethernet Timing (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
135	$\overline{\text{RSTRT}}$ active delay (from TCLK1 falling edge)	10	50	ns
136	$\overline{\text{RSTRT}}$ inactive delay (from TCLK1 falling edge)	10	50	ns
137	$\overline{\text{REJECT}}$ width low	1	—	CLK
138	CLKO1 low to $\overline{\text{SDACK}}$ asserted ²	—	20	ns
139	CLKO1 low to $\overline{\text{SDACK}}$ negated ²	—	20	ns

¹ The ratios SYNCCLK/RCLK1 and SYNCCLK/TCLK1 must be greater than or equal to 2/1.

² $\overline{\text{SDACK}}$ is asserted whenever the SDMA writes the incoming frame DA into memory.

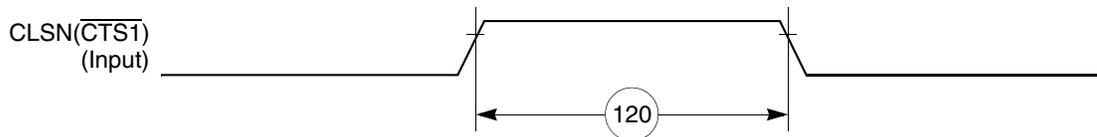


Figure 59. Ethernet Collision Timing Diagram

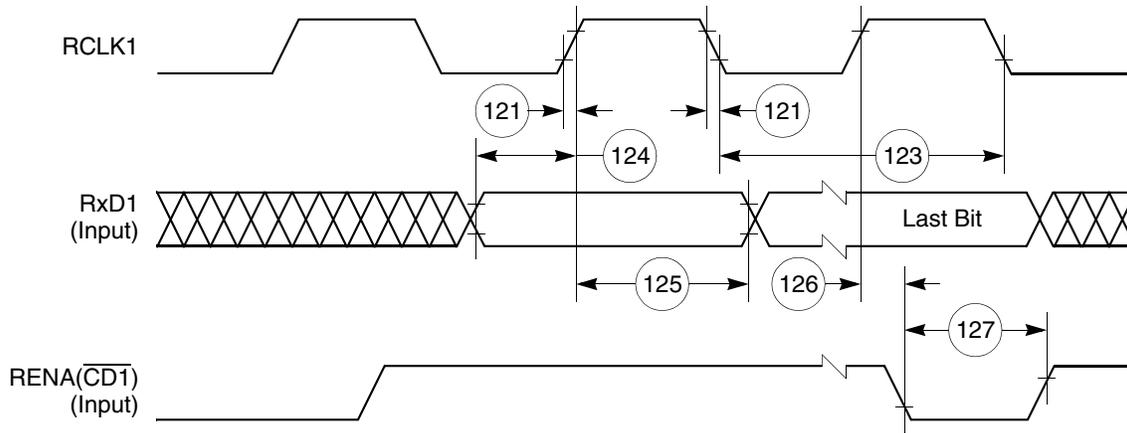
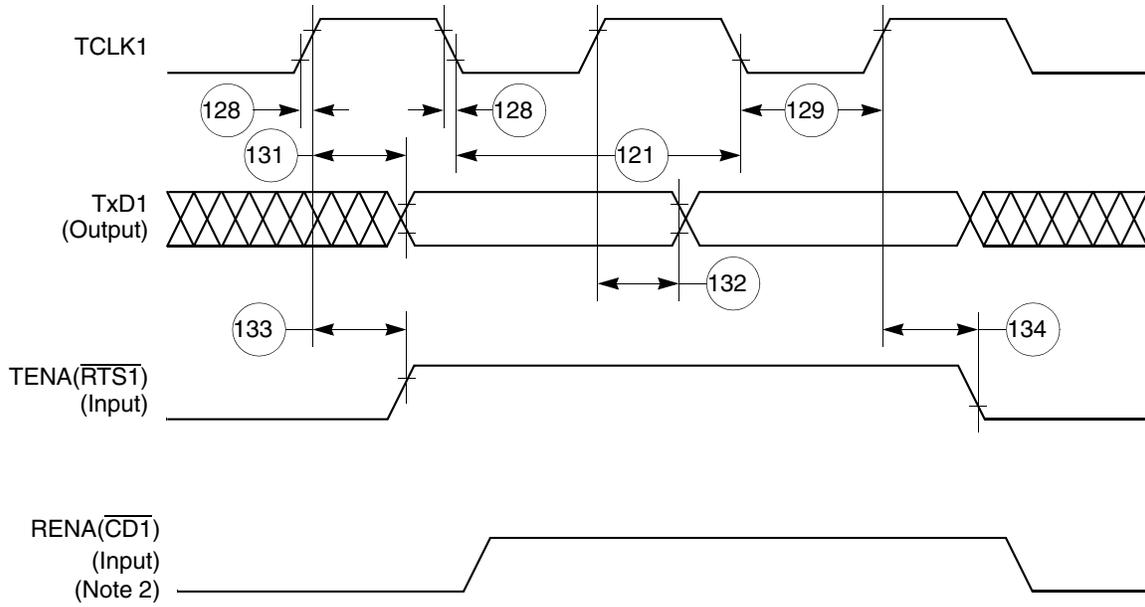


Figure 60. Ethernet Receive Timing Diagram



Notes:

1. Transmit clock invert (TCI) bit in GSMR is set.
2. If RENA is deasserted before TENA, or RENA is not asserted at all during transmit, then the CSL bit is set in the buffer descriptor at the end of the frame transmission.

Figure 61. Ethernet Transmit Timing Diagram

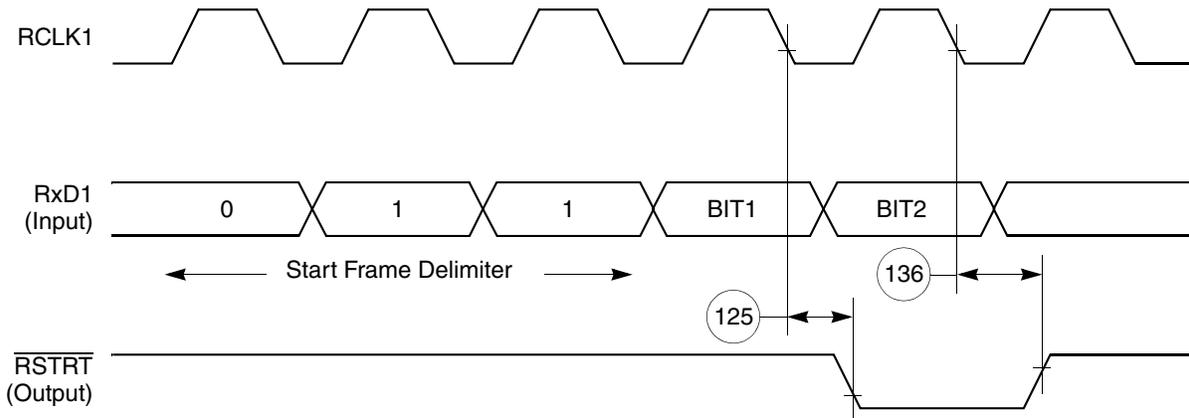


Figure 62. CAM Interface Receive Start Timing Diagram



Figure 63. CAM Interface $\overline{\text{REJECT}}$ Timing Diagram

Figure 69 shows the I²C bus timing.

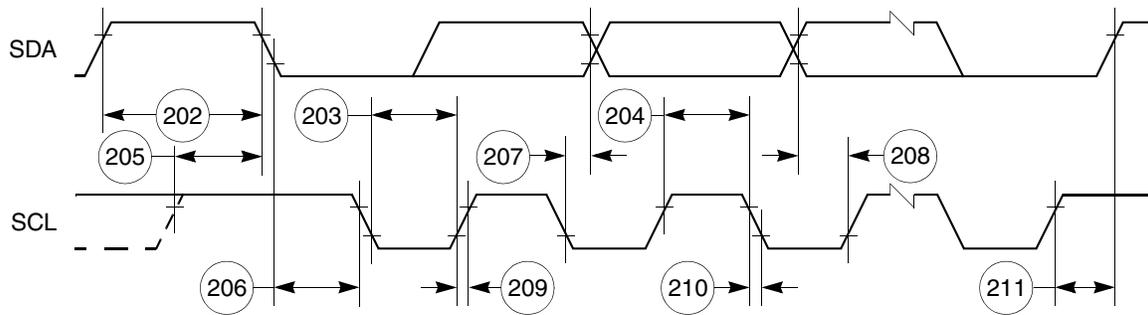


Figure 69. I²C Bus Timing Diagram

12 UTOPIA AC Electrical Specifications

Table 28 shows the AC electrical specifications for the UTOPIA interface.

Table 28. UTOPIA AC Electrical Specifications

Num	Signal Characteristic	Direction	Min	Max	Unit
U1	UtpClk rise/fall time (Internal clock option)	Output	—	3.5	ns
	Duty cycle		50	50	%
	Frequency		—	50	MHz
U1a	UtpClk rise/fall time (external clock option)	Input	—	3.5	ns
	Duty cycle		40	60	%
	Frequency		—	50	MHz
U2	$\overline{\text{RxEnb}}$ and $\overline{\text{TxEnb}}$ active delay	Output	2	16	ns
U3	UTPB, SOC, Rxclav and Txclav setup time	Input	8	—	ns
U4	UTPB, SOC, Rxclav and Txclav hold time	Input	1	—	ns
U5	UTPB, SOC active delay (and PHREQ and PHSEL active delay in MPHY mode)	Output	2	16	ns

13.2 MII Transmit Signal Timing (MII_TXD[3:0], MII_TX_EN, MII_TX_ER, MII_TX_CLK)

The transmitter functions correctly up to a MII_TX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed the MII_TX_CLK frequency – 1%.

Table 30 provides information on the MII transmit signal timing.

Table 30. MII Transmit Signal Timing

Num	Characteristic	Min	Max	Unit
M5	MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER invalid	5	—	ns
M6	MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER valid	—	25	
M7	MII_TX_CLK pulse width high	35	65%	MII_TX_CLK period
M8	MII_TX_CLK pulse width low	35%	65%	MII_TX_CLK period

Figure 73 shows the MII transmit signal timing diagram.

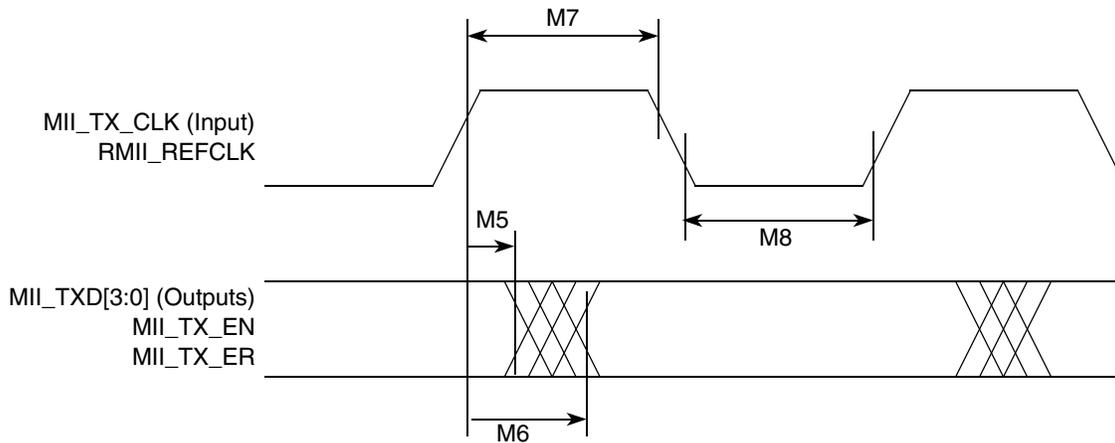


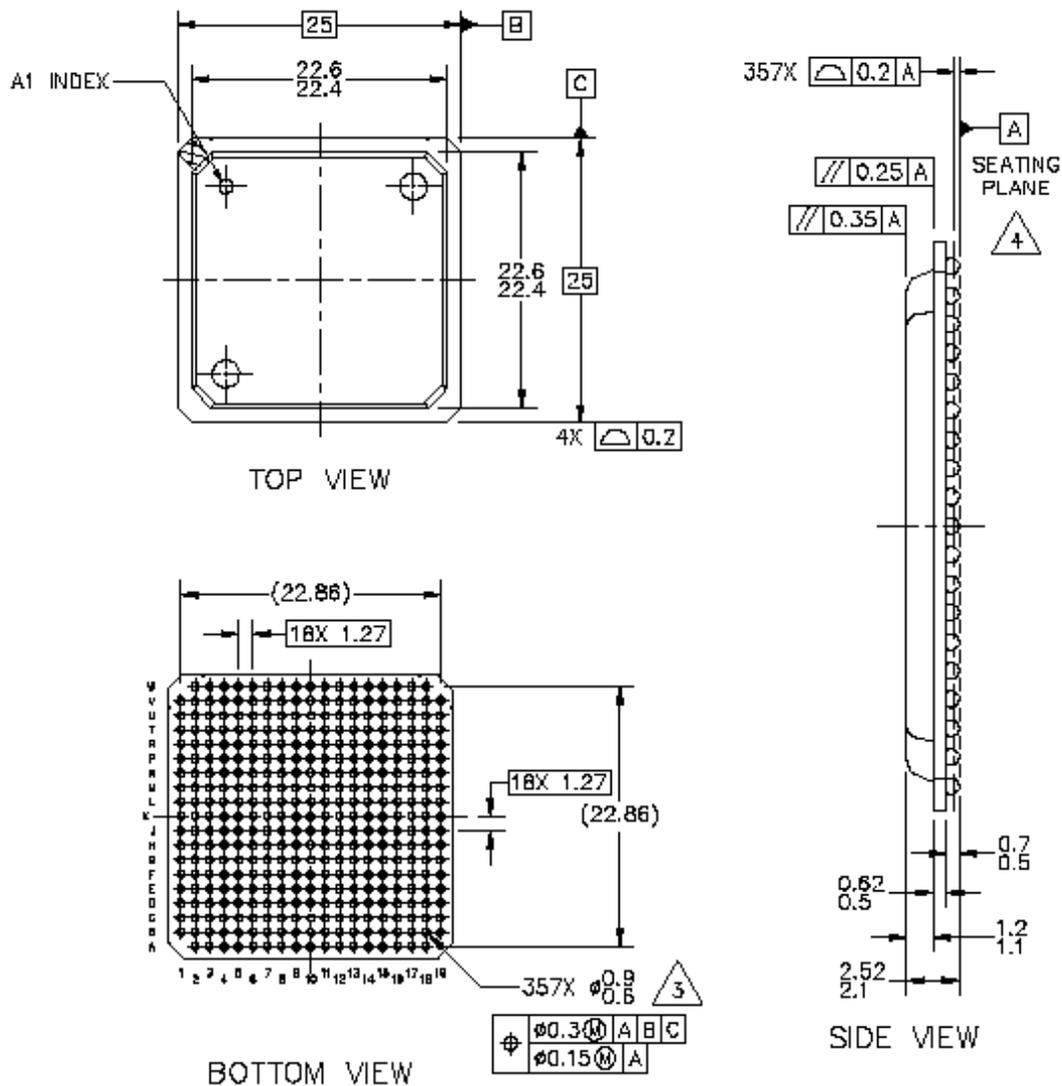
Figure 73. MII Transmit Signal Timing Diagram

Table 34 identifies the packages and operating frequencies available for the MPC860.

Table 34. MPC860 Family Package/Frequency Availability

Package Type	Freq. (MHz) / Temp. (Tj)	Package	Order Number	
Ball grid array ZP suffix—leaded ZQ suffix—leaded VR suffix—lead-free	50 0° to 95°C	ZP/ZQ ¹	MPC855TZQ50D4 MPC860DEZQ50D4 MPC860DTZQ50D4 MPC860ENZQ50D4 MPC860SRZQ50D4 MPC860TZQ50D4 MPC860DPZQ50D4 MPC860PZQ50D4	
		Tape and Reel	MPC855TZQ50D4R2 MPC860DEZQ50D4R2 MPC860ENZQ50D4R2 MPC860SRZQ50D4R2 MPC860TZQ50D4R2 MPC860DPZQ50D4R2 MPC855TVR50D4R2 MPC860ENVR50D4R2 MPC860SRVR50D4R2 MPC860TVR50D4R2	
		VR	MPC855TVR50D4 MPC860DEV50D4 MPC860DPVR50D4 MPC860DTPVR50D4 MPC860ENVR50D4 MPC860PVR50D4 MPC860SRVR50D4 MPC860TVR50D4	
		66 0° to 95°C	ZP/ZQ ¹	MPC855TZQ66D4 MPC860DEZQ66D4 MPC860DTZQ66D4 MPC860ENZQ66D4 MPC860SRZQ66D4 MPC860TZQ66D4 MPC860DPZQ66D4 MPC860PZQ66D4
			Tape and Reel	MPC860SRZQ66D4R2 MPC860PZQ66D4R2
			VR	MPC855TVR66D4 MPC860DEV66D4 MPC860DPVR66D4 MPC860DTPVR66D4 MPC860ENVR66D4 MPC860PVR66D4 MPC860SRVR66D4 MPC860TVR66D4

Figure 78 shows the mechanical dimensions of the ZQ PBGA package.



NOTE

1. All Dimensions in millimeters.
2. Dimensions and tolerance per ASME Y14.5M, 1994.
3. Maximum Solder Ball Diameter measured parallel to Datum A.
4. Datum A, the seating plane, is defined by the spherical crowns of the solder balls.

Figure 78. Mechanical Dimensions and Bottom Surface Nomenclature of the ZQ PBGA Package