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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Obsolete
MPC8xx
1 Core, 32-Bit
66MHz
Communications; CPM
DRAM
No
-
10Mbps (4)
-
-
3.3V
-40°C ~ 95°C (TA)
-
357-BBGA
357-PBGA (25x25)
https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc860enczq66d4

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



2 Features

The following list summarizes the key MPC860 features:

- Embedded single-issue, 32-bit core (implementing the Power Architecture technology) with thirty-two 32-bit general-purpose registers (GPRs)
 - The core performs branch prediction with conditional prefetch without conditional execution.
 - 4- or 8-Kbyte data cache and 4- or 16-Kbyte instruction cache (see Table 1)
 - 16-Kbyte instruction caches are four-way, set-associative with 256 sets; 4-Kbyte instruction caches are two-way, set-associative with 128 sets.
 - 8-Kbyte data caches are two-way, set-associative with 256 sets; 4-Kbyte data caches are two-way, set-associative with 128 sets.
 - Cache coherency for both instruction and data caches is maintained on 128-bit (4-word) cache blocks.
 - Caches are physically addressed, implement a least recently used (LRU) replacement algorithm, and are lockable on a cache block basis.
 - MMUs with 32-entry TLB, fully-associative instruction, and data TLBs
 - MMUs support multiple page sizes of 4-, 16-, and 512-Kbytes, and 8-Mbytes; 16 virtual address spaces and 16 protection groups
 - Advanced on-chip-emulation debug mode
- Up to 32-bit data bus (dynamic bus sizing for 8, 16, and 32 bits)
- 32 address lines
- Operates at up to 80 MHz
- Memory controller (eight banks)
 - Contains complete dynamic RAM (DRAM) controller
 - Each bank can be a chip select or \overline{RAS} to support a DRAM bank.
 - Up to 15 wait states programmable per memory bank
 - Glueless interface to DRAM, SIMMS, SRAM, EPROM, Flash EPROM, and other memory devices
 - DRAM controller programmable to support most size and speed memory interfaces
 - Four $\overline{\text{CAS}}$ lines, four $\overline{\text{WE}}$ lines, and one $\overline{\text{OE}}$ line
 - Boot chip-select available at reset (options for 8-, 16-, or 32-bit memory)
 - Variable block sizes (32 Kbytes to 256 Mbytes)
 - Selectable write protection
 - On-chip bus arbitration logic
- General-purpose timers
 - Four 16-bit timers or two 32-bit timers
 - Gate mode can enable/disable counting
 - Interrupt can be masked on reference match and event capture.



Characteristic	Symbol	Min	Max	Unit
Input leakage current, V_{in} = 3.6 V (except TMS, TRST, DSCK, and DSDI pins)	l _{in}	—	10	μA
Input leakage current, V _{in} = 0 V (except TMS, TRST, DSCK, and DSDI pins)	l _{in}	—	10	μA
Input capacitance ²	C _{in}	—	20	pF
Output high voltage, $I_{OH} = -2.0$ mA, $V_{DDH} = 3.0$ V (except XTAL, XFC, and open-drain pins)	V _{OH}	2.4	—	V
$\label{eq:IDE_Interm} \begin{array}{ c c c c c } \hline Output low voltage \\ I_{OL} = 2.0 \text{ mA, CLKOUT} \\ I_{OL} = 3.2 \text{ mA}^3 \\ I_{OL} = 5.3 \text{ mA}^4 \\ I_{OL} = 7.0 \text{ mA, TXD1/PA14, TXD2/PA12} \\ I_{OL} = 8.9 \text{ mA, TS, TA, TEA, BI, BB, HRESET, SRESET} \end{array}$	V _{OL}		0.5	V

Table 6. DC Electrical Specifications (continued)

 1 V_{IL}(max) for the I²C interface is 0.8 V rather than the 1.5 V as specified in the I²C standard.

² Input capacitance is periodically sampled.

- ³ A(0:31), TSIZ0/REG, TSIZ1, D(0:31), DP(0:3)/IRQ(3:6), RD/WR, BURST, RSV/IRQ2, IP_B(0:1)/IWP(0:1)/VFLS(0:1), IP_B2/IOIS16_B/AT2, IP_B3/IWP2/VF2, IP_B4/LWP0/VF0, IP_B5/LWP1/VF1, IP_B6/DSDI/AT0, IP_B7/PTR/AT3, RXD1/PA15, RXD2/PA13, L1TXDB/PA11, L1RXDB/PA10, L1TXDA/PA9, L1RXDA/PA8, TIN1/L1RCLKA/BRGO1/CLK1/PA7, BRGCLK1/TOUT1/CLK2/PA6, TIN2/L1TCLKA/BRGO2/CLK3/PA5, TOUT2/CLK4/PA4, TIN3/BRGO3/CLK5/PA3, BRGCLK2/ L1RCLKB/TOUT3/CLK6/PA2, TIN4/BRGO4/CLK7/PA1, L1TCLKB/TOUT4/CLK8/PA0, REJCT1/SPISEL/PB31, SPICLK/ PB30,SPIMOSI/PB29, BRGO4/SPIMISO/PB28, BRGO1/I2CSDA/PB27, BRGO2/I2CSCL/PB26, SMTXD1/PB25, SMRXD1/ PB24, SMSYN1/SDACK1/PB23, SMSYN2/SDACK2/PB22, SMTXD2/L1CLKOB/PB21, SMRXD2/L1CLKOA/PB20, L1ST1/ RTS1/PB19, L1ST2/RTS2/PB18, L1ST3/L1RQB/PB17, L1ST4/L1RQA/PB16, BRGO3/PB15, RSTRT1/PB14, L1ST1/RTS1/ DREQ0/PC15, L1ST2/RTS2/DREQ1/PC14, L1ST3/L1RQB/PC13, L1ST4/L1RQA/PC12, CTS1/PC11, TGATE1/CD1/PC10, CTS2/PC9, TGATE2/CD2/PC8, SDACK2/L1TSYNCB/PC7, L1RSYNCB/PC6, SDACK1/L1TSYNCA/PC5, L1RSYNCA/PC4, PD15, PD14, PD13, PD12, PD11, PD10, PD9, PD8, PD5, PD6, PD7, PD4, PD3, MII_MDC, MII_TX_ER, MII_EN, MII_MDIO, and MII_TXD[0:3]
- ⁴ BDIP/GPL_B(5), BR, BG, FRZ/IRQ6, CS(0:5), CS(6)/CE(1)_B, CS(7)/CE(2)_B, WE0/BS_B0/IORD, WE1/BS_B1/IOWR, WE2/BS_B2/PCOE, WE3/BS_B3/PCWE, BS_A(0:3), GPL_A0/GPL_B0, OE/GPL_A1/GPL_B1, GPL_A(2:3)/GPL_B(2:3)/ CS(2:3), UPWAITA/GPL_A4, UPWAITB/GPL_B4, GPL_A5, ALE_A, CE1_A, CE2_A, ALE_B/DSCK/AT1, OP(0:1), OP2/MODCK1/STS, OP3/MODCK2/DSDO, and BADDR(28:30)



Bus Signal Timing

	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		
Num	Characteristic	Min	Мах	Min	Мах	Min	Мах	Min	Max	Unit
B29d	$\overline{WE}(0:3)$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 0	43.45		35.5	_	28.00		20.73	_	ns
B29e	$\overline{\text{CS}}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 0	43.45		35.5		28.00		29.73	_	ns
B29f	\overline{WE} (0:3) negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 1	8.86		6.88	_	5.00	_	3.18		ns
B29g	$\overline{\text{CS}}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 1	8.86	_	6.88	—	5.00	—	3.18	_	ns
B29h	$\overline{WE}(0:3)$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 1	38.67	—	31.38	—	24.50	—	17.83	_	ns
B29i	$\overline{\text{CS}}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 1	38.67		31.38		24.50		17.83	_	ns
B30	\overline{CS} , \overline{WE} (0:3) negated to A(0:31), BADDR(28:30) invalid GPCM write access ⁸	5.58	—	4.25	—	3.00	—	1.79		ns
B30a	$\overline{\text{WE}}(0:3)$ negated to A(0:31), BADDR(28:30) invalid GPCM, write access, TRLX = 0, CSNT = 1, $\overline{\text{CS}}$ negated to A(0:31) invalid GPCM write access, TRLX = 0, CSNT = 1 ACS = 10, or ACS = 11, EBDF = 0	13.15	_	10.50	_	8.00	_	5.58		ns
B30b	$\label{eq:weighted} \hline WE(0:3) \ negated to \ A(0:31), \ invalid \ GPCM \\ BADDR(28:30) \ invalid \ GPCM \ write \ access, \\ TRLX = 1, \ CSNT = 1. \ \overline{CS} \ negated to \\ A(0:31), \ Invalid \ GPCM, \ write \ access, \\ TRLX = 1, \ CSNT = 1, \ ACS = 10, \ or \\ ACS = 11, \ EBDF = 0 \\ \hline \hline \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \$	43.45	_	35.50	_	28.00	_	20.73	_	ns
B30c	$\label{eq:weighted} \begin{array}{ c c c c } \hline WE(0:3) \mbox{ negated to } A(0:31), \mbox{ BADDR}(28:30) \\ \hline \mbox{ invalid GPCM write access, TRLX = 0, } \\ \hline CSNT = 1. \end{cmathcelline CS} \mbox{ negated to } A(0:31) \mbox{ invalid GPCM write access, TRLX = 0, } \\ \hline GPCM \mbox{ write access, TRLX = 0, } \\ \hline ACS = 10, \mbox{ ACS = 11, EBDF = 1} \end{array}$	8.36	_	6.38	_	4.50	_	2.68		ns
B30d	$\overline{WE}(0:3)$ negated to A(0:31), BADDR(28:30) invalid GPCM write access, TRLX = 1, CSNT =1. \overline{CS} negated to A(0:31) invalid GPCM write access TRLX = 1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 1	38.67	_	31.38	_	24.50	_	17.83		ns
B31	CLKOUT falling edge to CS valid—as requested by control bit CST4 in the corresponding word in UPM	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns

Table 7. Bus Operation Timings (continued)



		33 MHz		40 MHz		50 MHz		66 MHz		
Num	Characteristic	Min	Max	Min	Max	Min	Max	Min	Max	Unit
B31a	CLKOUT falling edge to CS valid—as requested by control bit CST1 in the corresponding word in UPM	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.54	ns
B31b	CLKOUT rising edge to \overline{CS} valid—as requested by control bit CST2 in the corresponding word in UPM	1.50	8.00	1.50	8.00	1.50	8.00	1.50	8.00	ns
B31c	CLKOUT rising edge to $\overline{\text{CS}}$ valid—as requested by control bit CST3 in the corresponding word in UPM	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.04	ns
B31d	CLKOUT falling edge to \overline{CS} valid—as requested by control bit CST1 in the corresponding word in UPM, EBDF = 1	13.26	17.99	11.28	16.00	9.40	14.13	7.58	12.31	ns
B32	CLKOUT falling edge to BS valid—as requested by control bit BST4 in the corresponding word in UPM	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns
B32a	CLKOUT falling edge to \overline{BS} valid—as requested by control bit BST1 in the corresponding word in UPM, EBDF = 0	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.54	ns
B32b	CLKOUT rising edge to $\overline{\text{BS}}$ valid—as requested by control bit BST2 in the corresponding word in UPM	1.50	8.00	1.50	8.00	1.50	8.00	1.50	8.00	ns
B32c	CLKOUT rising edge to $\overline{\text{BS}}$ valid—as requested by control bit BST3 in the corresponding word in UPM	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.54	ns
B32d	CLKOUT falling edge to \overline{BS} valid—as requested by control bit BST1 in the corresponding word in UPM, EBDF = 1	13.26	17.99	11.28	16.00	9.40	14.13	7.58	12.31	ns
B33	CLKOUT falling edge to GPL valid—as requested by control bit GxT4 in the corresponding word in UPM	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns
B33a	CLKOUT rising edge to GPL valid—as requested by control bit GxT3 in the corresponding word in UPM	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.54	ns
B34	A(0:31), BADDR(28:30), and D(0:31) to \overline{CS} valid—as requested by control bit CST4 in the corresponding word in UPM	5.58	—	4.25	—	3.00	—	1.79	—	ns
B34a	A(0:31), BADDR(28:30), and D(0:31) to \overline{CS} valid—as requested by control bit CST1 in the corresponding word in UPM	13.15		10.50		8.00		5.58	_	ns
B34b	A(0:31), BADDR(28:30), and D(0:31) to \overline{CS} valid—as requested by control bit CST2 in the corresponding word in UPM	20.73	_	16.75		13.00		9.36	_	ns

Table 7. Bus Operation Timings (continued)



Bus Signal Timing

Figure 9 provides the timing for the input data controlled by the UPM for data beats where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)



Figure 9. Input Data Timing when Controlled by UPM in the Memory Controller and DLT3 = 1

Figure 10 through Figure 13 provide the timing for the external bus read controlled by various GPCM factors.





Figure 14 through Figure 16 provide the timing for the external bus write controlled by various GPCM factors.



Figure 14. External Bus Write Timing (GPCM Controlled—TRLX = 0 or 1, CSNT = 0)



Bus Signal Timing



Figure 20 provides the timing for the synchronous external master access controlled by the GPCM.

Figure 20. Synchronous External Master Access Timing (GPCM Handled ACS = 00)

Figure 21 provides the timing for the asynchronous external master memory access controlled by the GPCM.





Figure 22 provides the timing for the asynchronous external master control signals negation.



Figure 22. Asynchronous External Master—Control Signals Negation Timing



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Table 8 provides interrupt timing for the MPC860.

Table 8. Interrupt Timing

Num	Characteristic1	All Frequencies		Unit
	Characteristic	Min	Мах	Unit
139	IRQx valid to CLKOUT rising edge (setup time)	6.00	_	ns
140	IRQx hold time after CLKOUT	2.00	_	ns
141	IRQx pulse width low	3.00	—	ns
142	IRQx pulse width high	3.00	_	ns
143	IRQx edge-to-edge time	$4 \times T_{CLOCKOUT}$	—	—

The timings I39 and I40 describe the testing conditions under which the IRQ lines are tested when being defined as level-sensitive. The IRQ lines are synchronized internally and do not have to be asserted or negated with reference to the CLKOUT.

The timings I41, I42, and I43 are specified to allow the correct function of the IRQ lines detection circuitry and have no direct relation with the total system interrupt latency that the MPC860 is able to support.

Figure 23 provides the interrupt detection timing for the external level-sensitive lines.



Figure 23. Interrupt Detection Timing for External Level Sensitive Lines

Figure 24 provides the interrupt detection timing for the external edge-sensitive lines.



Figure 24. Interrupt Detection Timing for External Edge Sensitive Lines





Figure 34 provides the reset timing for the debug port configuration.

Figure 34. Reset Timing—Debug Port Configuration

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Table 13 provides the JTAG timings for the MPC860 shown in Figure 35 through Figure 38.

Num	Characteristic	All Freq	Unit	
Nulli	Characteristic	Min	Мах	Onit
J82	TCK cycle time	100.00	—	ns
J83	TCK clock pulse width measured at 1.5 V	40.00	_	ns
J84	TCK rise and fall times	0.00	10.00	ns
J85	TMS, TDI data setup time	5.00	—	ns
J86	TMS, TDI data hold time	25.00	_	ns
J87	TCK low to TDO data valid	—	27.00	ns
J88	TCK low to TDO data invalid	0.00	—	ns
J89	TCK low to TDO high impedance	—	20.00	ns
J90	TRST assert time	100.00	_	ns
J91	TRST setup time to TCK low	40.00	—	ns
J92	TCK falling edge to output valid	—	50.00	ns
J93	TCK falling edge to output valid out of high impedance	—	50.00	ns
J94	TCK falling edge to output high impedance	—	50.00	ns
J95	Boundary scan input valid to TCK rising edge	50.00	—	ns
J96	TCK rising edge to boundary scan input invalid	50.00		ns

Table 13. JTAG Timing



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Figure 35. JTAG Test Clock Input Timing



Figure 36. JTAG Test Access Port Timing Diagram



Figure 37. JTAG TRST Timing Diagram







Figure 43. Parallel I/O Data-In/Data-Out Timing Diagram

11.2 Port C Interrupt AC Electrical Specifications

Table 15 provides the timings for port C interrupts.

Num	Characteristic		\geq 33.34 MHz ¹		
		Min	Max	Onic	
35	Port C interrupt pulse width low (edge-triggered mode)	55	—	ns	
36	Port C interrupt minimum time between active edges	55		ns	

¹ External bus frequency of greater than or equal to 33.34 MHz.

Figure 44 shows the port C interrupt detection timing.



Figure 44. Port C Interrupt Detection Timing

11.3 IDMA Controller AC Electrical Specifications

Table 16 provides the IDMA controller timings as shown in Figure 45 through Figure 48.

Table 16. IDMA Controller Timing

Num	Characteristic	All Freq	Unit	
		Min	Max	Unit
40	DREQ setup time to clock high	7	_	ns
41	DREQ hold time from clock high	3	_	ns



Num	Charactariatia	All Freq	Unit	
		Min	Мах	Unit
42	SDACK assertion delay from clock high	—	12	ns
43	SDACK negation delay from clock low	—	12	ns
44	SDACK negation delay from TA low	—	20	ns
45	SDACK negation delay from clock high	_	15	ns
46	\overline{TA} assertion to rising edge of the clock setup time (applies to external \overline{TA})	7		ns

Table 16. IDMA Controller Timing (continued)



Figure 45. IDMA External Requests Timing Diagram



Figure 46. SDACK Timing Diagram—Peripheral Write, Externally-Generated TA



11.4 Baud Rate Generator AC Electrical Specifications

Table 17 provides the baud rate generator timings as shown in Figure 49.

Table 17. Baud Rate Generator Timing

Num	Characteristic	All Freq	Unit	
		Min	Мах	Unit
50	BRGO rise and fall time	—	10	ns
51	BRGO duty cycle	40	60	%
52	BRGO cycle	40	—	ns



Figure 49. Baud Rate Generator Timing Diagram

11.5 Timer AC Electrical Specifications

Table 18 provides the general-purpose timer timings as shown in Figure 50.

Table 18. Timer Timing

Num	Characteristic	All Freq	Unit	
		Min	Мах	Unit
61	TIN/TGATE rise and fall time	10	—	ns
62	TIN/TGATE low time	1	—	CLK
63	TIN/TGATE high time	2	—	CLK
64	TIN/TGATE cycle time	3	—	CLK
65	CLKO low to TOUT valid	3	25	ns





Figure 50. CPM General-Purpose Timers Timing Diagram

11.6 Serial Interface AC Electrical Specifications

Table 19 provides the serial interface timings as shown in Figure 51 through Figure 55.

Num	Obevectovictie	All Freq	luencies	ncies	
NUM	Min		Max	Unit	
70	L1RCLK, L1TCLK frequency (DSC = 0) ^{1, 2}		SYNCCLK/2.5	MHz	
71	L1RCLK, L1TCLK width low $(DSC = 0)^2$	P + 10	—	ns	
71a	L1RCLK, L1TCLK width high $(DSC = 0)^3$	P + 10	—	ns	
72	L1TXD, L1ST(1–4), L1RQ, L1CLKO rise/fall time	—	15.00	ns	
73	L1RSYNC, L1TSYNC valid to L1CLK edge (SYNC setup time)	20.00	—	ns	
74	L1CLK edge to L1RSYNC, L1TSYNC, invalid (SYNC hold time)	35.00	—	ns	
75	L1RSYNC, L1TSYNC rise/fall time	—	15.00	ns	
76	L1RXD valid to L1CLK edge (L1RXD setup time)	17.00	—	ns	
77	L1CLK edge to L1RXD invalid (L1RXD hold time)	13.00	—	ns	
78	L1CLK edge to L1ST(1-4) valid ⁴	10.00	45.00	ns	
78A	L1SYNC valid to L1ST(1-4) valid	10.00	45.00	ns	
79	L1CLK edge to L1ST(1-4) invalid	10.00	45.00	ns	
80	L1CLK edge to L1TXD valid	10.00	55.00	ns	
80A	L1TSYNC valid to L1TXD valid ⁴	10.00	55.00	ns	
81	L1CLK edge to L1TXD high impedance	0.00	42.00	ns	
82	L1RCLK, L1TCLK frequency (DSC =1)	—	16.00 or SYNCCLK/2	MHz	
83	L1RCLK, L1TCLK width low (DSC = 1)	P + 10	_	ns	
83a	L1RCLK, L1TCLK width high $(DSC = 1)^3$	P + 10	—	ns	

Table 19. SI Timing



CPM Electrical Characteristics



MPC860 PowerQUICC Family Hardware Specifications, Rev. 10



Num	Chavastavistia	All Frequencies		Unit
	Characteristic	Min	Мах	Unit
135	RSTRT active delay (from TCLK1 falling edge)	10	50	ns
136	RSTRT inactive delay (from TCLK1 falling edge)	10	50	ns
137	REJECT width low	1	—	CLK
138	CLKO1 low to SDACK asserted ²		20	ns
139	CLKO1 low to SDACK negated ²	_	20	ns

Table 22. Ethernet Timing (continued)

¹ The ratios SYNCCLK/RCLK1 and SYNCCLK/TCLK1 must be greater than or equal to 2/1.

² SDACK is asserted whenever the SDMA writes the incoming frame DA into memory.



Figure 59. Ethernet Collision Timing Diagram



Figure 60. Ethernet Receive Timing Diagram



11.12 I²C AC Electrical Specifications

Table 26 provides the I^2C (SCL < 100 kHz) timings.

Table 26. I²C Timing (SCL < 100 kHz)

Num	Characteristic	All Freq	encies	
		Min	Мах	Unit
200	SCL clock frequency (slave)	0	100	kHz
200	SCL clock frequency (master) ¹	1.5	100	kHz
202	Bus free time between transmissions	4.7	—	μS
203	Low period of SCL	4.7	—	μS
204	High period of SCL	4.0	—	μS
205	Start condition setup time	4.7	—	μS
206	Start condition hold time	4.0	—	μS
207	Data hold time	0	—	μS
208	Data setup time	250	—	ns
209	SDL/SCL rise time	—	1	μS
210	SDL/SCL fall time	—	300	ns
211	Stop condition setup time	4.7	—	μS

SCL frequency is given by SCL = BRGCLK_frequency / ((BRG register + 3 × pre_scaler × 2). The ratio SYNCCLK/(BRGCLK/pre_scaler) must be greater than or equal to 4/1.

Table 27 provides the I^2C (SCL > 100 kHz) timings.

Table 27. . I²C Timing (SCL > 100 kHz)

Num	Characteristic	Expression Min	All Freq	All Frequencies	
Num	Characteristic		Min	Мах	onit
200	SCL clock frequency (slave)	fSCL	0	BRGCLK/48	Hz
200	SCL clock frequency (master) ¹	fSCL	BRGCLK/16512	BRGCLK/48	Hz
202	Bus free time between transmissions		1/(2.2 * fSCL)	—	S
203	Low period of SCL		1/(2.2 * fSCL)	—	S
204	High period of SCL		1/(2.2 * fSCL)	—	S
205	Start condition setup time		1/(2.2 * fSCL)	—	S
206	Start condition hold time		1/(2.2 * fSCL)	—	S
207	Data hold time		0	—	S
208	Data setup time		1/(40 * fSCL)	—	S
209	SDL/SCL rise time		—	1/(10 * fSCL)	S
210	SDL/SCL fall time		—	1/(33 * fSCL)	S
211	Stop condition setup time		1/2(2.2 * fSCL)	—	s

SCL frequency is given by SCL = BRGCLK_frequency / ((BRG register + 3) × pre_scaler × 2). The ratio SYNCCLK/(BRGCLK / pre_scaler) must be greater than or equal to 4/1.



Mechanical Data and Ordering Information

Figure 75 shows the MII serial management channel timing diagram.



Figure 75. MII Serial Management Channel Timing Diagram

14 Mechanical Data and Ordering Information

14.1 Ordering Information

Table 33 provides information on the MPC860 Revision D.4 derivative devices.

Device	Number of SCCs ¹	Ethernet Support ² (Mbps)	Multichannel HDLC Support	ATM Support
MPC855T	1	10/100	Yes	Yes
MPC860DE	2	10	N/A	N/A
MPC860DT		10/100	Yes	Yes
MPC860DP		10/100	Yes	Yes
MPC860EN	4	10	N/A	N/A
MPC860SR		10	Yes	Yes
MPC860T		10/100	Yes	Yes
MPC860P		10/100	Yes	Yes

Table 33. MPC860 Family Revision D.4 Derivatives

¹ Serial communications controller (SCC)

² Up to 4 channels at 40 MHz or 2 channels at 25 MHz



Table 34 identifies the packages and operating frequencies available for the MPC860.

Package Type	Freq. (MHz) / Temp. (Tj)	Package	Order Number
Ball grid array ZP suffix—leaded ZQ suffix—leaded VR suffix—lead-free	50 0° to 95°C	ZP/ZQ ¹	MPC855TZQ50D4 MPC860DEZQ50D4 MPC860DTZQ50D4 MPC860ENZQ50D4 MPC860SRZQ50D4 MPC860TZQ50D4 MPC860DPZQ50D4 MPC860PZQ50D4
		Tape and Reel	MPC855TZQ50D4R2 MPC860DEZQ50D4R2 MPC860ENZQ50D4R2 MPC860SRZQ50D4R2 MPC860TZQ50D4R2 MPC860DPZQ50D4R2 MPC855TVR50D4R2 MPC860ENVR50D4R2 MPC860SRVR50D4R2 MPC860TVR50D4R2
		VR	MPC855TVR50D4 MPC860DEVR50D4 MPC860DPVR50D4 MPC860DTVR50D4 MPC860ENVR50D4 MPC860PVR50D4 MPC860SRVR50D4 MPC860SRVR50D4 MPC860TVR50D4
	66 0° to 95°C	ZP/ZQ ¹	MPC855TZQ66D4 MPC860DEZQ66D4 MPC860DTZQ66D4 MPC860ENZQ66D4 MPC860SRZQ66D4 MPC860TZQ66D4 MPC860DPZQ66D4 MPC860PZQ66D4
		Tape and Reel	MPC860SRZQ66D4R2 MPC860PZQ66D4R2
		VR	MPC855TVR66D4 MPC860DEVR66D4 MPC860DPVR66D4 MPC860DTVR66D4 MPC860ENVR66D4 MPC860PVR66D4 MPC860SRVR66D4 MPC860TVR66D4

Table 34. MPC860 Family Package/Frequency Availability



Mechanical Data and Ordering Information

Package Type	Freq. (MHz) / Temp. (Tj)	Package	Order Number
Ball grid array <i>(continued)</i> ZP suffix—leaded ZQ suffix—leaded VR suffix—lead-free	80 0° to 95°C	ZP/ZQ ¹	MPC855TZQ80D4 MPC860DEZQ80D4 MPC860DTZQ80D4 MPC860ENZQ80D4 MPC860SRZQ80D4 MPC860TZQ80D4 MPC860DPZQ80D4 MPC860PZQ80D4
		Tape and Reel	MPC860PZQ80D4R2 MPC860PVR80D4R2
		VR	MPC855TVR80D4 MPC860DEVR80D4 MPC860DPVR80D4 MPC860ENVR80D4 MPC860PVR80D4 MPC860SRVR80D4 MPC860SRVR80D4
Ball grid array (CZP suffix) CZP suffix—leaded CZQ suffix—leaded CVR suffix—lead-free	50 –40° to 95°C	ZP/ZQ ¹	MPC855TCZQ50D4 MPC855TCVR50D4 MPC860DECZQ50D4 MPC860DTCZQ50D4 MPC860ENCZQ50D4 MPC860SRCZQ50D4 MPC860TCZQ50D4 MPC860DPCZQ50D4 MPC860PCZQ50D4
		Tape and Reel	MPC855TCZQ50D4R2 MC860ENCVR50D4R2
		CVR	MPC860DECVR50D4 MPC860DTCVR50D4 MPC860ENCVR50D4 MPC860PCVR50D4 MPC860SRCVR50D4 MPC860TCVR50D4
	66 –40° to 95°C	ZP/ZQ ¹	MPC855TCZQ66D4 MPC855TCVR66D4 MPC860ENCZQ66D4 MPC860SRCZQ66D4 MPC860TCZQ66D4 MPC860DPCZQ66D4 MPC860PCZQ66D4
		CVR	MPC860DTCVR66D4 MPC860ENCVR66D4 MPC860PCVR66D4 MPC860SRCVR66D4 MPC860TCVR66D4

Table 34. MPC860 Family Package/Frequency Availability (continued)

¹ The ZP package is no longer recommended for use. The ZQ package replaces the ZP package.