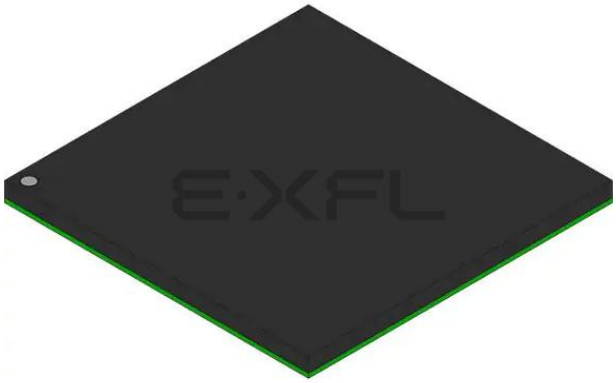

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Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	80MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (4)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 95°C (TA)
Security Features	-
Package / Case	357-BBGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc860envr80d4

3 Maximum Tolerated Ratings

This section provides the maximum tolerated voltage and temperature ranges for the MPC860. Table 2 provides the maximum ratings.

This device contains circuitry protecting against damage due to high-static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or V_{DD}).

Table 2. Maximum Tolerated Ratings

(GND = 0 V)

Rating	Symbol	Value	Unit
Supply voltage[1]	V_{DDH}	–0.3 to 4.0	V
	V_{DDL}	–0.3 to 4.0	V
	KAPWR	–0.3 to 4.0	V
	V_{DDSYN}	–0.3 to 4.0	V
Input voltage[2]	V_{in}	GND – 0.3 to V_{DDH}	V
Temperature[3] (standard)	$T_{A(min)}$	0	°C
	$T_{j(max)}$	95	°C
Temperature[3] (extended)	$T_{A(min)}$	–40	°C
	$T_{j(max)}$	95	°C
Storage temperature range	T_{stg}	–55 to 150	°C

1 The power supply of the device must start its ramp from 0.0 V.

2 Functional operating conditions are provided with the DC electrical specifications in Table 6. Absolute maximum ratings are stress ratings only; functional operation at the maxima is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device.
Caution: All inputs that tolerate 5 V cannot be more than 2.5 V greater than the supply voltage. This restriction applies to power-up and normal operation (that is, if the MPC860 is unpowered, voltage greater than 2.5 V must not be applied to its inputs).

3 Minimum temperatures are guaranteed as ambient temperature, T_A. Maximum temperatures are guaranteed as junction temperature, T_j.

Table 4 shows the thermal characteristics for the MPC860.

Table 4. MPC860 Thermal Resistance Data

Rating	Environment		Symbol	ZP MPC860P	ZQ / VR MPC860P	Unit
Mold Compound Thickness				0.85	1.15	mm
Junction-to-ambient [1]	Natural convection	Single-layer board (1s)	$R_{\theta JA}$ [2]	34	34	°C/W
		Four-layer board (2s2p)	$R_{\theta JMA}$ [3]	22	22	
	Airflow (200 ft/min)	Single-layer board (1s)	$R_{\theta JMA}$ [3]	27	27	
		Four-layer board (2s2p)	$R_{\theta JMA}$ [3]	18	18	
Junction-to-board [4]			$R_{\theta JB}$	14	13	
Junction-to-case [5]			$R_{\theta JC}$	6	8	
Junction-to-package top [6]	Natural convection		Ψ_{JT}	2	2	

1 Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.

2 Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature. For exposed pad packages where the pad would be expected to be soldered, junction-to-case thermal resistance is a simulated value from the junction to the exposed pad without contact resistance.

6 Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2.

9 Bus Signal Timing

Table 7 provides the bus operation timing for the MPC860 at 33, 40, 50, and 66 MHz.

The maximum bus speed supported by the MPC860 is 66 MHz. Higher-speed parts must be operated in half-speed bus mode (for example, an MPC860 used at 80 MHz must be configured for a 40-MHz bus).

The timing for the MPC860 bus shown assumes a 50-pF load for maximum delays and a 0-pF load for minimum delays.

Table 7. Bus Operation Timings

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B1	CLKOUT period	30.30	30.30	25.00	30.30	20.00	30.30	15.15	30.30	ns
B1a	EXTCLK to CLKOUT phase skew (EXTCLK > 15 MHz and MF <= 2)	–0.90	0.90	–0.90	0.90	–0.90	0.90	–0.90	0.90	ns
B1b	EXTCLK to CLKOUT phase skew (EXTCLK > 10 MHz and MF < 10)	–2.30	2.30	–2.30	2.30	–2.30	2.30	–2.30	2.30	ns
B1c	CLKOUT phase jitter (EXTCLK > 15 MHz and MF <= 2)[1]	–0.60	0.60	–0.60	0.60	–0.60	0.60	–0.60	0.60	ns
B1d	CLKOUT phase jitter[1]	–2.00	2.00	–2.00	2.00	–2.00	2.00	–2.00	2.00	ns
B1e	CLKOUT frequency jitter (MF < 10)[1]	—	0.50	—	0.50	—	0.50	—	0.50	%
B1f	CLKOUT frequency jitter (10 < MF < 500)[1]	—	2.00	—	2.00	—	2.00	—	2.00	%
B1g	CLKOUT frequency jitter (MF > 500)[1]	—	3.00	—	3.00	—	3.00	—	3.00	%
B1h	Frequency jitter on EXTCLK[2]	—	0.50	—	0.50	—	0.50	—	0.50	%
B2	CLKOUT pulse width low	12.12	—	10.00	—	8.00	—	6.06	—	ns
B3	CLKOUT width high	12.12	—	10.00	—	8.00	—	6.06	—	ns
B4	CLKOUT rise time[3]	—	4.00	—	4.00	—	4.00	—	4.00	ns
B5[33]	CLKOUT fall time[3]	—	4.00	—	4.00	—	4.00	—	4.00	ns
B7	CLKOUT to A(0:31), BADDR(28:30), RD/$\overline{WR}$, $\overline{BURST}$, D(0:31), DP(0:3) invalid	7.58	—	6.25	—	5.00	—	3.80	—	ns
B7a	CLKOUT to TSIZ(0:1), $\overline{REG}$, $\overline{RSV}$, AT(0:3), $\overline{BDIP}$, PTR invalid	7.58	—	6.25	—	5.00	—	3.80	—	ns
B7b	CLKOUT to $\overline{BR}$, $\overline{BG}$, FRZ, VFLS(0:1), VF(0:2) IWP(0:2), LWP(0:1), $\overline{STS}$ invalid [4]	7.58	—	6.25	—	5.00	—	3.80	—	ns
B8	CLKOUT to A(0:31), BADDR(28:30) RD/$\overline{WR}$, $\overline{BURST}$, D(0:31), DP(0:3) valid	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.04	ns
B8a	CLKOUT to TSIZ(0:1), $\overline{REG}$, $\overline{RSV}$, AT(0:3) $\overline{BDIP}$, PTR valid	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.04	ns
B8b	CLKOUT to $\overline{BR}$, $\overline{BG}$, VFLS(0:1), VF(0:2), IWP(0:2), FRZ, LWP(0:1), $\overline{STS}$ valid [4]	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.04	ns

Table 7. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B29d	$\overline{WE}$(0:3) negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 0	43.45	—	35.5	—	28.00	—	20.73	—	ns
B29e	$\overline{CS}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 0	43.45	—	35.5	—	28.00	—	29.73	—	ns
B29f	$\overline{WE}$(0:3) negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 1	8.86	—	6.88	—	5.00	—	3.18	—	ns
B29g	$\overline{CS}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 1	8.86	—	6.88	—	5.00	—	3.18	—	ns
B29h	$\overline{WE}$(0:3) negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 1	38.67	—	31.38	—	24.50	—	17.83	—	ns
B29i	$\overline{CS}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 1	38.67	—	31.38	—	24.50	—	17.83	—	ns
B30	$\overline{CS}$, $\overline{WE}$(0:3) negated to A(0:31), BADDR(28:30) invalid GPCM write access [8]	5.58	—	4.25	—	3.00	—	1.79	—	ns
B30a	$\overline{WE}$(0:3) negated to A(0:31), BADDR(28:30) invalid GPCM, write access, TRLX = 0, CSNT = 1, $\overline{CS}$ negated to A(0:31) invalid GPCM write access, TRLX = 0, CSNT = 1 ACS = 10, or ACS = 11, EBDF = 0	13.15	—	10.50	—	8.00	—	5.58	—	ns
B30b	$\overline{WE}$(0:3) negated to A(0:31), invalid GPCM BADDR(28:30) invalid GPCM write access, TRLX = 1, CSNT = 1. $\overline{CS}$ negated to A(0:31), Invalid GPCM, write access, TRLX = 1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 0	43.45	—	35.50	—	28.00	—	20.73	—	ns
B30c	$\overline{WE}$(0:3) negated to A(0:31), BADDR(28:30) invalid GPCM write access, TRLX = 0, CSNT = 1. $\overline{CS}$ negated to A(0:31) invalid GPCM write access, TRLX = 0, CSNT = 1, ACS = 10, ACS = 11, EBDF = 1	8.36	—	6.38	—	4.50	—	2.68	—	ns
B30d	$\overline{WE}$(0:3) negated to A(0:31), BADDR(28:30) invalid GPCM write access, TRLX = 1, CSNT =1. $\overline{CS}$ negated to A(0:31) invalid GPCM write access TRLX = 1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 1	38.67	—	31.38	—	24.50	—	17.83	—	ns
B31	CLKOUT falling edge to $\overline{CS}$ valid—as requested by control bit CST4 in the corresponding word in UPM	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns

Table 7. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B35	A(0:31), BADDR(28:30) to $\overline{CS}$ valid—as requested by control bit BST4 in the corresponding word in UPM	5.58	—	4.25	—	3.00	—	1.79	—	ns
B35a	A(0:31), BADDR(28:30), and D(0:31) to $\overline{BS}$ valid—as requested by control bit BST1 in the corresponding word in UPM	13.15	—	10.50	—	8.00	—	5.58	—	ns
B35b	A(0:31), BADDR(28:30), and D(0:31) to $\overline{BS}$ valid—as requested by control bit BST2 in the corresponding word in UPM	20.73	—	16.75	—	13.00	—	9.36	—	ns
B36	A(0:31), BADDR(28:30), and D(0:31) to $\overline{GPL}$ valid—as requested by control bit GxT4 in the corresponding word in UPM	5.58	—	4.25	—	3.00	—	1.79	—	ns
B37	UPWAIT valid to CLKOUT falling edge[9]	6.00	—	6.00	—	6.00	—	6.00	—	ns
B38	CLKOUT falling edge to UPWAIT valid[9]	1.00	—	1.00	—	1.00	—	1.00	—	ns
B39	$\overline{AS}$ valid to CLKOUT rising edge[10]	7.00	—	7.00	—	7.00	—	7.00	—	ns
B40	A(0:31), TSIZ(0:1), RD/$\overline{WR}$, $\overline{BURST}$, valid to CLKOUT rising edge	7.00	—	7.00	—	7.00	—	7.00	—	ns
B41	$\overline{TS}$ valid to CLKOUT rising edge (setup time)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B42	CLKOUT rising edge to $\overline{TS}$ valid (hold time)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B43	$\overline{AS}$ negation to memory controller signals negation	—	TBD	—	TBD	—	TBD	—	TBD	ns

1 Phase and frequency jitter performance results are only valid if the input jitter is less than the prescribed value.

2 If the rate of change of the frequency of EXTAL is slow (that is, it does not jump between the minimum and maximum values in one cycle) or the frequency of the jitter is fast (that is, it does not stay at an extreme value for a long time) then the maximum allowed jitter on EXTAL can be up to 2%.

3 The timings specified in B4 and B5 are based on full strength clock.

4 The timing for $\overline{BR}$ output is relevant when the MPC860 is selected to work with external bus arbiter. The timing for $\overline{BG}$ output is relevant when the MPC860 is selected to work with internal bus arbiter.

5 The timing required for $\overline{BR}$ input is relevant when the MPC860 is selected to work with internal bus arbiter. The timing for $\overline{BG}$ input is relevant when the MPC860 is selected to work with external bus arbiter.

6 The D(0:31) and DP(0:3) input timings B18 and B19 refer to the rising edge of the CLKOUT in which the $\overline{TA}$ input signal is asserted.

7 The D(0:31) and DP(0:3) input timings B20 and B21 refer to the falling edge of the CLKOUT. This timing is valid only for read accesses controlled by chip-selects under control of the UPM in the memory controller, for data beats where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

8 The timing B30 refers to $\overline{CS}$ when ACS = 00 and to $\overline{WE}$(0:3) when CSNT = 0.

9 The signal UPWAIT is considered asynchronous to the CLKOUT and synchronized internally. The timings specified in B37 and B38 are specified to enable the freeze of the UPM output signals as described in Figure 18.

10 The $\overline{AS}$ signal is considered asynchronous to the CLKOUT. The timing B39 is specified in order to allow the behavior specified in Figure 21.

Figure 5 provides the timing for the synchronous output signals.

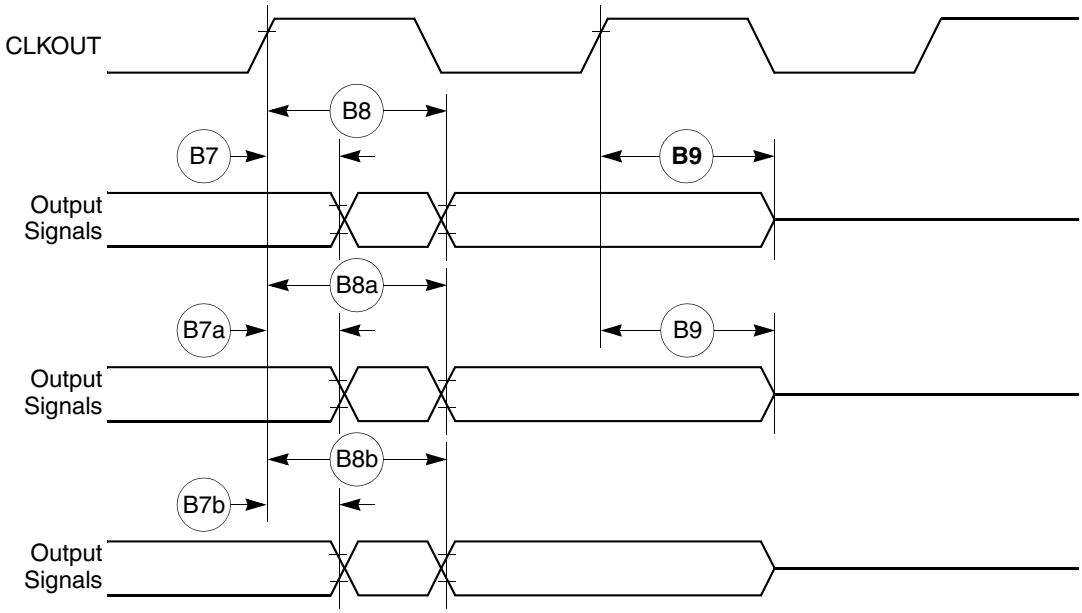

Figure 5. Synchronous Output Signals Timing

Figure 6 provides the timing for the synchronous active pull-up and open-drain output signals.

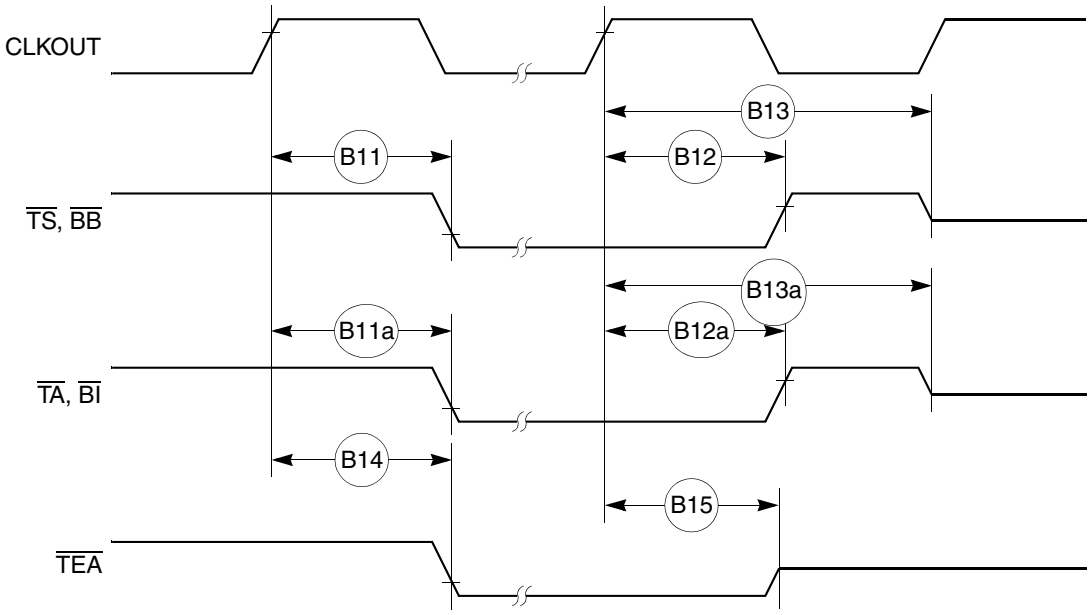

Figure 6. Synchronous Active Pull-Up Resistor and Open-Drain Outputs Signals Timing

Figure 7 provides the timing for the synchronous input signals.

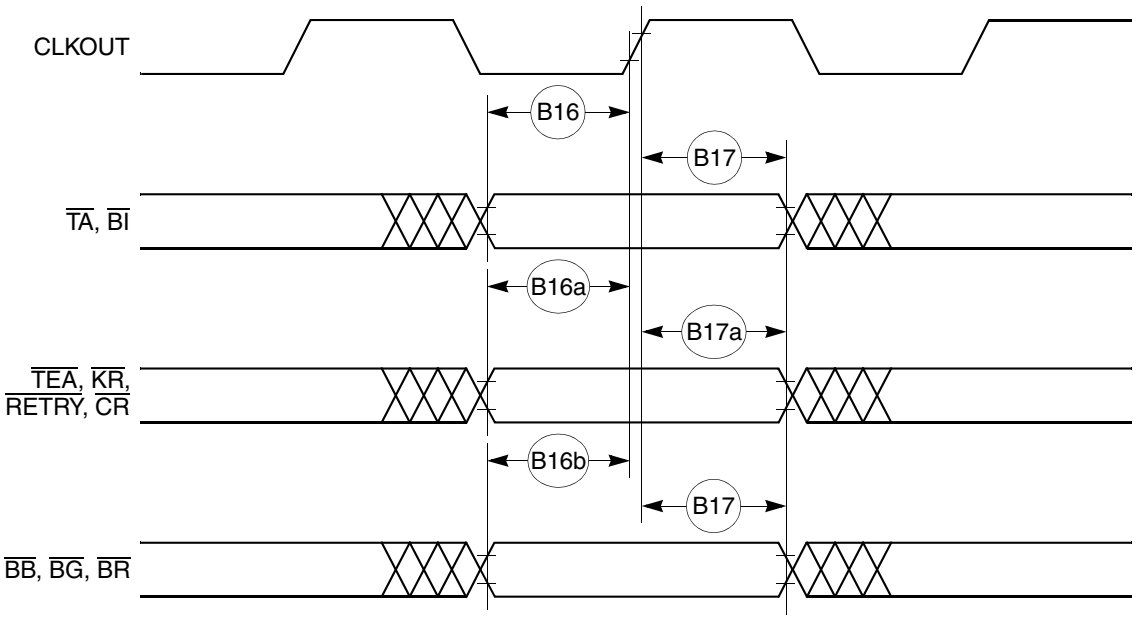

Figure 7. Synchronous Input Signals Timing

Figure 8 provides normal case timing for input data. It also applies to normal read accesses under the control of the UPM in the memory controller.

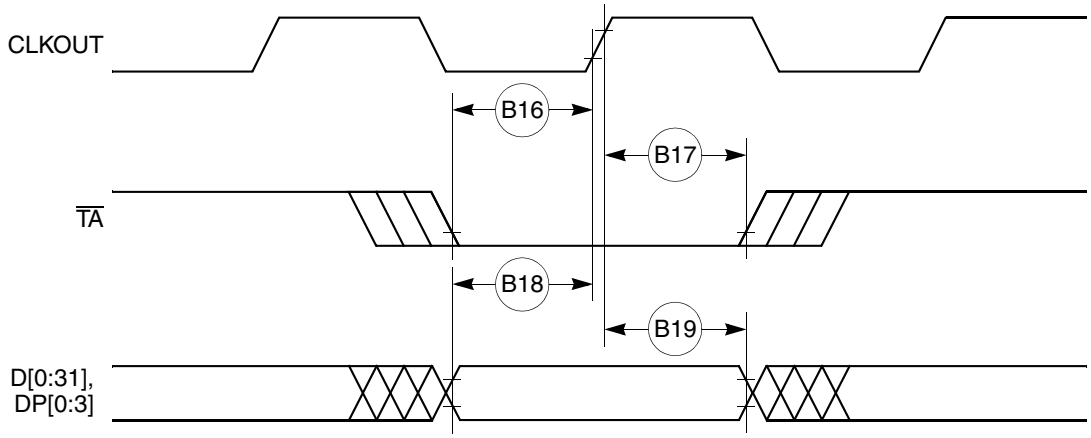

Figure 8. Input Data Timing in Normal Case

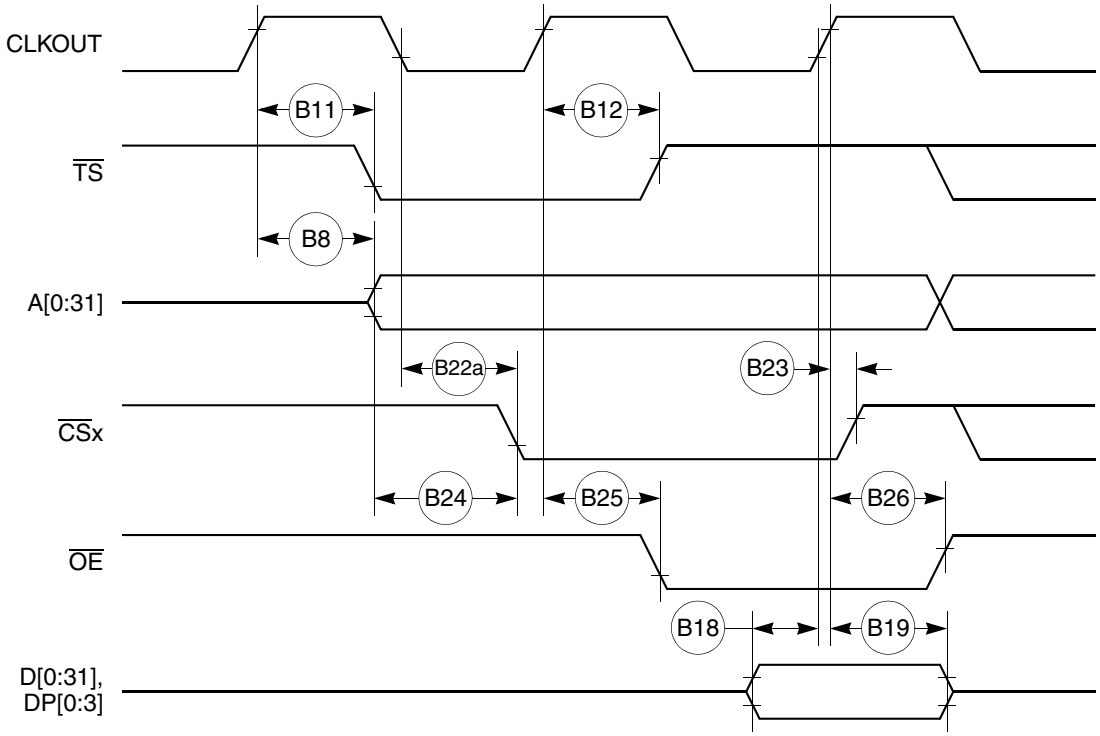

Figure 11. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 10)

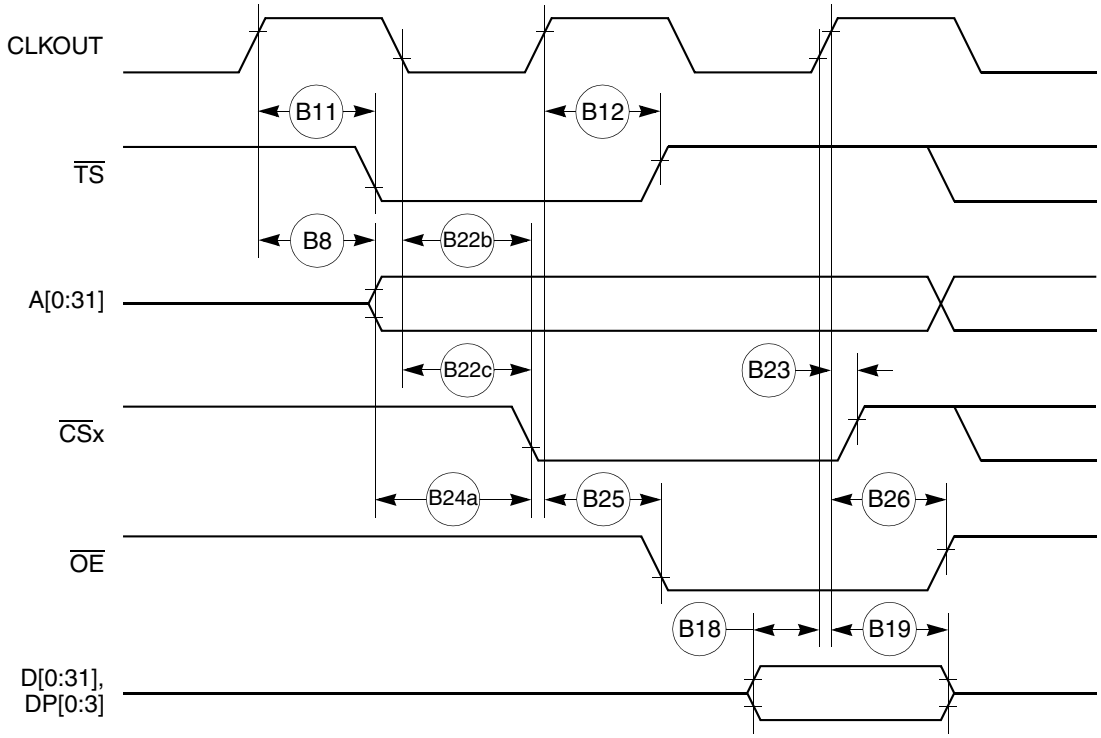

Figure 12. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 11)

Figure 14 through Figure 16 provide the timing for the external bus write controlled by various GPCM factors.

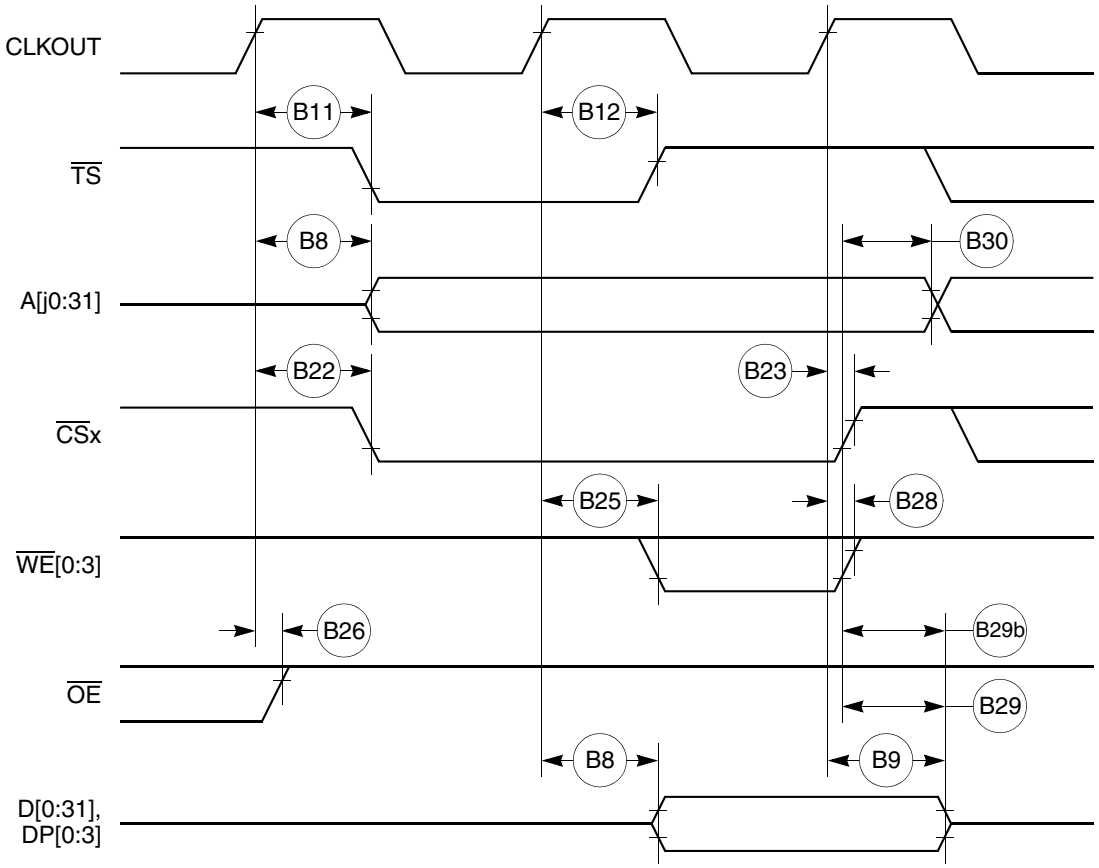

Figure 14. External Bus Write Timing (GPCM Controlled—TRLX = 0 or 1, CSNT = 0)

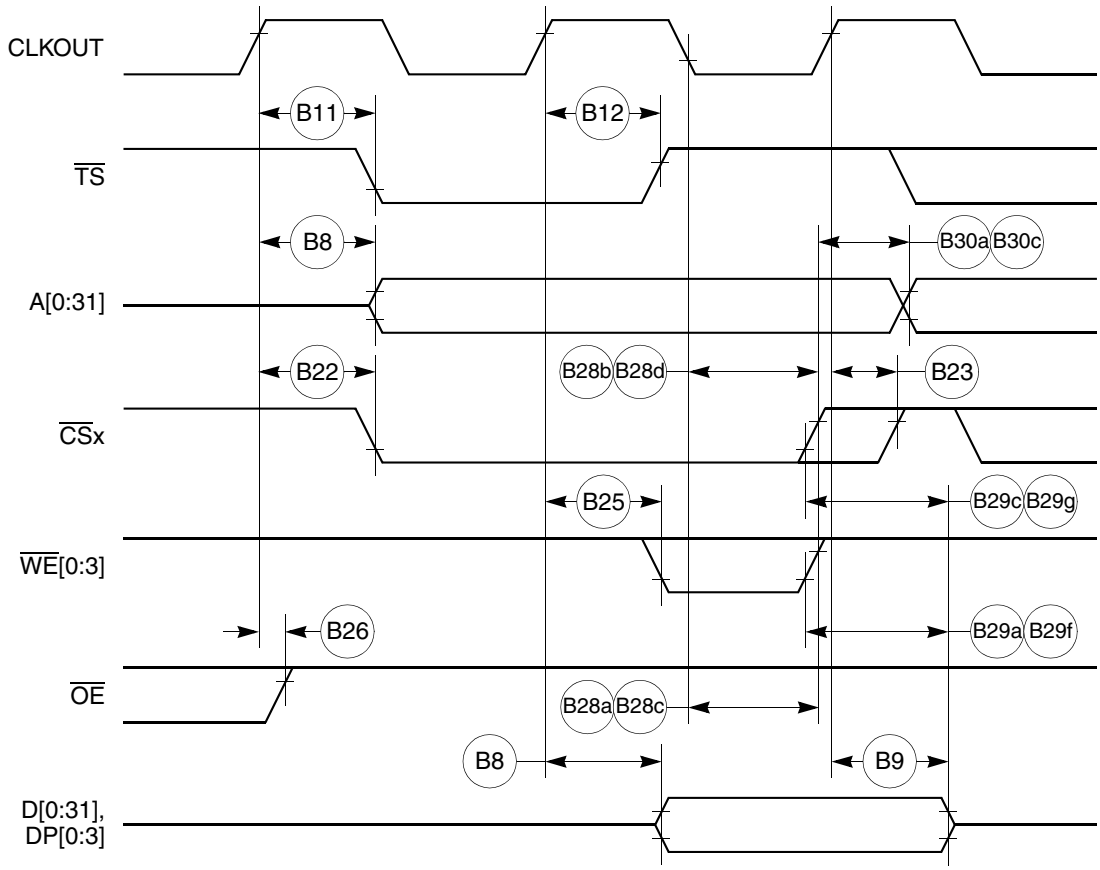

Figure 15. External Bus Write Timing (GPCM Controlled—TRLX = 0 or 1, CSNT = 1)

Figure 20 provides the timing for the synchronous external master access controlled by the GPCM.

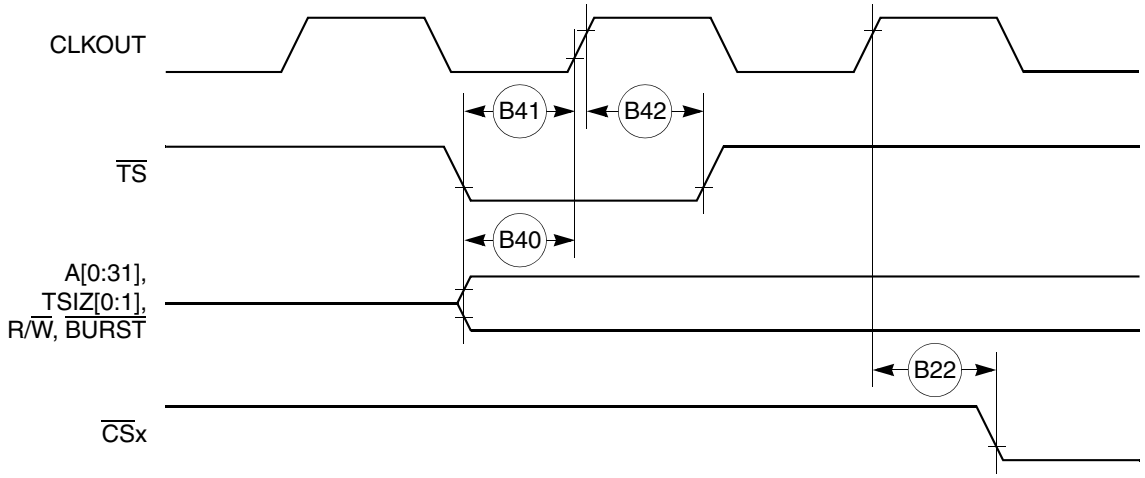

Figure 20. Synchronous External Master Access Timing (GPCM Handled ACS = 00)

Figure 21 provides the timing for the asynchronous external master memory access controlled by the GPCM.

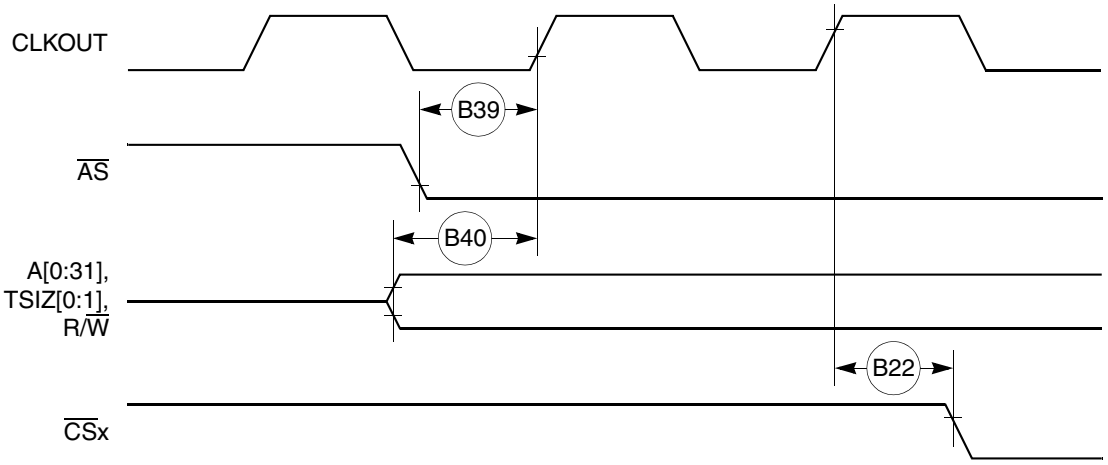

Figure 21. Asynchronous External Master Memory Access Timing (GPCM Controlled—ACS = 00)

Figure 22 provides the timing for the asynchronous external master control signals negation.

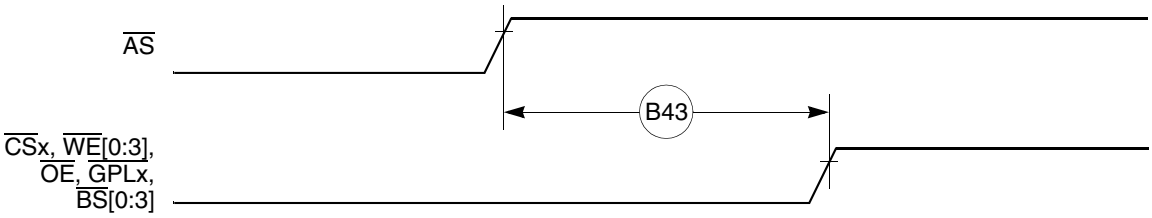

Figure 22. Asynchronous External Master—Control Signals Negation Timing

Table 9 shows the PCMCIA timing for the MPC860.

Table 9. PCMCIA Timing

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
P44	A(0:31), $\overline{\text{REG}}$ valid to PCMCIA Strobe asserted[1]	20.73	—	16.75	—	13.00	—	9.36	—	ns
P45	A(0:31), $\overline{\text{REG}}$ valid to ALE negation[1]	28.30	—	23.00	—	18.00	—	13.15	—	ns
P46	CLKOUT to $\overline{\text{REG}}$ valid	7.58	15.58	6.25	14.25	5.00	13.00	3.79	11.84	ns
P47	CLKOUT to $\overline{\text{REG}}$ invalid	8.58	—	7.25	—	6.00	—	4.84	—	ns
P48	CLKOUT to $\overline{\text{CE1}}$, $\overline{\text{CE2}}$ asserted	7.58	15.58	6.25	14.25	5.00	13.00	3.79	11.84	ns
P49	CLKOUT to $\overline{\text{CE1}}$, $\overline{\text{CE2}}$ negated	7.58	15.58	6.25	14.25	5.00	13.00	3.79	11.84	ns
P50	CLKOUT to $\overline{\text{PCOE}}$, $\overline{\text{IORD}}$, $\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ assert time	—	11.00		11.00	—	11.00	—	11.00	ns
P51	CLKOUT to $\overline{\text{PCOE}}$, $\overline{\text{IORD}}$, $\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ negate time	2.00	11.00	2.00	11.00	2.00	11.00	2.00	11.00	ns
P52	CLKOUT to ALE assert time	7.58	15.58	6.25	14.25	5.00	13.00	3.79	10.04	ns
P53	CLKOUT to ALE negate time	—	15.58		14.25	—	13.00	—	11.84	ns
P54	$\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ negated to D(0:31) invalid[1]	5.58	—	4.25	—	3.00	—	1.79	—	ns
P55	$\overline{\text{WAITA}}$ and $\overline{\text{WAITB}}$ valid to CLKOUT rising edge[1]	8.00	—	8.00	—	8.00	—	8.00	—	ns
P56	CLKOUT rising edge to $\overline{\text{WAITA}}$ and $\overline{\text{WAITB}}$ invalid[1]	2.00	—	2.00	—	2.00	—	2.00	—	ns

[1] PSST = 1. Otherwise add PSST times cycle time.
PSHT = 0. Otherwise add PSHT times cycle time.

These synchronous timings define when the $\overline{\text{WAITx}}$ signals are detected in order to freeze (or relieve) the PCMCIA current cycle. The $\overline{\text{WAITx}}$ assertion will be effective only if it is detected 2 cycles before the PSL timer expiration. See Chapter 16, “PCMCIA Interface,” in the *MPC860 PowerQUICC™ Family User’s Manual*.

Figure 26 provides the PCMCIA access cycle timing for the external bus write.

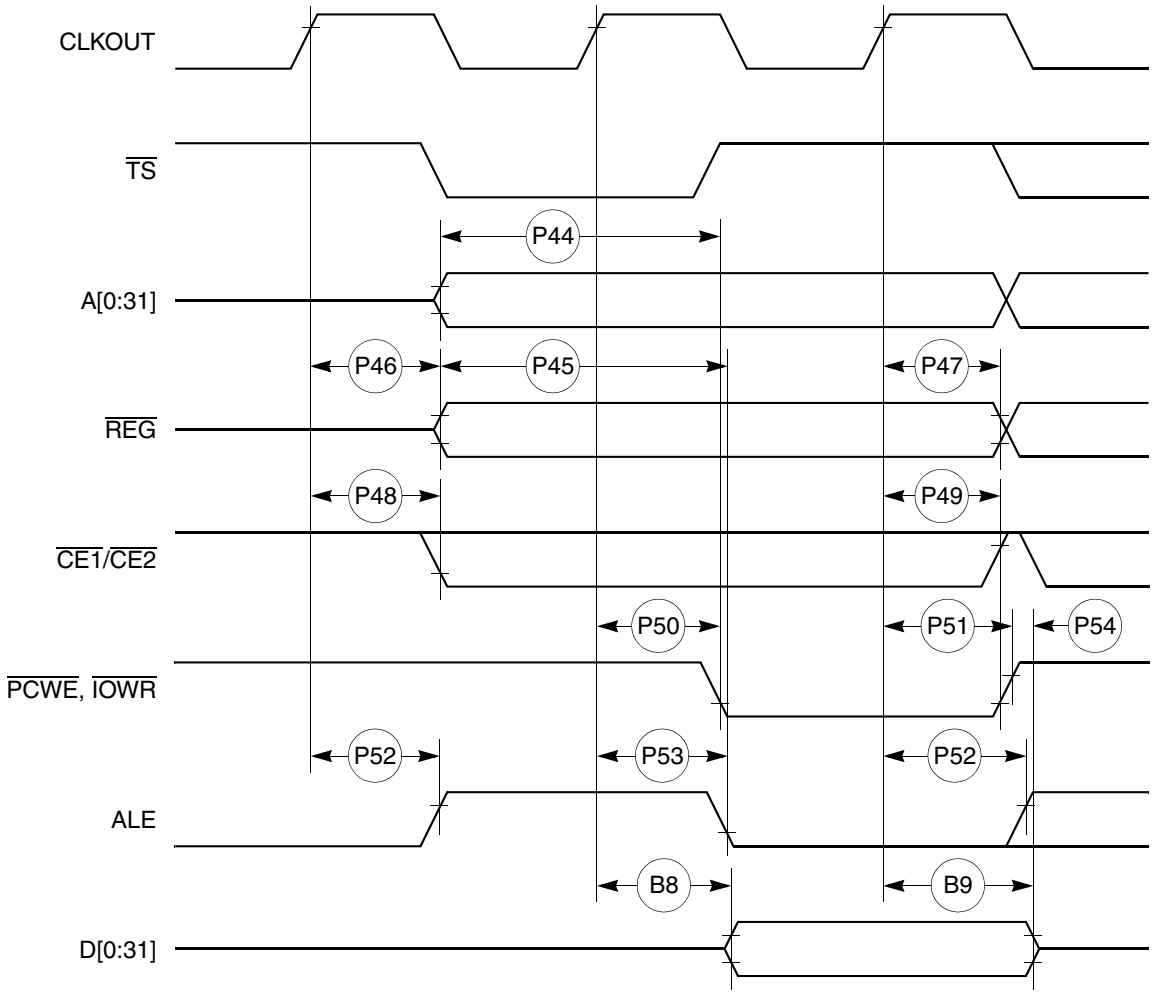

Figure 26. PCMCIA Access Cycle Timing External Bus Write

Figure 27 provides the PCMCIA WAIT signal detection timing.

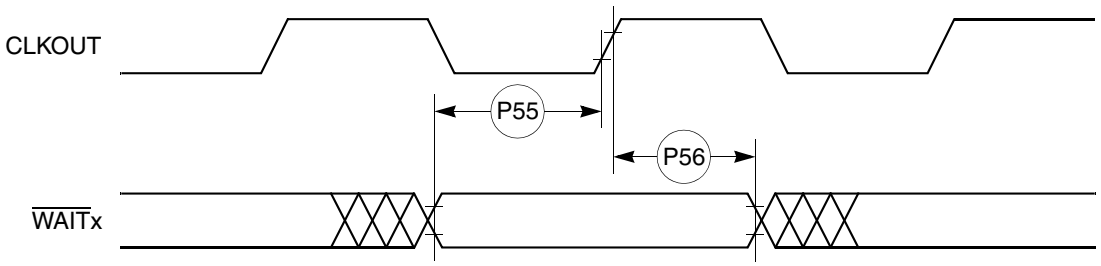

Figure 27. PCMCIA WAIT Signal Detection Timing

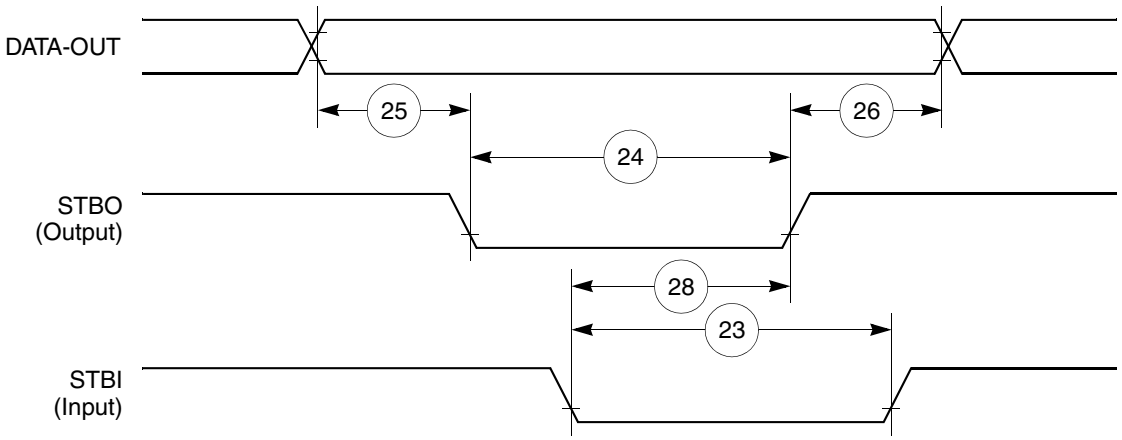

Figure 40. PIP Tx (Interlock Mode) Timing Diagram

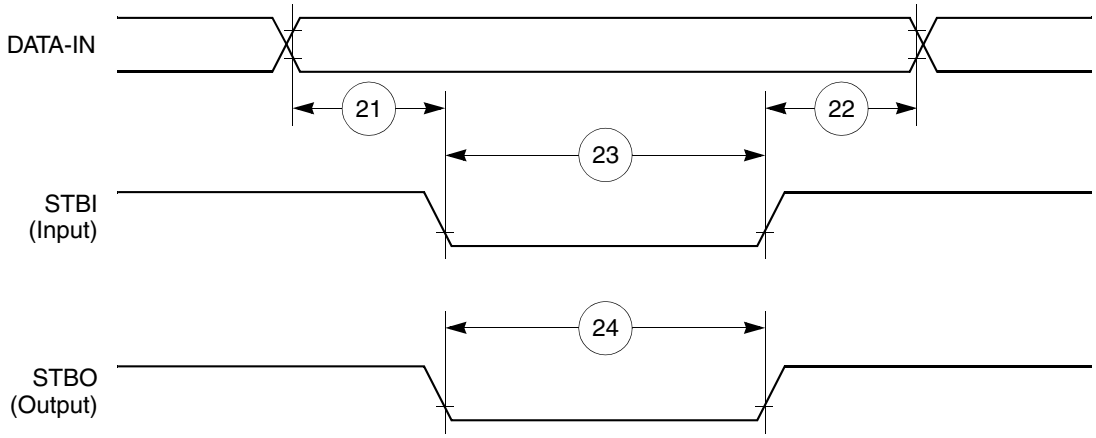

Figure 41. PIP Rx (Pulse Mode) Timing Diagram

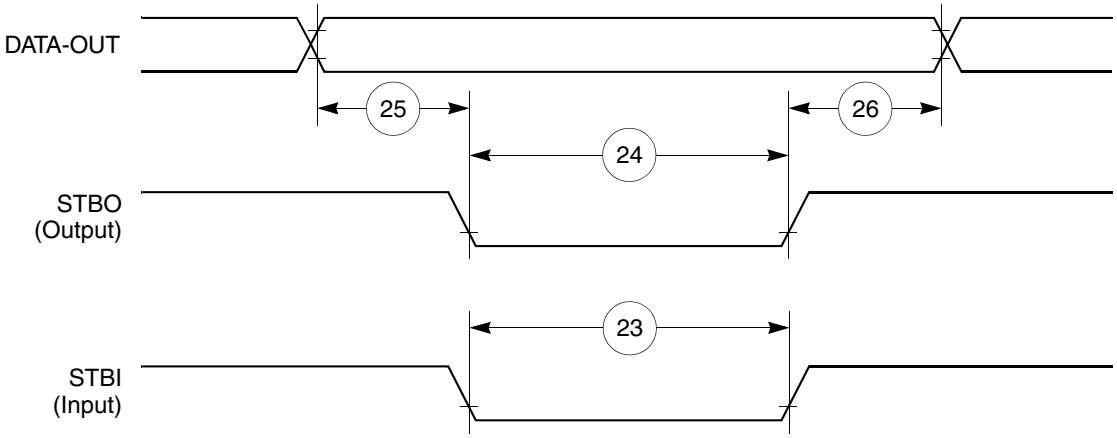

Figure 42. PIP TX (Pulse Mode) Timing Diagram

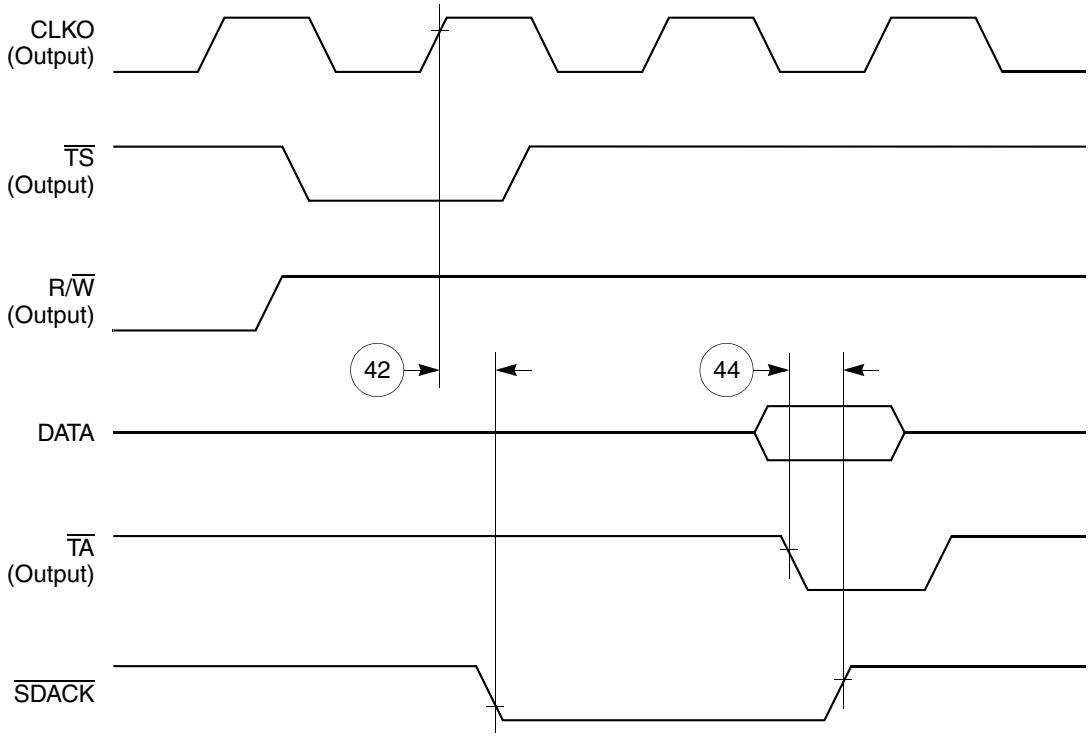

Figure 47. SDACK Timing Diagram—Peripheral Write, Internally-Generated TA

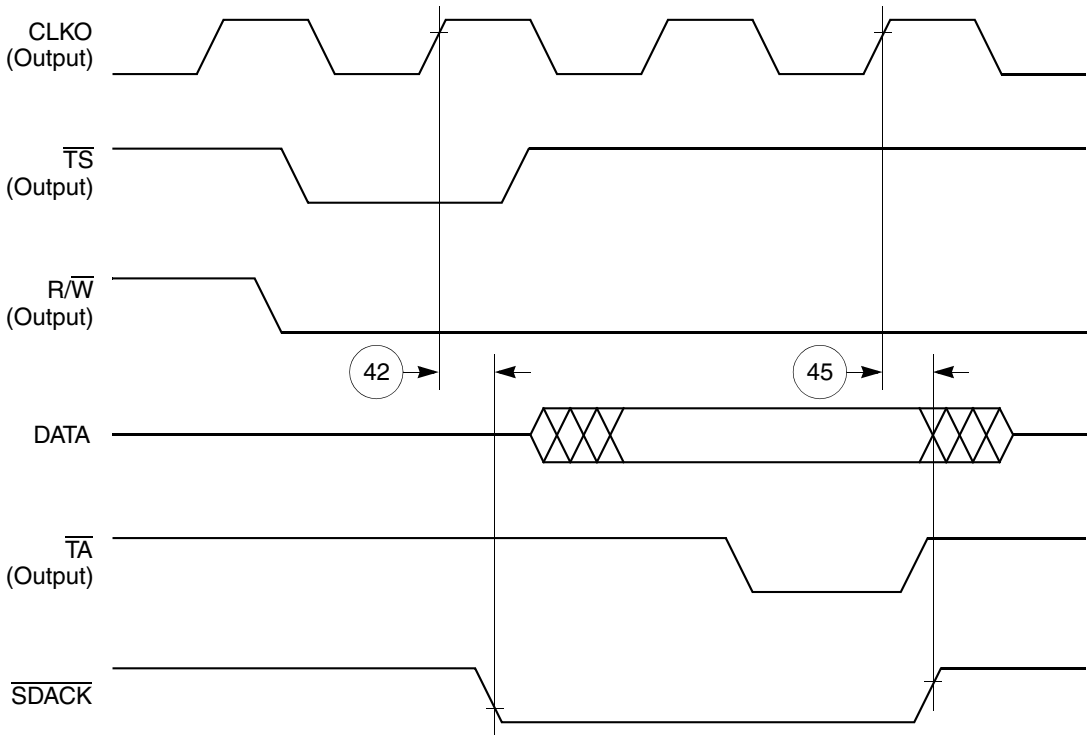

Figure 48. SDACK Timing Diagram—Peripheral Read, Internally-Generated TA

Table 22. Ethernet Timing (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
135	$\overline{\text{RSTRT}}$ active delay (from TCLK1 falling edge)	10	50	ns
136	$\overline{\text{RSTRT}}$ inactive delay (from TCLK1 falling edge)	10	50	ns
137	$\overline{\text{REJECT}}$ width low	1	—	CLK
138	CLKO1 low to $\overline{\text{SDACK}}$ asserted[2]	—	20	ns
139	CLKO1 low to $\overline{\text{SDACK}}$ negated[2]	—	20	ns

1 The ratios SYNCCLK/RCLK1 and SYNCCLK/TCLK1 must be greater than or equal to 2/1.
2 $\overline{\text{SDACK}}$ is asserted whenever the SDMA writes the incoming frame DA into memory.

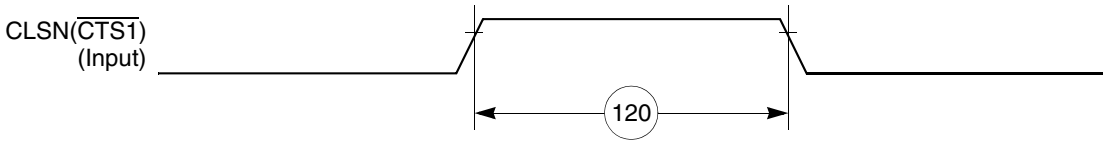

Figure 59. Ethernet Collision Timing Diagram

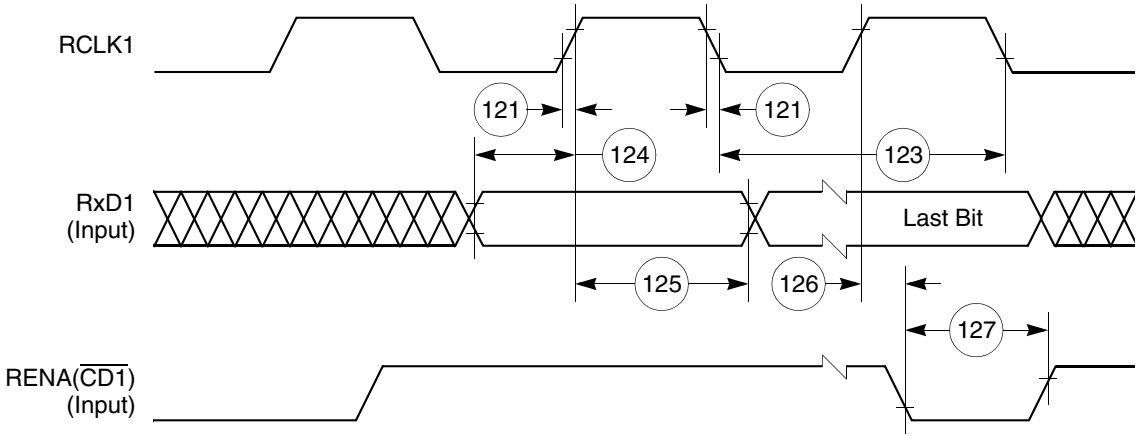

Figure 60. Ethernet Receive Timing Diagram

Figure 69 shows the I^2C bus timing.

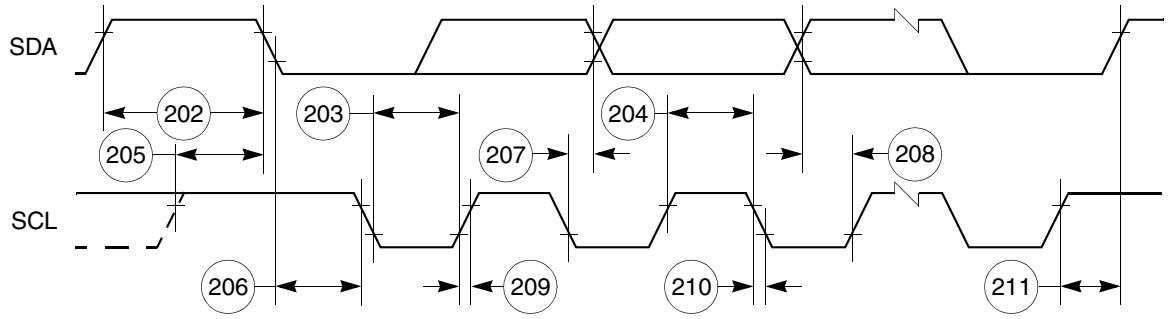

Figure 69. I^2C Bus Timing Diagram

12 UTOPIA AC Electrical Specifications

Table 28 shows the AC electrical specifications for the UTOPIA interface.

Table 28. UTOPIA AC Electrical Specifications

Num	Signal Characteristic	Direction	Min	Max	Unit
U1	UtpClk rise/fall time (Internal clock option)	Output	—	3.5	ns
	Duty cycle		50	50	%
	Frequency		—	50	MHz
U1a	UtpClk rise/fall time (external clock option)	Input	—	3.5	ns
	Duty cycle		40	60	%
	Frequency		—	50	MHz
U2	$\overline{\text{RxEnb}}$ and $\overline{\text{TxEnb}}$ active delay	Output	2	16	ns
U3	UTPB, SOC, Rxclav and Txclav setup time	Input	8	—	ns
U4	UTPB, SOC, Rxclav and Txclav hold time	Input	1	—	ns
U5	UTPB, SOC active delay (and PHREQ and PHSEL active delay in MPHY mode)	Output	2	16	ns

Table 34 identifies the packages and operating frequencies available for the MPC860.

Table 34. MPC860 Family Package/Frequency Availability

Package Type	Freq. (MHz) / Temp. (Tj)	Package	Order Number
Ball grid array ZP suffix—leaded ZQ suffix—leaded VR suffix—lead-free	50 0° to 95°C	ZP/ZQ[1]	MPC855TZQ50D4 MPC860DEZQ50D4 MPC860DTZQ50D4 MPC860ENZQ50D4 MPC860SRZQ50D4 MPC860TZQ50D4 MPC860DPZQ50D4 MPC860PZQ50D4
		Tape and Reel	MPC855TZQ50D4R2 MPC860DEZQ50D4R2 MPC860ENZQ50D4R2 MPC860SRZQ50D4R2 MPC860TZQ50D4R2 MPC860DPZQ50D4R2 MPC855TVR50D4R2 MPC860ENVR50D4R2 MPC860SRVR50D4R2 MPC860TVR50D4R2
		VR	MPC855TVR50D4 MPC860DEVR50D4 MPC860DPVR50D4 MPC860DTVR50D4 MPC860ENVR50D4 MPC860PVR50D4 MPC860SRVR50D4 MPC860TVR50D4
	66 0° to 95°C	ZP/ZQ[1]	MPC855TZQ66D4 MPC860DEZQ66D4 MPC860DTZQ66D4 MPC860ENZQ66D4 MPC860SRZQ66D4 MPC860TZQ66D4 MPC860DPZQ66D4 MPC860PZQ66D4
		Tape and Reel	MPC860SRZQ66D4R2 MPC860PZQ66D4R2
		VR	MPC855TVR66D4 MPC860DEVR66D4 MPC860DPVR66D4 MPC860DTVR66D4 MPC860ENVR66D4 MPC860PVR66D4 MPC860SRVR66D4 MPC860TVR66D4

Table 34. MPC860 Family Package/Frequency Availability (continued)

Package Type	Freq. (MHz) / Temp. (Tj)	Package	Order Number
Ball grid array *(continued)* ZP suffix—leaded ZQ suffix—leaded VR suffix—lead-free	80 0° to 95°C	ZP/ZQ[1]	MPC855TZQ80D4 MPC860DEZQ80D4 MPC860DTZQ80D4 MPC860ENZQ80D4 MPC860SRZQ80D4 MPC860TZQ80D4 MPC860DPZQ80D4 MPC860PZQ80D4
		Tape and Reel	MPC860PZQ80D4R2 MPC860PVR80D4R2
		VR	MPC855TVR80D4 MPC860DEVR80D4 MPC860DPVR80D4 MPC860ENVR80D4 MPC860PVR80D4 MPC860SRVR80D4 MPC860TVR80D4
Ball grid array (CZP suffix) CZP suffix—leaded CZQ suffix—leaded CVR suffix—lead-free	50 –40° to 95°C	ZP/ZQ[1]	MPC855TCZQ50D4 MPC855TCVR50D4 MPC860DECZQ50D4 MPC860DTCZQ50D4 MPC860ENCZQ50D4 MPC860SRCZQ50D4 MPC860TCZQ50D4 MPC860DPCZQ50D4 MPC860PCZQ50D4
		Tape and Reel	MPC855TCZQ50D4R2 MC860ENCVR50D4R2
		CVR	MPC860DECVR50D4 MPC860DTCVR50D4 MPC860ENCVR50D4 MPC860PCVR50D4 MPC860SRCVR50D4 MPC860TCVR50D4
	66 –40° to 95°C	ZP/ZQ[1]	MPC855TCZQ66D4 MPC855TCVR66D4 MPC860ENCZQ66D4 MPC860SRCZQ66D4 MPC860TCZQ66D4 MPC860DPCZQ66D4 MPC860PCZQ66D4
		CVR	MPC860DTCVR66D4 MPC860ENCVR66D4 MPC860PCVR66D4 MPC860SRCVR66D4 MPC860TCVR66D4

[1] The ZP package is no longer recommended for use. The ZQ package replaces the ZP package.

14.2 Pin Assignments

Figure 76 shows the top view pinout of the PBGA package. For additional information, see the *MPC860 PowerQUICC User's Manual*, or the *MPC855T User's Manual*.

NOTE: This is the top view of the device.

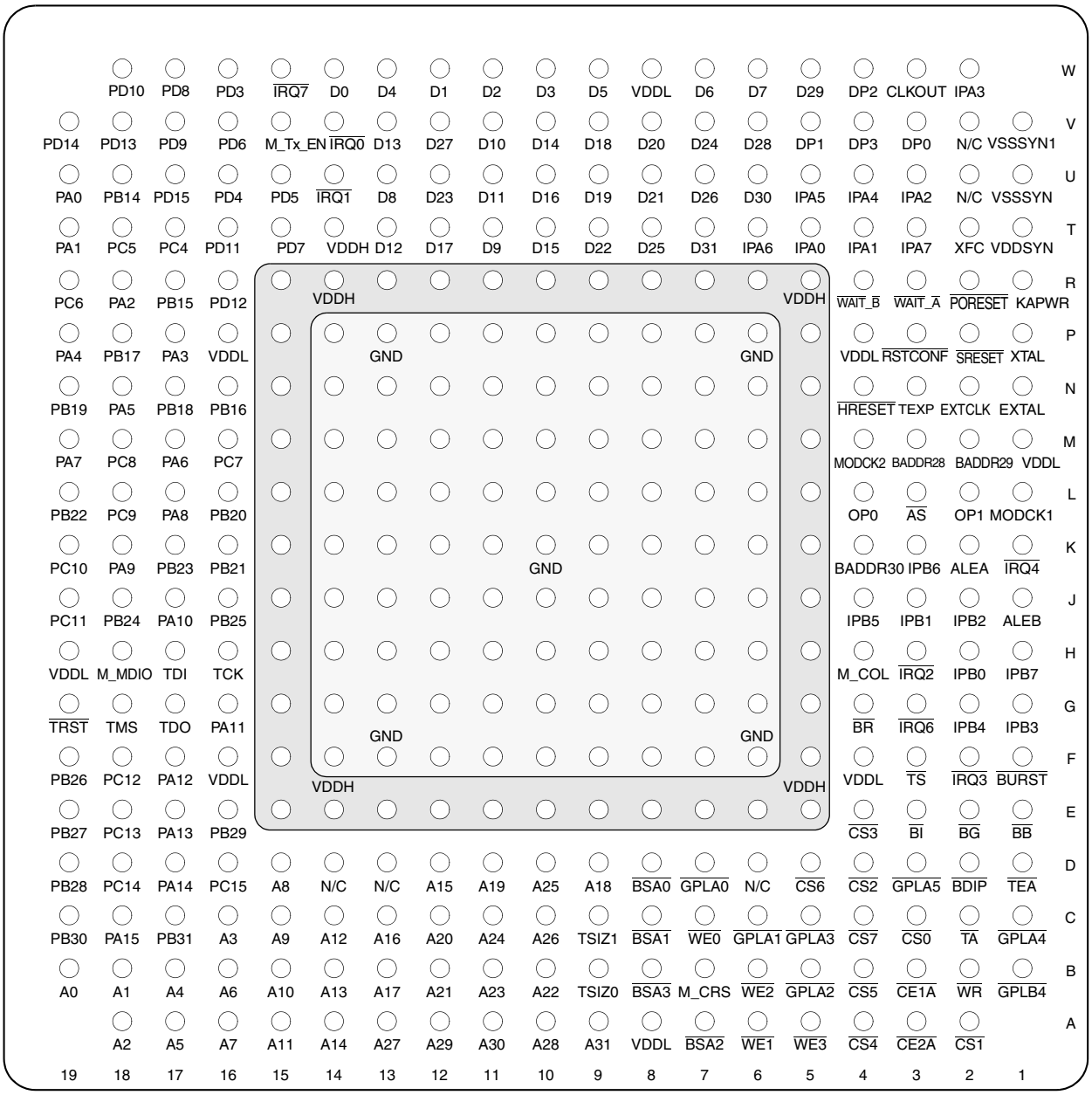

Figure 76. Pinout of the PBGA Package