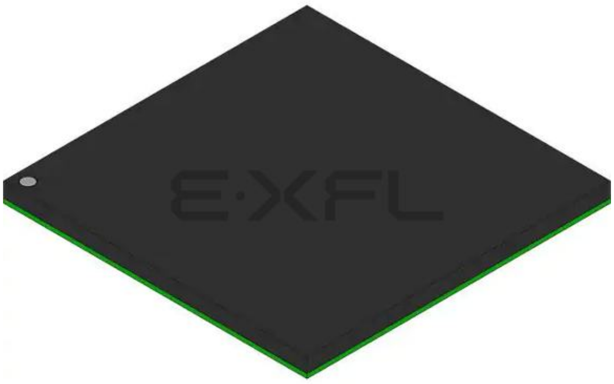

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	50MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (4)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 95°C (TA)
Security Features	-
Package / Case	357-BBGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc860enzq50d4

1 Overview

The MPC860 power quad integrated communications controller (PowerQUICC™) is a versatile one-chip integrated microprocessor and peripheral combination designed for a variety of controller applications. It particularly excels in communications and networking systems. The PowerQUICC unit is referred to as the MPC860 in this hardware specification.

The MPC860 implements Power Architecture™ technology and contains a superset of Freescale's MC68360 quad integrated communications controller (QUICC), referred to here as the QUICC, RISC communications proccessor module (CPM). The CPU on the MPC860 is a 32-bit core built on Power Architecture technology that incorporates memory management units (MMUs) and instruction and data caches.. The CPM from the MC68360 QUICC has been enhanced by the addition of the inter-integrated controller (I^2C) channel. The memory controller has been enhanced, enabling the MPC860 to support any type of memory, including high-performance memories and new types of DRAMs. A PCMCIA socket controller supports up to two sockets. A real-time clock has also been integrated.

Table 1 shows the functionality supported by the MPC860 family.

Table 1. MPC860 Family Functionality

Part	Cache (Kbytes)		Ethernet		ATM	SCC	Reference[1]
	Instruction Cache	Data Cache	10T	10/100			
MPC860DE	4	4	Up to 2	—	—	2	1
MPC860DT	4	4	Up to 2	1	Yes	2	1
MPC860DP	16	8	Up to 2	1	Yes	2	1
MPC860EN	4	4	Up to 4	—	—	4	1
MPC860SR	4	4	Up to 4	—	Yes	4	1
MPC860T	4	4	Up to 4	1	Yes	4	1
MPC860P	16	8	Up to 4	1	Yes	4	1
MPC855T	4	4	1	1	Yes	1	2

[1] Supporting documentation for these devices refers to the following:
1. MPC860 PowerQUICC Family User's Manual (MPC860UM, Rev. 3)
2. MPC855T User's Manual (MPC855TUM, Rev. 1)

Table 4 shows the thermal characteristics for the MPC860.

Table 4. MPC860 Thermal Resistance Data

Rating	Environment		Symbol	ZP MPC860P	ZQ / VR MPC860P	Unit
Mold Compound Thickness				0.85	1.15	mm
Junction-to-ambient [1]	Natural convection	Single-layer board (1s)	$R_{\theta JA}$[2]	34	34	°C/W
		Four-layer board (2s2p)	$R_{\theta JMA}$[3]	22	22	
	Airflow (200 ft/min)	Single-layer board (1s)	$R_{\theta JMA}$[3]	27	27	
		Four-layer board (2s2p)	$R_{\theta JMA}$[3]	18	18	
Junction-to-board [4]			$R_{\theta JB}$	14	13	
Junction-to-case [5]			$R_{\theta JC}$	6	8	
Junction-to-package top [6]	Natural convection		Ψ_{JT}	2	2	

1 Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.

2 Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature. For exposed pad packages where the pad would be expected to be soldered, junction-to-case thermal resistance is a simulated value from the junction to the exposed pad without contact resistance.

6 Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2.

Figure 7 provides the timing for the synchronous input signals.

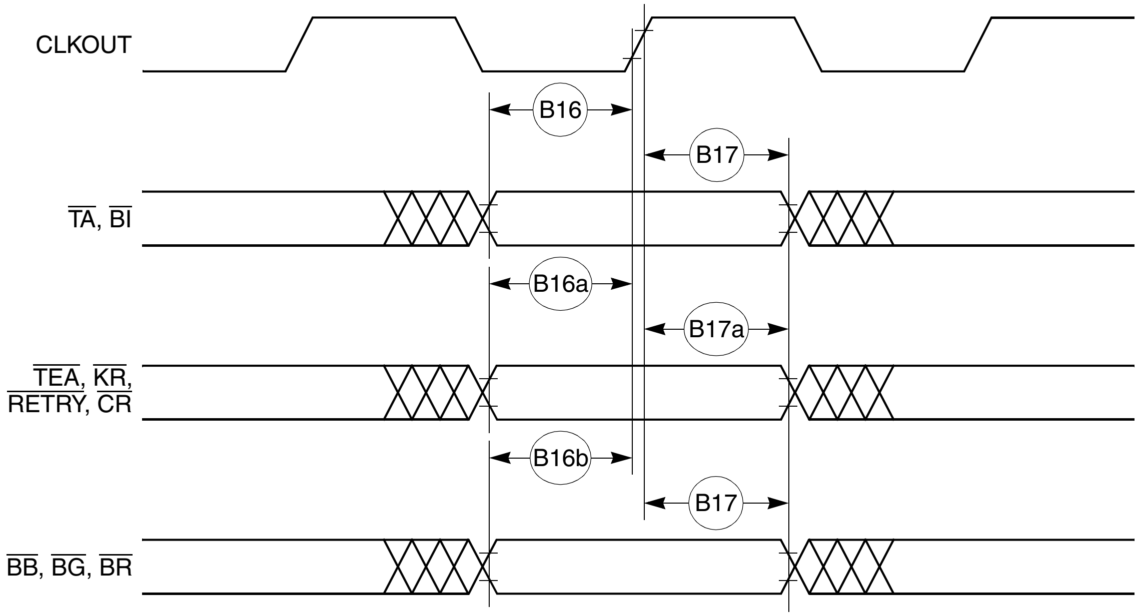


Figure 7. Synchronous Input Signals Timing

Figure 8 provides normal case timing for input data. It also applies to normal read accesses under the control of the UPM in the memory controller.

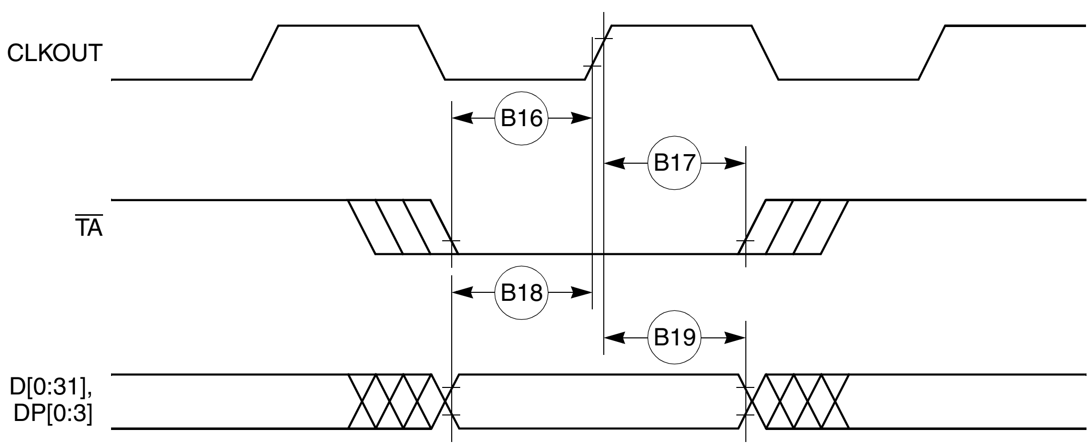


Figure 8. Input Data Timing in Normal Case

Figure 9 provides the timing for the input data controlled by the UPM for data beats where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

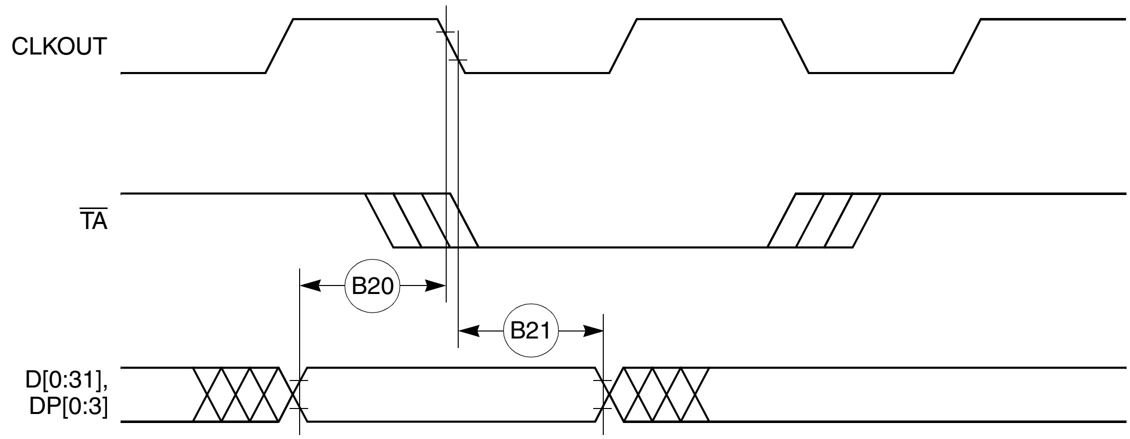


Figure 9. Input Data Timing when Controlled by UPM in the Memory Controller and DLT3 = 1

Figure 10 through Figure 13 provide the timing for the external bus read controlled by various GPCM factors.

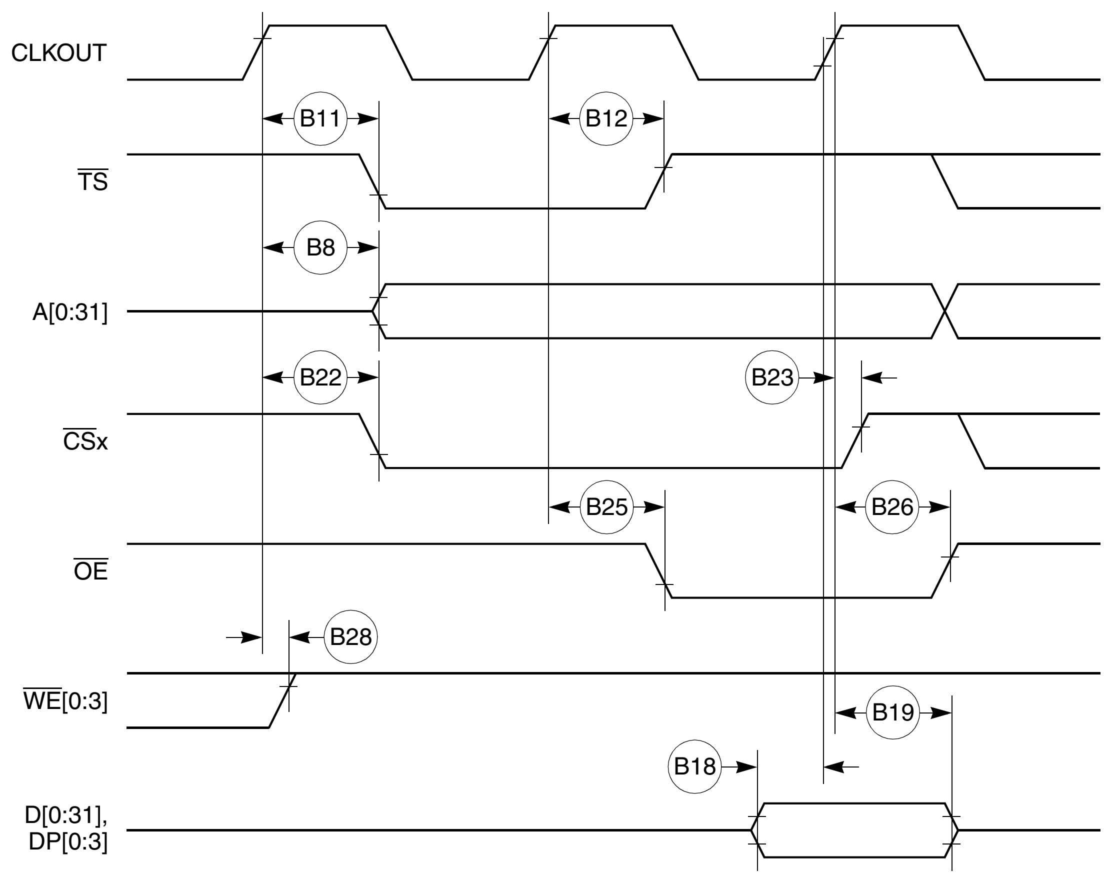


Figure 10. External Bus Read Timing (GPCM Controlled—ACS = 00)

Figure 14 through Figure 16 provide the timing for the external bus write controlled by various GPCM factors.

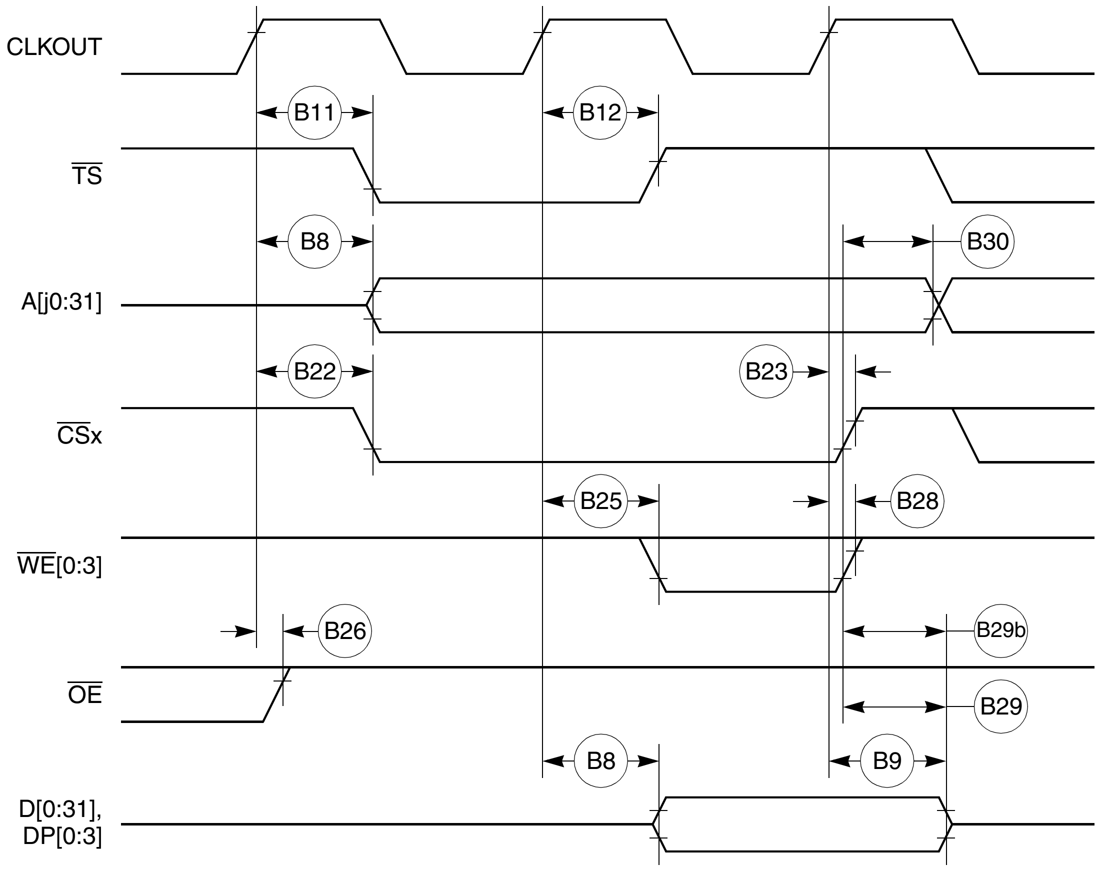


Figure 14. External Bus Write Timing (GPCM Controlled—TRLX = 0 or 1, CSNT = 0)

Figure 17 provides the timing for the external bus controlled by the UPM.

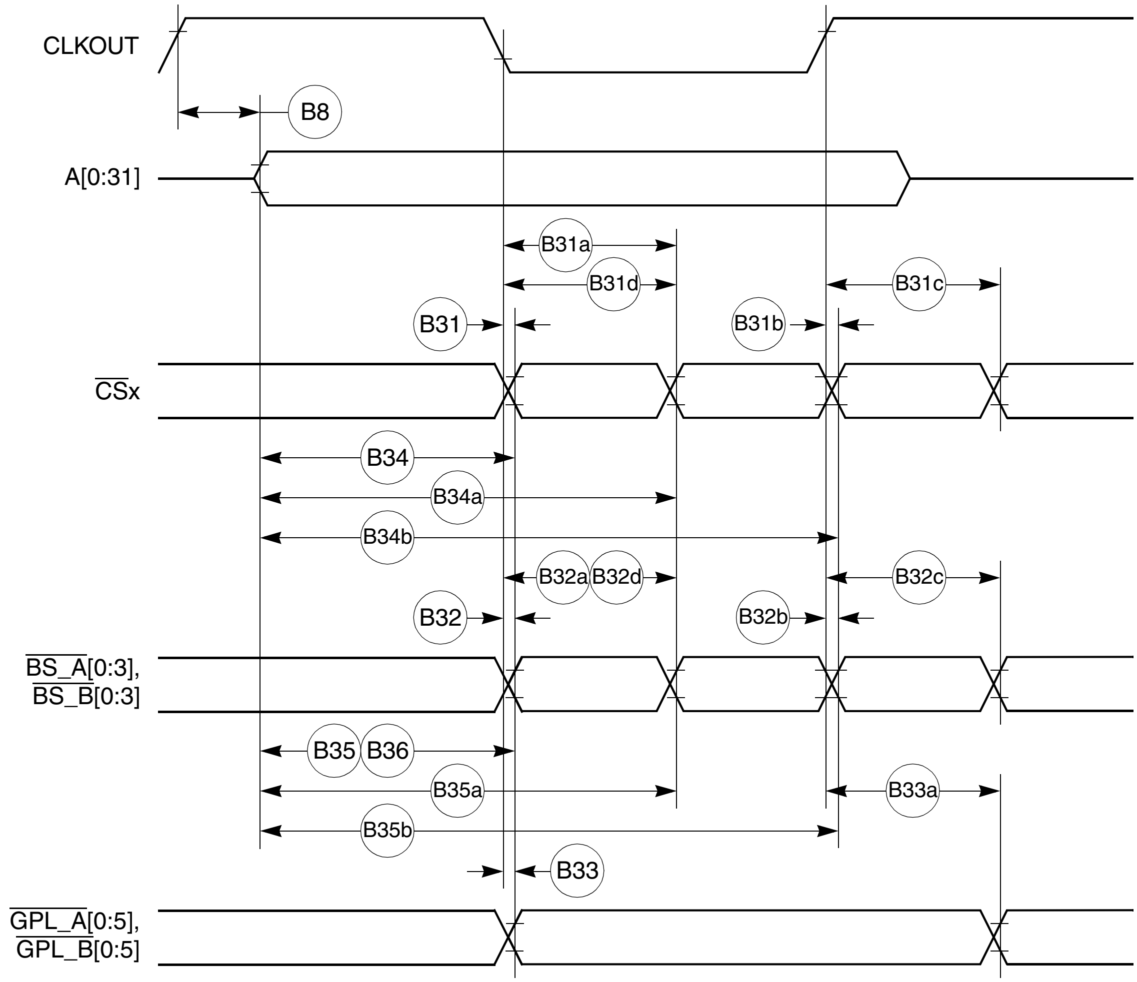


Figure 17. External Bus Timing (UPM Controlled Signals)

Table 8 provides interrupt timing for the MPC860.

Table 8. Interrupt Timing

Num	Characteristic[1]	All Frequencies		Unit
		Min	Max	
I39	$\overline{IRQ}$x valid to CLKOUT rising edge (setup time)	6.00	—	ns
I40	$\overline{IRQ}$x hold time after CLKOUT	2.00	—	ns
I41	$\overline{IRQ}$x pulse width low	3.00	—	ns
I42	$\overline{IRQ}$x pulse width high	3.00	—	ns
I43	$\overline{IRQ}$x edge-to-edge time	$4 \times T_{CLOCKOUT}$	—	—

[1] The timings I39 and I40 describe the testing conditions under which the $\overline{IRQ}$ lines are tested when being defined as level-sensitive. The $\overline{IRQ}$ lines are synchronized internally and do not have to be asserted or negated with reference to the CLKOUT.
The timings I41, I42, and I43 are specified to allow the correct function of the $\overline{IRQ}$ lines detection circuitry and have no direct relation with the total system interrupt latency that the MPC860 is able to support.

Figure 23 provides the interrupt detection timing for the external level-sensitive lines.

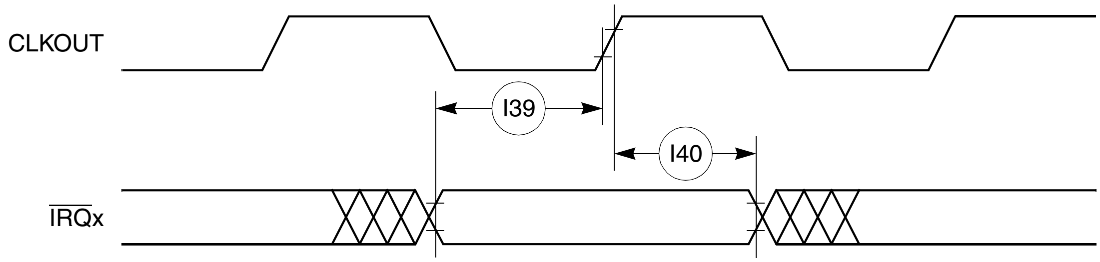


Figure 23. Interrupt Detection Timing for External Level Sensitive Lines

Figure 24 provides the interrupt detection timing for the external edge-sensitive lines.

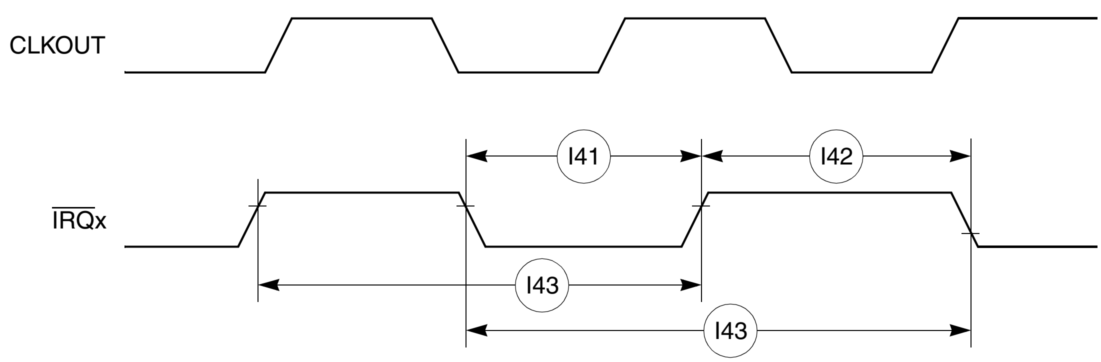


Figure 24. Interrupt Detection Timing for External Edge Sensitive Lines

Table 9 shows the PCMCIA timing for the MPC860.

Table 9. PCMCIA Timing

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
P44	A(0:31), $\overline{REG}$ valid to PCMCIA Strobe asserted[1]	20.73	—	16.75	—	13.00	—	9.36	—	ns
P45	A(0:31), $\overline{REG}$ valid to ALE negation[1]	28.30	—	23.00	—	18.00	—	13.15	—	ns
P46	CLKOUT to $\overline{REG}$ valid	7.58	15.58	6.25	14.25	5.00	13.00	3.79	11.84	ns
P47	CLKOUT to $\overline{REG}$ invalid	8.58	—	7.25	—	6.00	—	4.84	—	ns
P48	CLKOUT to $\overline{CE1}$, $\overline{CE2}$ asserted	7.58	15.58	6.25	14.25	5.00	13.00	3.79	11.84	ns
P49	CLKOUT to $\overline{CE1}$, $\overline{CE2}$ negated	7.58	15.58	6.25	14.25	5.00	13.00	3.79	11.84	ns
P50	CLKOUT to $\overline{PCOE}$, $\overline{IORD}$, $\overline{PCWE}$, $\overline{IOWR}$ assert time	—	11.00		11.00	—	11.00	—	11.00	ns
P51	CLKOUT to $\overline{PCOE}$, $\overline{IORD}$, $\overline{PCWE}$, $\overline{IOWR}$ negate time	2.00	11.00	2.00	11.00	2.00	11.00	2.00	11.00	ns
P52	CLKOUT to ALE assert time	7.58	15.58	6.25	14.25	5.00	13.00	3.79	10.04	ns
P53	CLKOUT to ALE negate time	—	15.58		14.25	—	13.00	—	11.84	ns
P54	$\overline{PCWE}$, $\overline{IOWR}$ negated to D(0:31) invalid[1]	5.58	—	4.25	—	3.00	—	1.79	—	ns
P55	$\overline{WAITA}$ and $\overline{WAITB}$ valid to CLKOUT rising edge[1]	8.00	—	8.00	—	8.00	—	8.00	—	ns
P56	CLKOUT rising edge to $\overline{WAITA}$ and $\overline{WAITB}$ invalid[1]	2.00	—	2.00	—	2.00	—	2.00	—	ns

[1] PSST = 1. Otherwise add PSST times cycle time.
PSHT = 0. Otherwise add PSHT times cycle time.

These synchronous timings define when the $\overline{WAITx}$ signals are detected in order to freeze (or relieve) the PCMCIA current cycle. The $\overline{WAITx}$ assertion will be effective only if it is detected 2 cycles before the PSL timer expiration. See Chapter 16, “PCMCIA Interface,” in the *MPC860 PowerQUICC™ Family User’s Manual*.

Figure 34 provides the reset timing for the debug port configuration.

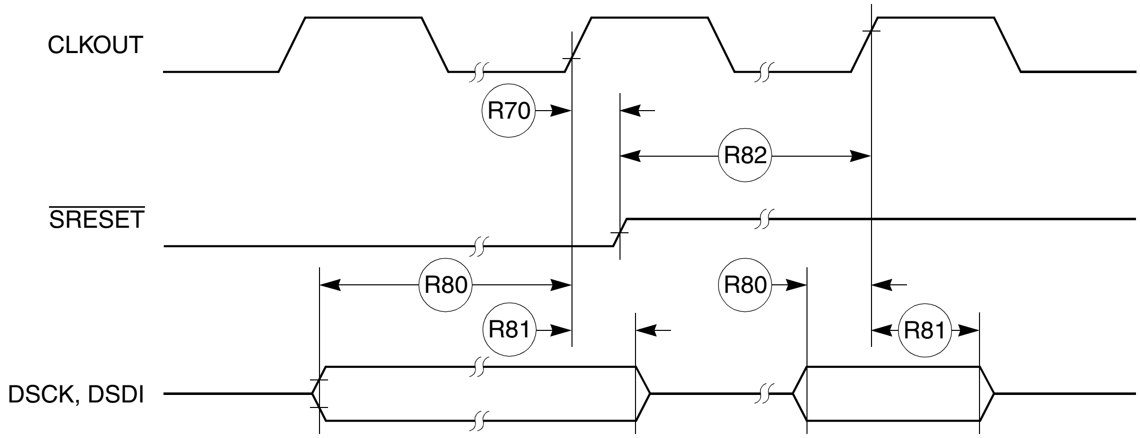


Figure 34. Reset Timing—Debug Port Configuration

10 IEEE 1149.1 Electrical Specifications

Table 13 provides the JTAG timings for the MPC860 shown in Figure 35 through Figure 38.

Table 13. JTAG Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
J82	TCK cycle time	100.00	—	ns
J83	TCK clock pulse width measured at 1.5 V	40.00	—	ns
J84	TCK rise and fall times	0.00	10.00	ns
J85	TMS, TDI data setup time	5.00	—	ns
J86	TMS, TDI data hold time	25.00	—	ns
J87	TCK low to TDO data valid	—	27.00	ns
J88	TCK low to TDO data invalid	0.00	—	ns
J89	TCK low to TDO high impedance	—	20.00	ns
J90	$\overline{\text{TRST}}$ assert time	100.00	—	ns
J91	$\overline{\text{TRST}}$ setup time to TCK low	40.00	—	ns
J92	TCK falling edge to output valid	—	50.00	ns
J93	TCK falling edge to output valid out of high impedance	—	50.00	ns
J94	TCK falling edge to output high impedance	—	50.00	ns
J95	Boundary scan input valid to TCK rising edge	50.00	—	ns
J96	TCK rising edge to boundary scan input invalid	50.00	—	ns

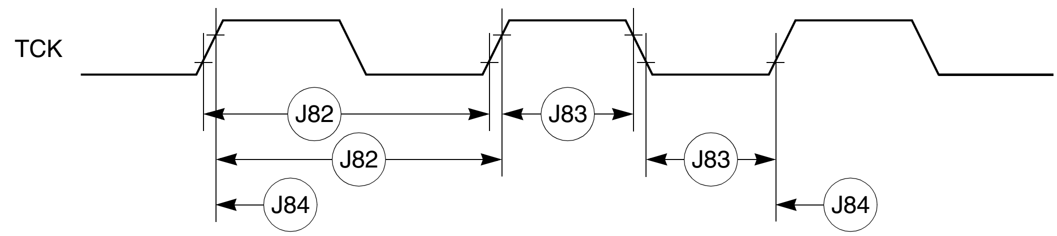


Figure 35. JTAG Test Clock Input Timing

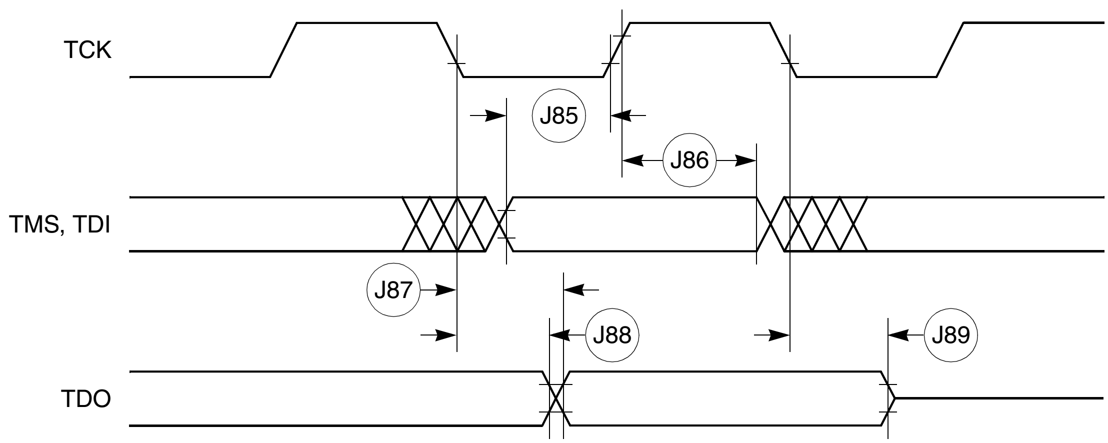


Figure 36. JTAG Test Access Port Timing Diagram

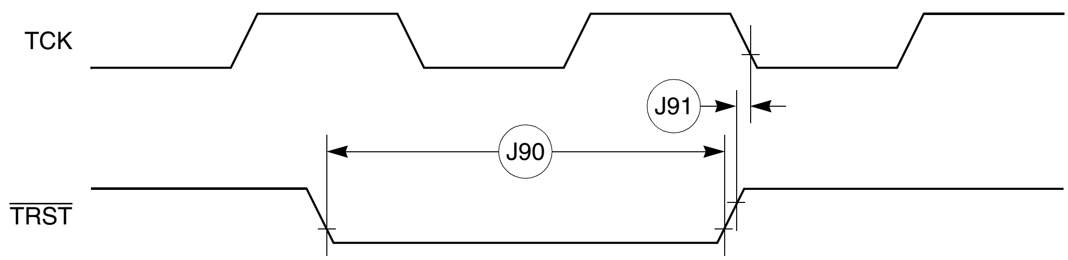


Figure 37. JTAG $\overline{\textbf{TRST}}$ Timing Diagram

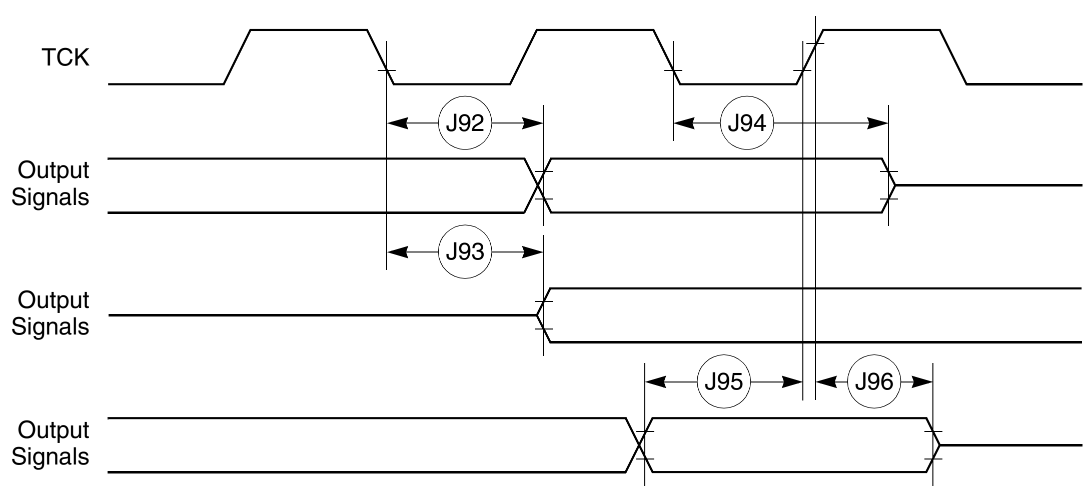


Figure 38. Boundary Scan (JTAG) Timing Diagram

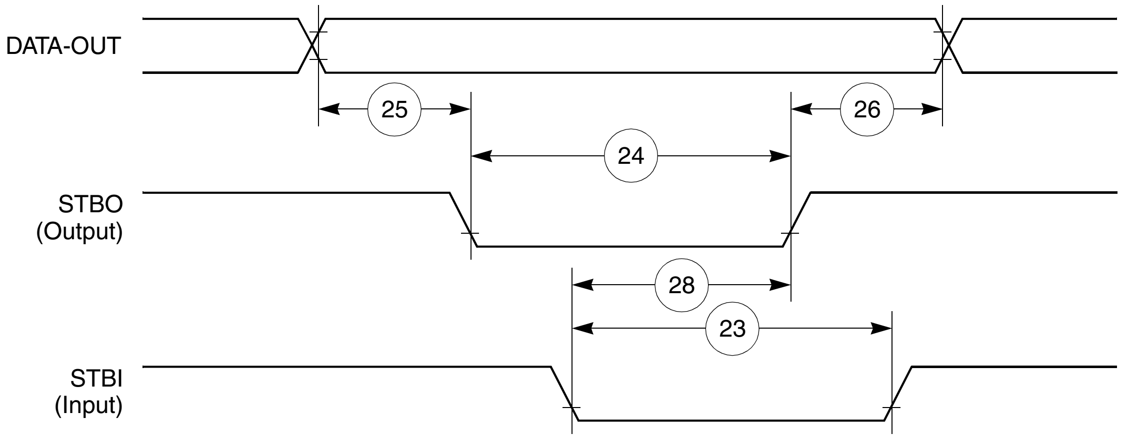


Figure 40. PIP Tx (Interlock Mode) Timing Diagram

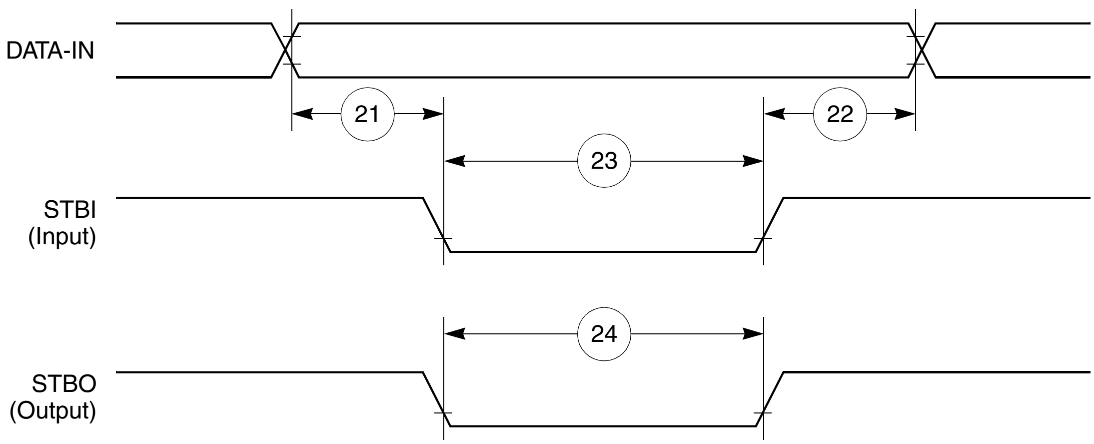


Figure 41. PIP Rx (Pulse Mode) Timing Diagram

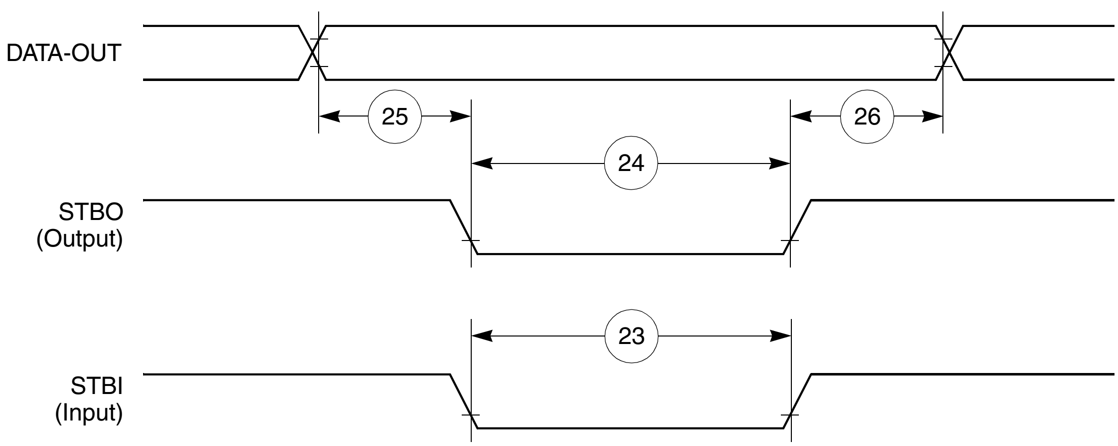


Figure 42. PIP TX (Pulse Mode) Timing Diagram

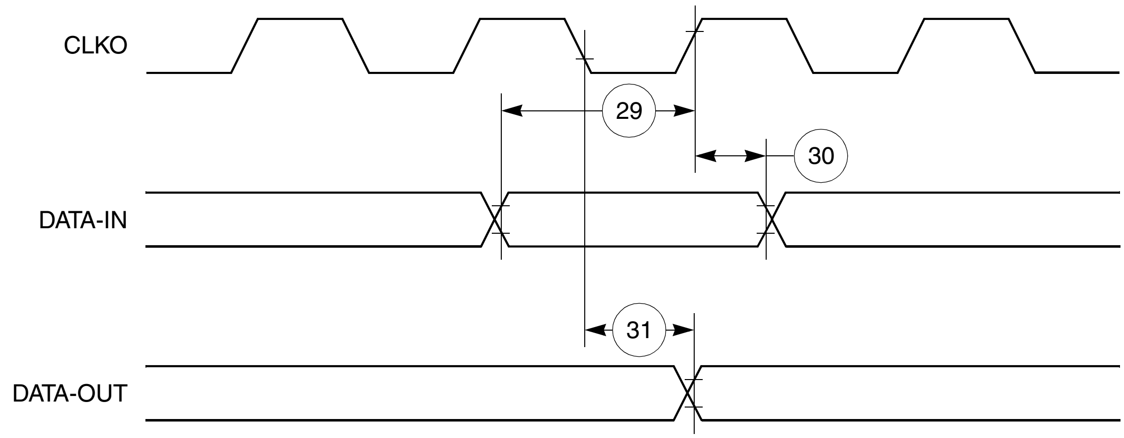


Figure 43. Parallel I/O Data-In/Data-Out Timing Diagram

11.2 Port C Interrupt AC Electrical Specifications

Table 15 provides the timings for port C interrupts.

Table 15. Port C Interrupt Timing

Num	Characteristic	≥ 33.34 MHz[1]		Unit
		Min	Max	
35	Port C interrupt pulse width low (edge-triggered mode)	55	—	ns
36	Port C interrupt minimum time between active edges	55	—	ns

[1] External bus frequency of greater than or equal to 33.34 MHz.

Figure 44 shows the port C interrupt detection timing.

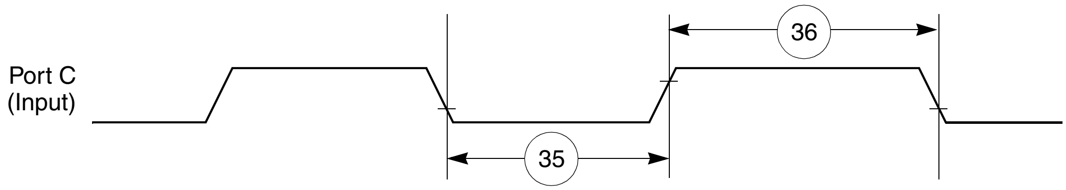


Figure 44. Port C Interrupt Detection Timing

11.3 IDMA Controller AC Electrical Specifications

Table 16 provides the IDMA controller timings as shown in Figure 45 through Figure 48.

Table 16. IDMA Controller Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
40	$\overline{\text{DREQ}}$ setup time to clock high	7	—	ns
41	$\overline{\text{DREQ}}$ hold time from clock high	3	—	ns

Figure 56 through Figure 58 show the NMSI timings.

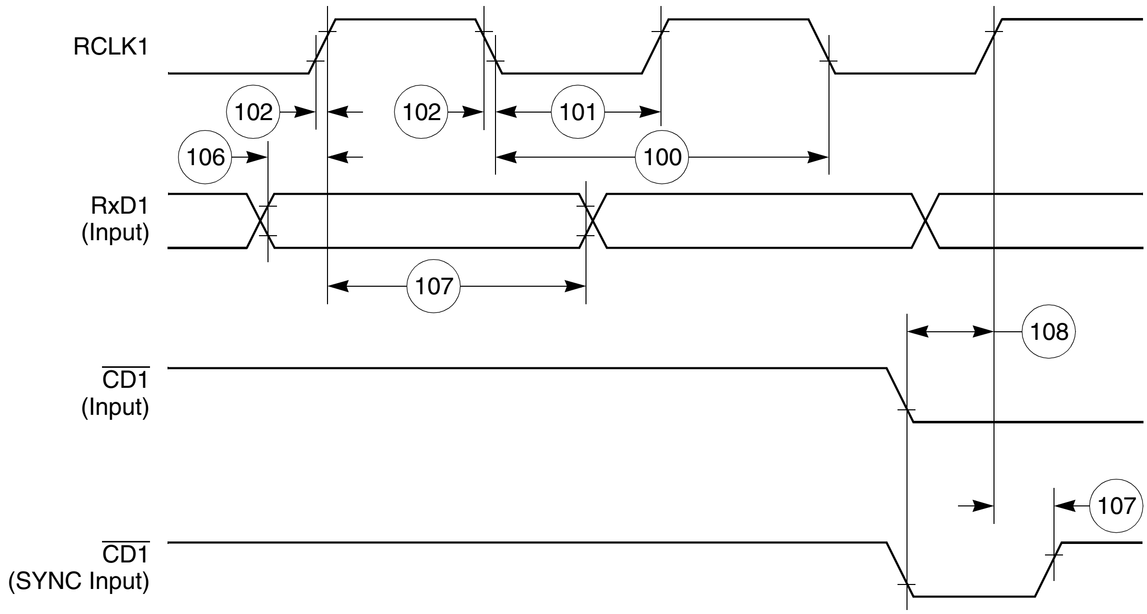


Figure 56. SCC NMSI Receive Timing Diagram

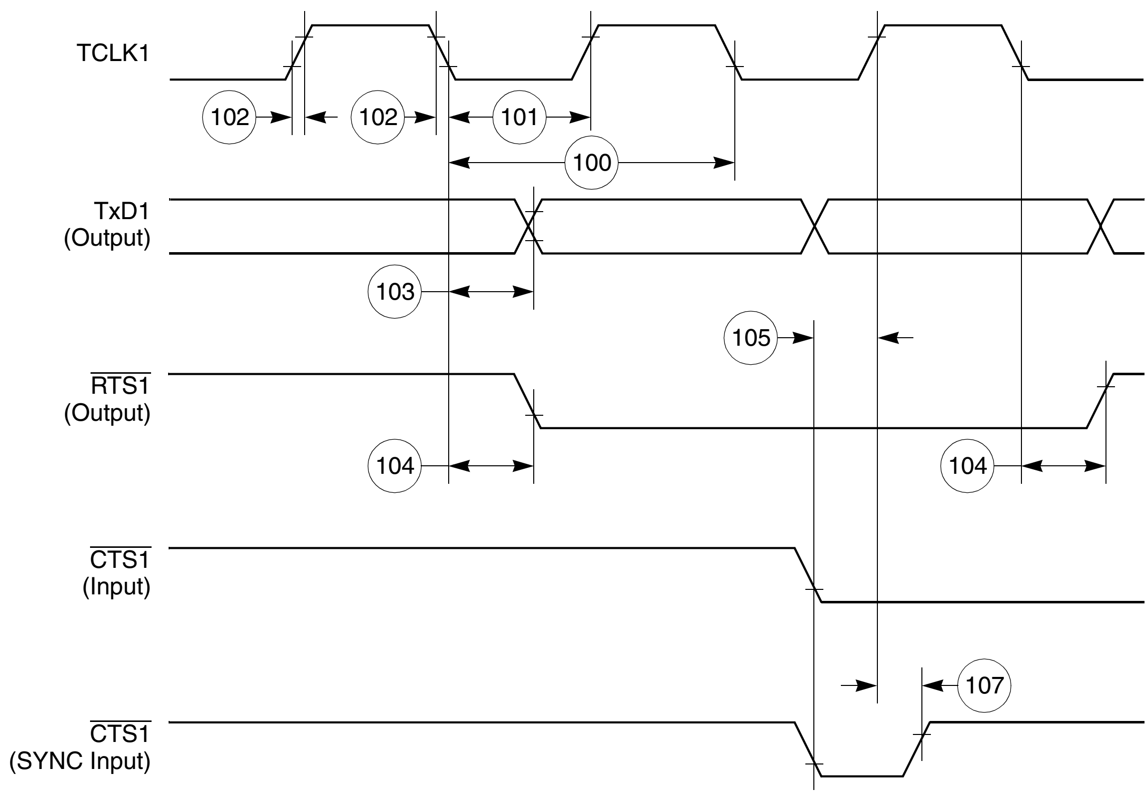


Figure 57. SCC NMSI Transmit Timing Diagram

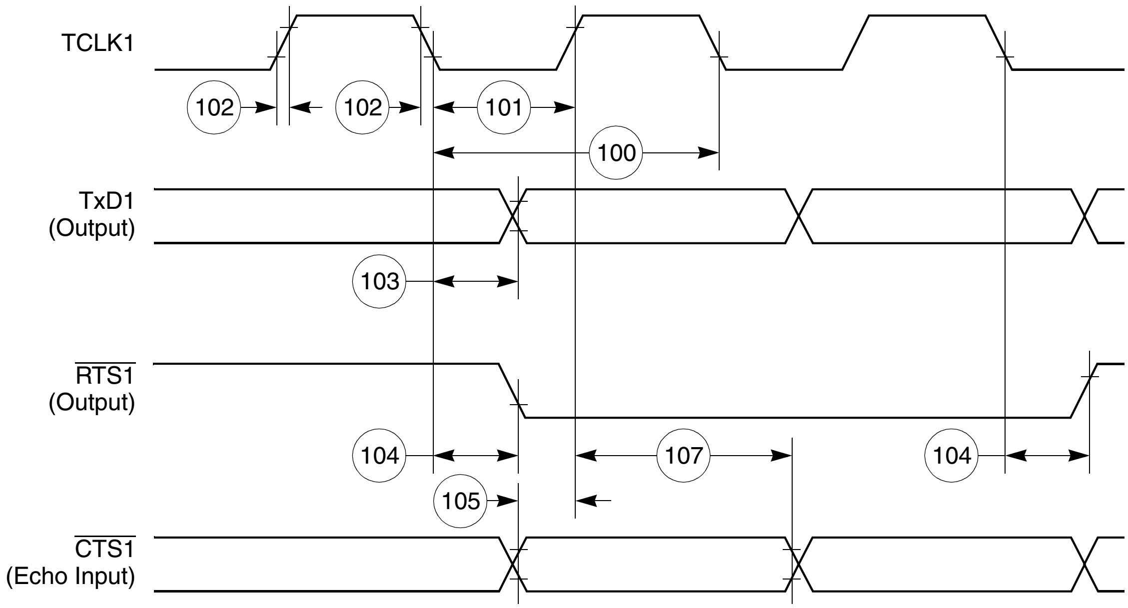


Figure 58. HDLC Bus Timing Diagram

11.8 Ethernet Electrical Specifications

Table 22 provides the Ethernet timings as shown in Figure 59 through Figure 63.

Table 22. Ethernet Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
120	CLSN width high	40	—	ns
121	RCLK1 rise/fall time	—	15	ns
122	RCLK1 width low	40	—	ns
123	RCLK1 clock period[1]	80	120	ns
124	RXD1 setup time	20	—	ns
125	RXD1 hold time	5	—	ns
126	RENA active delay (from RCLK1 rising edge of the last data bit)	10	—	ns
127	RENA width low	100	—	ns
128	TCLK1 rise/fall time	—	15	ns
129	TCLK1 width low	40	—	ns
130	TCLK1 clock period[1]	99	101	ns
131	TXD1 active delay (from TCLK1 rising edge)	10	50	ns
132	TXD1 inactive delay (from TCLK1 rising edge)	10	50	ns
133	TENA active delay (from TCLK1 rising edge)	10	50	ns
134	TENA inactive delay (from TCLK1 rising edge)	10	50	ns

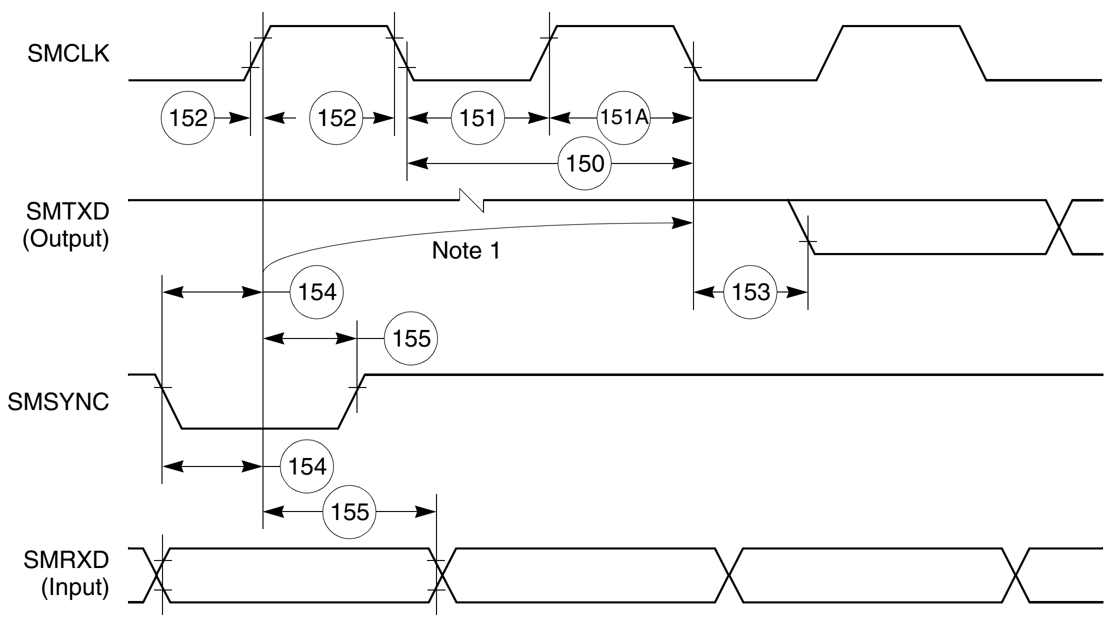
11.9 SMC Transparent AC Electrical Specifications

Table 23 provides the SMC transparent timings as shown in Figure 64.

Table 23. SMC Transparent Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
150	SMCLK clock period[1]	100	—	ns
151	SMCLK width low	50	—	ns
151A	SMCLK width high	50	—	ns
152	SMCLK rise/fall time	—	15	ns
153	SMTXD active delay (from SMCLK falling edge)	10	50	ns
154	SMRXD/SMSYNC setup time	20	—	ns
155	RXD1/SMSYNC hold time	5	—	ns

[1] SYNCCLK must be at least twice as fast as SMCLK.



Note:
1. This delay is equal to an integer number of character-length clocks.

Figure 64. SMC Transparent Timing Diagram

Figure 69 shows the I^{2}C bus timing.

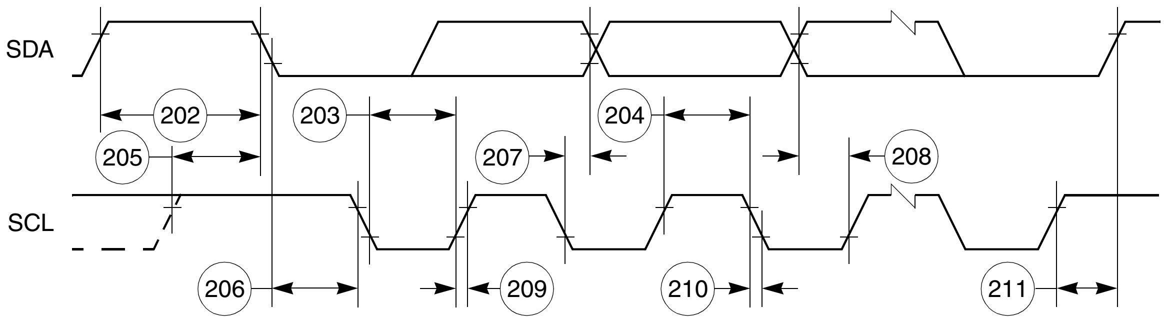


Figure 69. I^{2}C Bus Timing Diagram

12 UTOPIA AC Electrical Specifications

Table 28 shows the AC electrical specifications for the UTOPIA interface.

Table 28. UTOPIA AC Electrical Specifications

Num	Signal Characteristic	Direction	Min	Max	Unit
U1	UtpClk rise/fall time (Internal clock option)	Output	—	3.5	ns
	Duty cycle		50	50	%
	Frequency		—	50	MHz
U1a	UtpClk rise/fall time (external clock option)	Input	—	3.5	ns
	Duty cycle		40	60	%
	Frequency		—	50	MHz
U2	$\overline{\text{RxEnb}}$ and $\overline{\text{TxEnb}}$ active delay	Output	2	16	ns
U3	UTPB, SOC, Rxclav and Txclav setup time	Input	8	—	ns
U4	UTPB, SOC, Rxclav and Txclav hold time	Input	1	—	ns
U5	UTPB, SOC active delay (and PHREQ and PHSEL active delay in MPHY mode)	Output	2	16	ns

13.2 MII Transmit Signal Timing (MII_TXD[3:0], MII_TX_EN, MII_TX_ER, MII_TX_CLK)

The transmitter functions correctly up to a MII_TX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed the MII_TX_CLK frequency – 1%.

Table 30 provides information on the MII transmit signal timing.

Table 30. MII Transmit Signal Timing

Num	Characteristic	Min	Max	Unit
M5	MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER invalid	5	—	ns
M6	MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER valid	—	25	
M7	MII_TX_CLK pulse width high	35	65%	MII_TX_CLK period
M8	MII_TX_CLK pulse width low	35%	65%	MII_TX_CLK period

Figure 73 shows the MII transmit signal timing diagram.

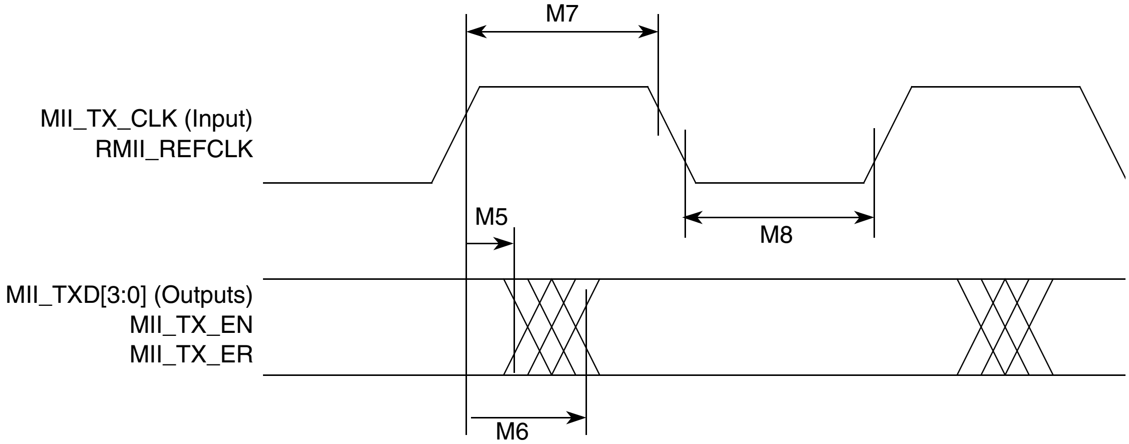


Figure 73. MII Transmit Signal Timing Diagram

13.3 MII Async Inputs Signal Timing (MII_CRS, MII_COL)

Table 31 provides information on the MII async inputs signal timing.

Table 31. MII Async Inputs Signal Timing

Num	Characteristic	Min	Max	Unit
M9	MII_CRS, MII_COL minimum pulse width	1.5	—	MII_TX_CLK period

Figure 74 shows the MII asynchronous inputs signal timing diagram.

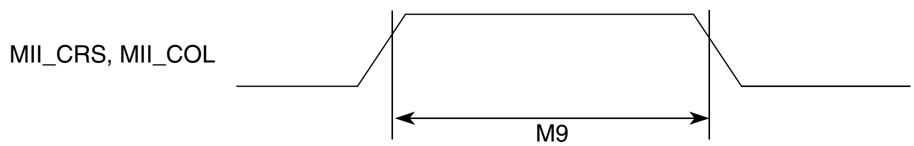


Figure 74. MII Async Inputs Timing Diagram

13.4 MII Serial Management Channel Timing (MII_MDIO, MII_MDC)

Table 32 provides information on the MII serial management channel signal timing. The FEC functions correctly with a maximum MDC frequency in excess of 2.5 MHz. The exact upper bound is under investigation.

Table 32. MII Serial Management Channel Timing

Num	Characteristic	Min	Max	Unit
M10	MII_MDC falling edge to MII_MDIO output invalid (minimum propagation delay)	0	—	ns
M11	MII_MDC falling edge to MII_MDIO output valid (max prop delay)	—	25	ns
M12	MII_MDIO (input) to MII_MDC rising edge setup	10	—	ns
M13	MII_MDIO (input) to MII_MDC rising edge hold	0	—	ns
M14	MII_MDC pulse width high	40%	60%	MII_MDC period
M15	MII_MDC pulse width low	40%	60%	MII_MDC period

Table 34. MPC860 Family Package/Frequency Availability (continued)

Package Type	Freq. (MHz) / Temp. (Tj)	Package	Order Number
Ball grid array *(continued)* ZP suffix—leaded ZQ suffix—leaded VR suffix—lead-free	80 0° to 95°C	ZP/ZQ[1]	MPC855TZQ80D4 MPC860DEZQ80D4 MPC860DTZQ80D4 MPC860ENZQ80D4 MPC860SRZQ80D4 MPC860TZQ80D4 MPC860DPZQ80D4 MPC860PZQ80D4
		Tape and Reel	MPC860PZQ80D4R2 MPC860PVR80D4R2
		VR	MPC855TVR80D4 MPC860DEVR80D4 MPC860DPVR80D4 MPC860ENVR80D4 MPC860PVR80D4 MPC860SRVR80D4 MPC860TVR80D4
Ball grid array (CZP suffix) CZP suffix—leaded CZQ suffix—leaded CVR suffix—lead-free	50 –40° to 95°C	ZP/ZQ[1]	MPC855TCZQ50D4 MPC855TCVR50D4 MPC860DECZQ50D4 MPC860DTCZQ50D4 MPC860ENCZQ50D4 MPC860SRCZQ50D4 MPC860TCZQ50D4 MPC860DPCZQ50D4 MPC860PCZQ50D4
		Tape and Reel	MPC855TCZQ50D4R2 MC860ENCVR50D4R2
		CVR	MPC860DECVR50D4 MPC860DTCVR50D4 MPC860ENCVR50D4 MPC860PCVR50D4 MPC860SRCVR50D4 MPC860TCVR50D4
	66 –40° to 95°C	ZP/ZQ[1]	MPC855TCZQ66D4 MPC855TCVR66D4 MPC860ENCZQ66D4 MPC860SRCZQ66D4 MPC860TCZQ66D4 MPC860DPCZQ66D4 MPC860PCZQ66D4
		CVR	MPC860DTCVR66D4 MPC860ENCVR66D4 MPC860PCVR66D4 MPC860SRCVR66D4 MPC860TCVR66D4

[1] The ZP package is no longer recommended for use. The ZQ package replaces the ZP package.

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