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Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Active
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	50MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (4), 10/100Mbps (1)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 95°C (TJ)
Security Features	-
Package / Case	357-BBGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc860pcvr50d4

- System integration unit (SIU)
 - Bus monitor
 - Software watchdog
 - Periodic interrupt timer (PIT)
 - Low-power stop mode
 - Clock synthesizer
 - Decrementer, time base, and real-time clock (RTC)
 - Reset controller
 - IEEE 1149.1™ Std. test access port (JTAG)
- Interrupts
 - Seven external interrupt request (IRQ) lines
 - 12 port pins with interrupt capability
 - 23 internal interrupt sources
 - Programmable priority between SCCs
 - Programmable highest priority request
- 10/100 Mbps Ethernet support, fully compliant with the IEEE 802.3u® Standard (not available when using ATM over UTOPIA interface)
- ATM support compliant with ATM forum UNI 4.0 specification
 - Cell processing up to 50–70 Mbps at 50-MHz system clock
 - Cell multiplexing/demultiplexing
 - Support of AAL5 and AAL0 protocols on a per-VC basis. AAL0 support enables OAM and software implementation of other protocols.
 - ATM pace control (APC) scheduler, providing direct support for constant bit rate (CBR) and unspecified bit rate (UBR) and providing control mechanisms enabling software support of available bit rate (ABR)
 - Physical interface support for UTOPIA (10/100-Mbps is not supported with this interface) and byte-aligned serial (for example, T1/E1/ADSL)
 - UTOPIA-mode ATM supports level-1 master with cell-level handshake, multi-PHY (up to four physical layer devices), connection to 25-, 51-, or 155-Mbps framers, and UTOPIA/system clock ratios of 1/2 or 1/3.
 - Serial-mode ATM connection supports transmission convergence (TC) function for T1/E1/ADSL lines, cell delineation, cell payload scrambling/descrambling, automatic idle/unassigned cell insertion/stripping, header error control (HEC) generation, checking, and statistics.
- Communications processor module (CPM)
 - RISC communications processor (CP)
 - Communication-specific commands (for example, GRACEFUL STOP TRANSMIT, ENTER HUNT MODE, and RESTART TRANSMIT)
 - Supports continuous mode transmission and reception on all serial channels

5 Power Dissipation

Table 5 provides power dissipation information. The modes are 1:1, where CPU and bus speeds are equal, and 2:1, where CPU frequency is twice the bus speed.

Table 5. Power Dissipation (P_D)

Die Revision	Frequency (MHz)	Typical ¹	Maximum ²	Unit
D.4 (1:1 mode)	50	656	735	mW
	66	TBD	TBD	mW
D.4 (2:1 mode)	66	722	762	mW
	80	851	909	mW

¹ Typical power dissipation is measured at 3.3 V.

² Maximum power dissipation is measured at 3.5 V.

NOTE

Values in Table 5 represent V_{DDL} -based power dissipation and do not include I/O power dissipation over V_{DDH} . I/O power dissipation varies widely by application due to buffer current, depending on external circuitry.

6 DC Characteristics

Table 6 provides the DC electrical characteristics for the MPC860.

Table 6. DC Electrical Specifications

Characteristic	Symbol	Min	Max	Unit
Operating voltage at 40 MHz or less	V_{DDH} , V_{DDL} , V_{DDSYN}	3.0	3.6	V
	KAPWR (power-down mode)	2.0	3.6	V
	KAPWR (all other operating modes)	$V_{DDH} - 0.4$	V_{DDH}	V
Operating voltage greater than 40 MHz	V_{DDH} , V_{DDL} , KAPWR, V_{DDSYN}	3.135	3.465	V
	KAPWR (power-down mode)	2.0	3.6	V
	KAPWR (all other operating modes)	$V_{DDH} - 0.4$	V_{DDH}	V
Input high voltage (all inputs except EXTAL and EXTCLK)	V_{IH}	2.0	5.5	V
Input low voltage ¹	V_{IL}	GND	0.8	V
EXTAL, EXTCLK input high voltage	V_{IHC}	$0.7 \times (V_{DDH})$	$V_{DDH} + 0.3$	V
Input leakage current, $V_{in} = 5.5$ V (except TMS, \overline{TRST} , DSCK, and DSDI pins)	I_{in}	—	100	μ A

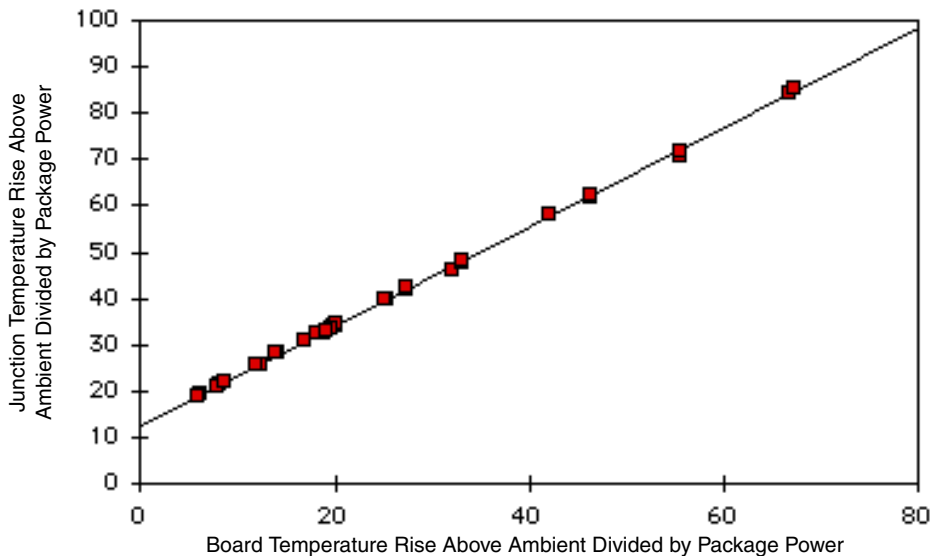


Figure 2. Effect of Board Temperature Rise on Thermal Behavior

If the board temperature is known, an estimate of the junction temperature in the environment can be made using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

$R_{\theta JB}$ = junction-to-board thermal resistance ($^{\circ}\text{C}/\text{W}$)

T_B = board temperature ($^{\circ}\text{C}$)

P_D = power dissipation in package

If the board temperature is known and the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. For this method to work, the board and board mounting must be similar to the test board used to determine the junction-to-board thermal resistance, namely a 2s2p (board with a power and a ground plane) and by attaching the thermal balls to the ground plane.

7.4 Estimation Using Simulation

When the board temperature is not known, a thermal simulation of the application is needed. The simple two-resistor model can be used with the thermal simulation of the application [2], or a more accurate and complex model of the package can be used in the thermal simulation.

7.5 Experimental Determination

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

Ψ_{JT} = thermal characterization parameter

T_T = thermocouple temperature on top of package

P_D = power dissipation in package

The thermal characterization parameter is measured per JEDEC JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

7.6 References

Semiconductor Equipment and Materials International (415) 964-5111
 805 East Middlefield Rd.
 Mountain View, CA 94043

MIL-SPEC and EIA/JESD (JEDEC) Specifications 800-854-7179 or
 (Available from Global Engineering Documents) 303-397-7956

JEDEC Specifications <http://www.jedec.org>

1. C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.
2. B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212–220.

8 Layout Practices

Each V_{DD} pin on the MPC860 should be provided with a low-impedance path to the board’s supply. Each GND pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on the chip. The V_{DD} power supply should be bypassed to ground using at least four 0.1 μ F-bypass capacitors located as close as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to chip V_{DD} and GND should be kept to less than half an inch per capacitor lead. A four-layer board employing two inner layers as V_{CC} and GND planes is recommended.

All output pins on the MPC860 have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized in order to minimize undershoot and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data buses. Maximum PC trace lengths of 6 inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the V_{CC} and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.

Table 7. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B29d	$\overline{WE}(0:3)$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 0	43.45	—	35.5	—	28.00	—	20.73	—	ns
B29e	\overline{CS} negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 0	43.45	—	35.5	—	28.00	—	29.73	—	ns
B29f	$\overline{WE}(0:3)$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 1	8.86	—	6.88	—	5.00	—	3.18	—	ns
B29g	\overline{CS} negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 1	8.86	—	6.88	—	5.00	—	3.18	—	ns
B29h	$\overline{WE}(0:3)$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 1	38.67	—	31.38	—	24.50	—	17.83	—	ns
B29i	\overline{CS} negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 1	38.67	—	31.38	—	24.50	—	17.83	—	ns
B30	\overline{CS} , $\overline{WE}(0:3)$ negated to A(0:31), BADDR(28:30) invalid GPCM write access ⁸	5.58	—	4.25	—	3.00	—	1.79	—	ns
B30a	$\overline{WE}(0:3)$ negated to A(0:31), BADDR(28:30) invalid GPCM, write access, TRLX = 0, CSNT = 1, \overline{CS} negated to A(0:31) invalid GPCM write access, TRLX = 0, CSNT = 1 ACS = 10, or ACS = 11, EBDF = 0	13.15	—	10.50	—	8.00	—	5.58	—	ns
B30b	$\overline{WE}(0:3)$ negated to A(0:31), invalid GPCM BADDR(28:30) invalid GPCM write access, TRLX = 1, CSNT = 1. \overline{CS} negated to A(0:31), Invalid GPCM, write access, TRLX = 1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 0	43.45	—	35.50	—	28.00	—	20.73	—	ns
B30c	$\overline{WE}(0:3)$ negated to A(0:31), BADDR(28:30) invalid GPCM write access, TRLX = 0, CSNT = 1. \overline{CS} negated to A(0:31) invalid GPCM write access, TRLX = 0, CSNT = 1, ACS = 10, ACS = 11, EBDF = 1	8.36	—	6.38	—	4.50	—	2.68	—	ns
B30d	$\overline{WE}(0:3)$ negated to A(0:31), BADDR(28:30) invalid GPCM write access, TRLX = 1, CSNT = 1. \overline{CS} negated to A(0:31) invalid GPCM write access TRLX = 1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 1	38.67	—	31.38	—	24.50	—	17.83	—	ns
B31	CLKOUT falling edge to \overline{CS} valid—as requested by control bit CST4 in the corresponding word in UPM	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns

Table 7. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B35	A(0:31), BADDR(28:30) to \overline{CS} valid—as requested by control bit BST4 in the corresponding word in UPM	5.58	—	4.25	—	3.00	—	1.79	—	ns
B35a	A(0:31), BADDR(28:30), and D(0:31) to \overline{BS} valid—as requested by control bit BST1 in the corresponding word in UPM	13.15	—	10.50	—	8.00	—	5.58	—	ns
B35b	A(0:31), BADDR(28:30), and D(0:31) to \overline{BS} valid—as requested by control bit BST2 in the corresponding word in UPM	20.73	—	16.75	—	13.00	—	9.36	—	ns
B36	A(0:31), BADDR(28:30), and D(0:31) to \overline{GPL} valid—as requested by control bit GxT4 in the corresponding word in UPM	5.58	—	4.25	—	3.00	—	1.79	—	ns
B37	UPWAIT valid to CLKOUT falling edge ⁹	6.00	—	6.00	—	6.00	—	6.00	—	ns
B38	CLKOUT falling edge to UPWAIT valid ⁹	1.00	—	1.00	—	1.00	—	1.00	—	ns
B39	\overline{AS} valid to CLKOUT rising edge ¹⁰	7.00	—	7.00	—	7.00	—	7.00	—	ns
B40	A(0:31), TSIZ(0:1), RD/ \overline{WR} , \overline{BURST} , valid to CLKOUT rising edge	7.00	—	7.00	—	7.00	—	7.00	—	ns
B41	\overline{TS} valid to CLKOUT rising edge (setup time)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B42	CLKOUT rising edge to \overline{TS} valid (hold time)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B43	\overline{AS} negation to memory controller signals negation	—	TBD	—	TBD	—	TBD	—	TBD	ns

¹ Phase and frequency jitter performance results are only valid if the input jitter is less than the prescribed value.

² If the rate of change of the frequency of EXTAL is slow (that is, it does not jump between the minimum and maximum values in one cycle) or the frequency of the jitter is fast (that is, it does not stay at an extreme value for a long time) then the maximum allowed jitter on EXTAL can be up to 2%.

³ The timings specified in B4 and B5 are based on full strength clock.

⁴ The timing for \overline{BR} output is relevant when the MPC860 is selected to work with external bus arbiter. The timing for \overline{BG} output is relevant when the MPC860 is selected to work with internal bus arbiter.

⁵ The timing required for \overline{BR} input is relevant when the MPC860 is selected to work with internal bus arbiter. The timing for \overline{BG} input is relevant when the MPC860 is selected to work with external bus arbiter.

⁶ The D(0:31) and DP(0:3) input timings B18 and B19 refer to the rising edge of the CLKOUT in which the \overline{TA} input signal is asserted.

⁷ The D(0:31) and DP(0:3) input timings B20 and B21 refer to the falling edge of the CLKOUT. This timing is valid only for read accesses controlled by chip-selects under control of the UPM in the memory controller, for data beats where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

⁸ The timing B30 refers to \overline{CS} when ACS = 00 and to $\overline{WE}(0:3)$ when CSNT = 0.

⁹ The signal UPWAIT is considered asynchronous to the CLKOUT and synchronized internally. The timings specified in B37 and B38 are specified to enable the freeze of the UPM output signals as described in [Figure 18](#).

¹⁰ The \overline{AS} signal is considered asynchronous to the CLKOUT. The timing B39 is specified in order to allow the behavior specified in [Figure 21](#).

Figure 5 provides the timing for the synchronous output signals.

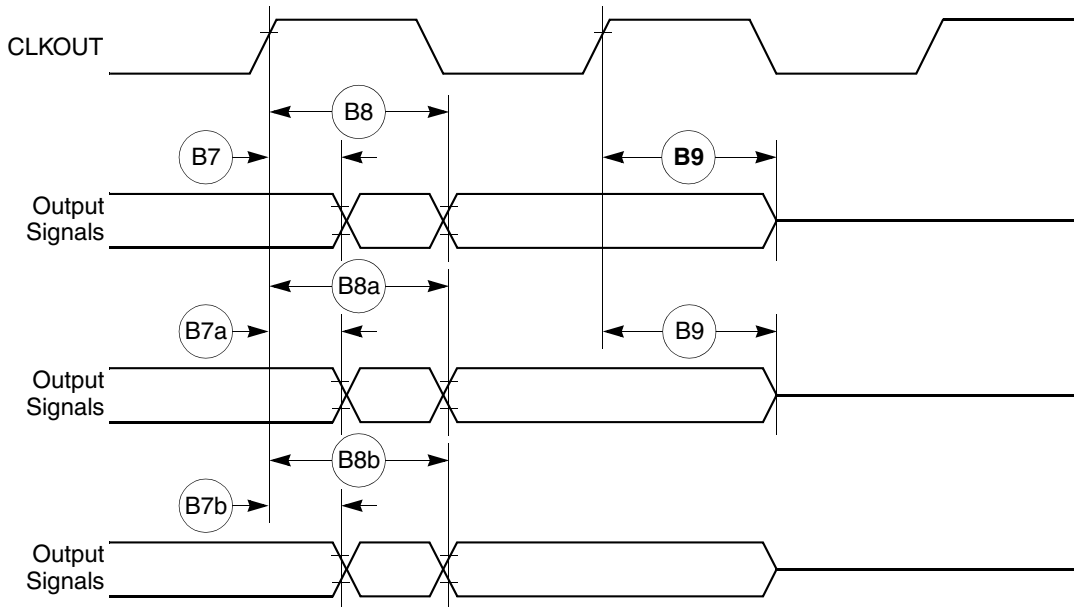


Figure 5. Synchronous Output Signals Timing

Figure 6 provides the timing for the synchronous active pull-up and open-drain output signals.

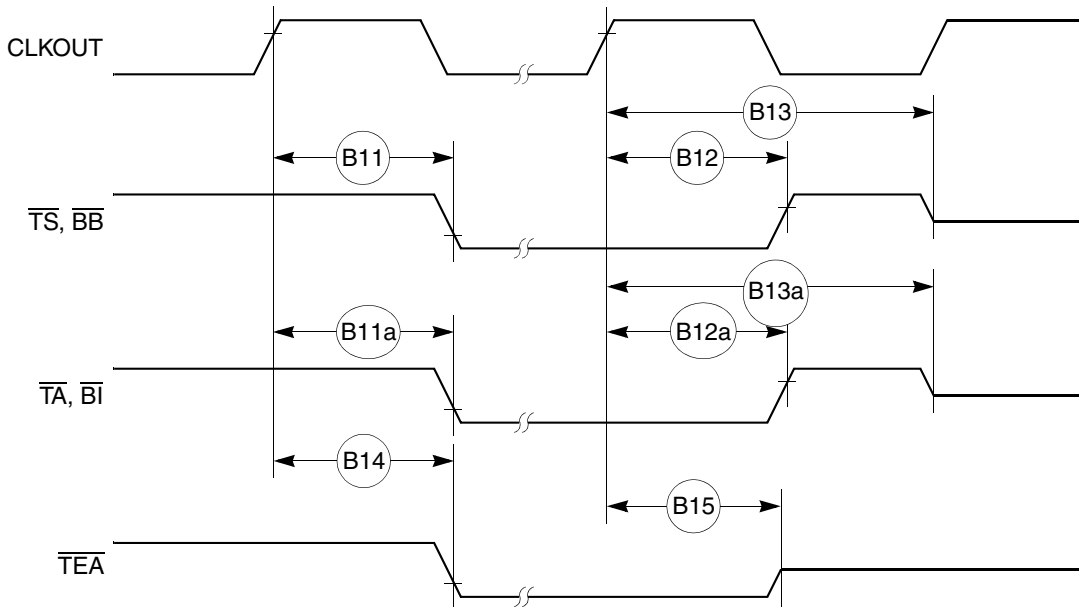


Figure 6. Synchronous Active Pull-Up Resistor and Open-Drain Outputs Signals Timing

Figure 7 provides the timing for the synchronous input signals.

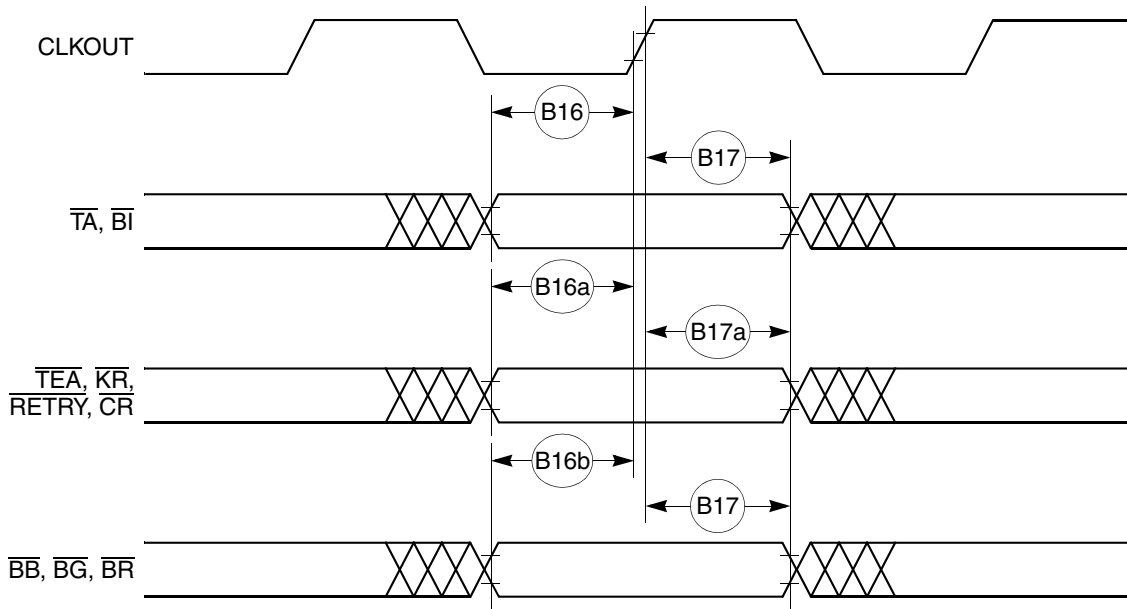


Figure 7. Synchronous Input Signals Timing

Figure 8 provides normal case timing for input data. It also applies to normal read accesses under the control of the UPM in the memory controller.

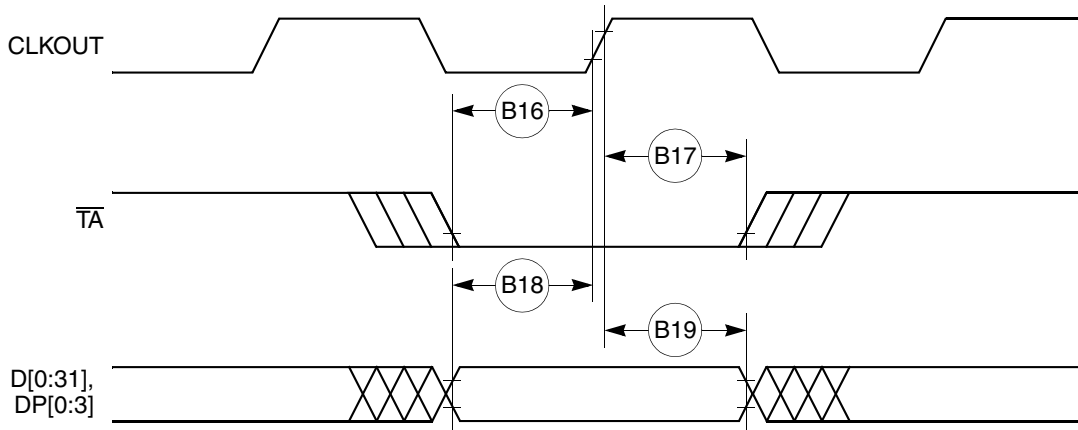


Figure 8. Input Data Timing in Normal Case

Figure 25 provides the PCMCIA access cycle timing for the external bus read.

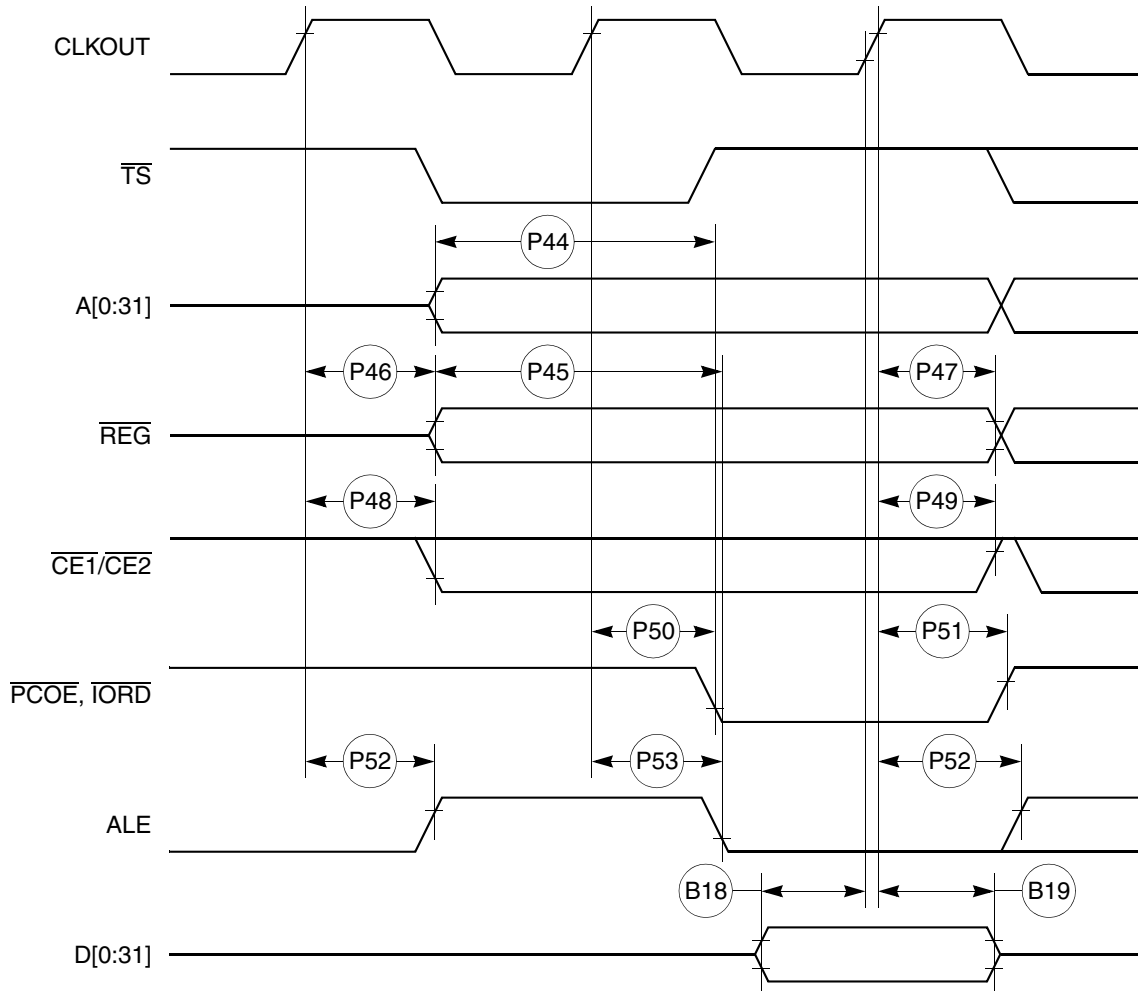


Figure 25. PCMCIA Access Cycle Timing External Bus Read

Figure 32 shows the reset timing for the data bus configuration.

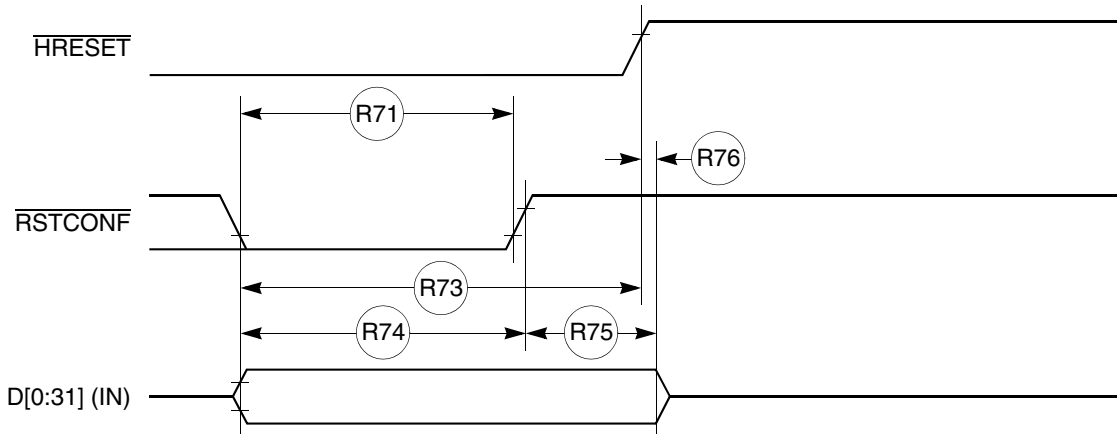


Figure 32. Reset Timing—Configuration from Data Bus

Figure 33 provides the reset timing for the data bus weak drive during configuration.

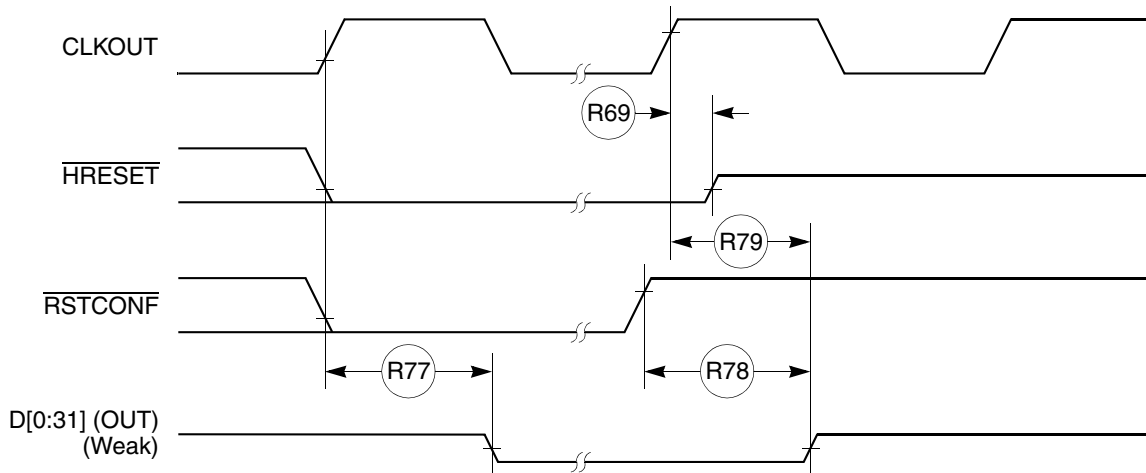


Figure 33. Reset Timing—Data Bus Weak Drive During Configuration

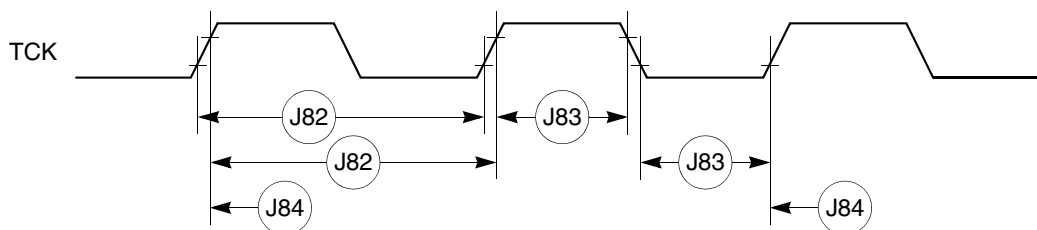


Figure 35. JTAG Test Clock Input Timing

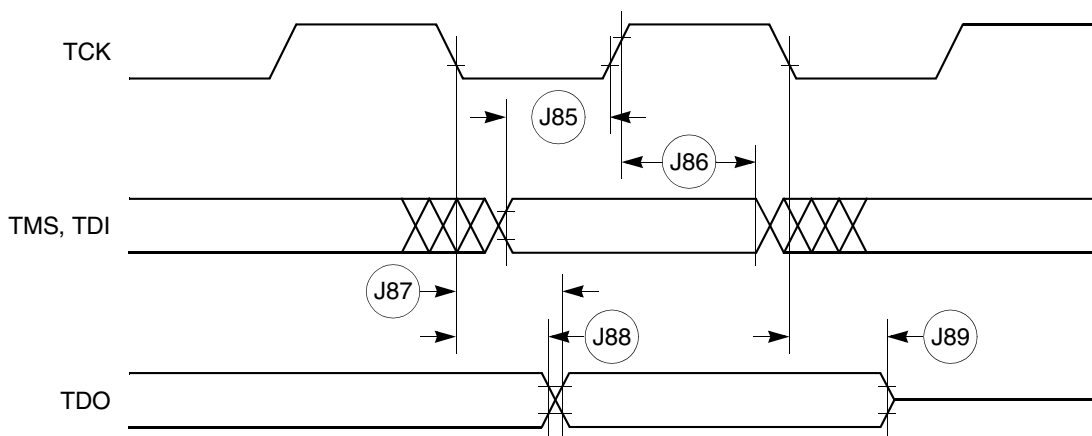


Figure 36. JTAG Test Access Port Timing Diagram

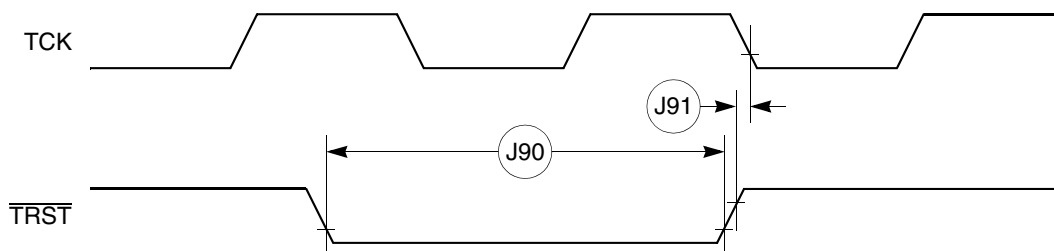


Figure 37. JTAG TRST Timing Diagram

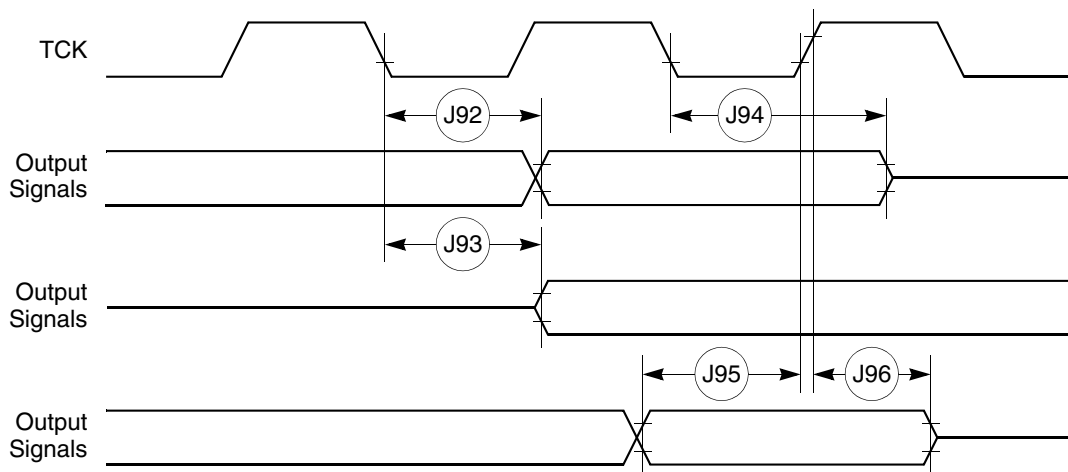


Figure 38. Boundary Scan (JTAG) Timing Diagram

11 CPM Electrical Characteristics

This section provides the AC and DC electrical specifications for the communications processor module (CPM) of the MPC860.

11.1 PIP/PIO AC Electrical Specifications

Table 14 provides the PIP/PIO AC timings as shown in Figure 39 through Figure 43.

Table 14. PIP/PIO Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
21	Data-in setup time to STBI low	0	—	ns
22	Data-in hold time to STBI high	$2.5 - t_3^1$	—	CLK
23	STBI pulse width	1.5	—	CLK
24	STBO pulse width	1 CLK – 5 ns	—	ns
25	Data-out setup time to STBO low	2	—	CLK
26	Data-out hold time from STBO high	5	—	CLK
27	STBI low to STBO low (Rx interlock)	—	2	CLK
28	STBI low to STBO high (Tx interlock)	2	—	CLK
29	Data-in setup time to clock high	15	—	ns
30	Data-in hold time from clock high	7.5	—	ns
31	Clock low to data-out valid (CPU writes data, control, or direction)	—	25	ns

¹ t_3 = Specification 23.

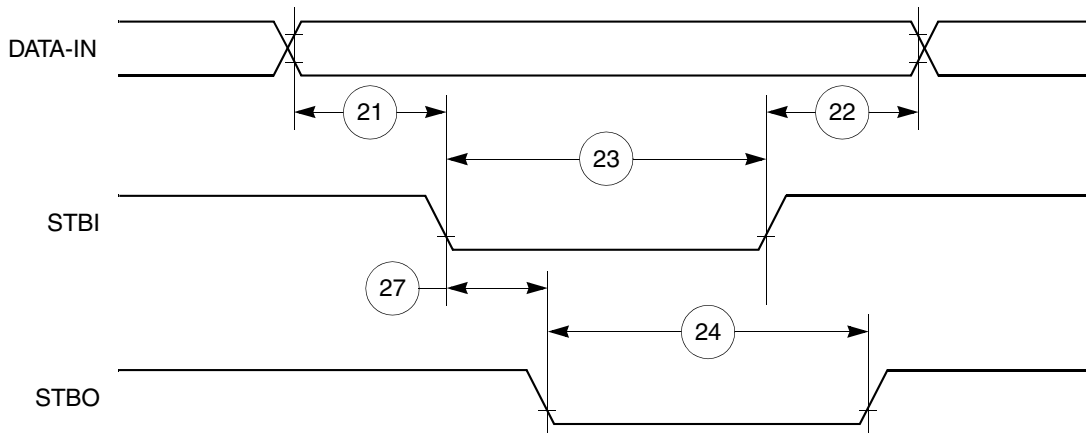


Figure 39. PIP Rx (Interlock Mode) Timing Diagram

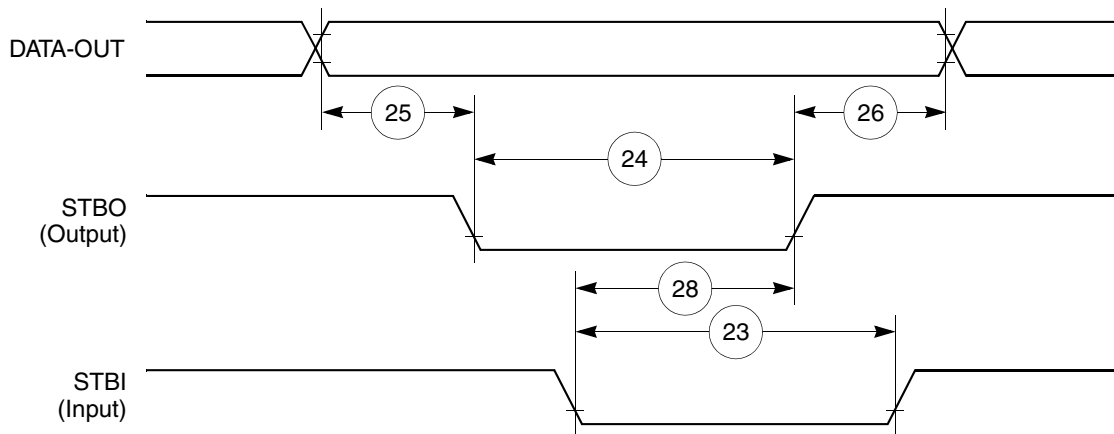


Figure 40. PIP Tx (Interlock Mode) Timing Diagram

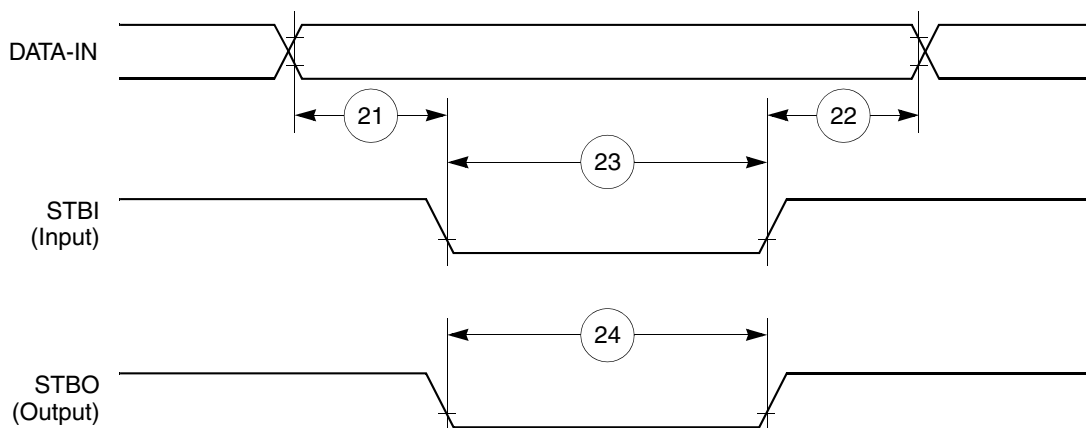


Figure 41. PIP Rx (Pulse Mode) Timing Diagram

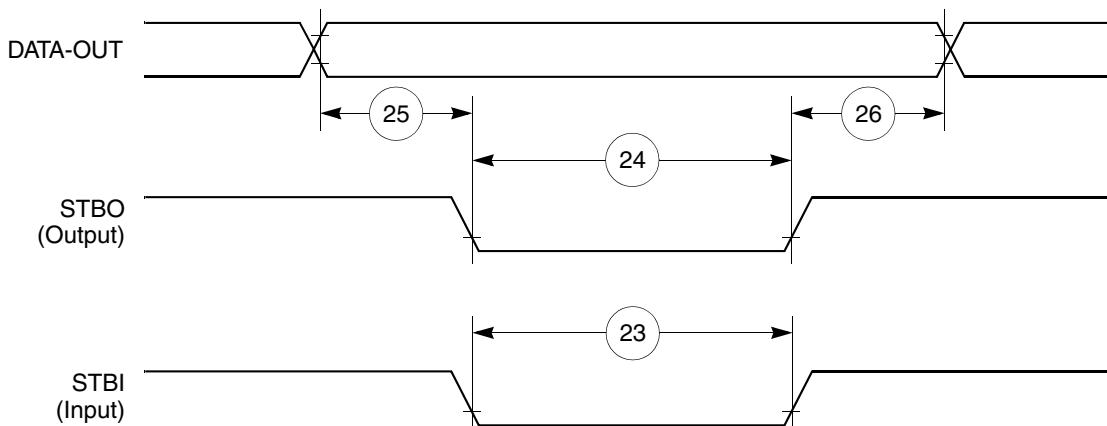


Figure 42. PIP TX (Pulse Mode) Timing Diagram

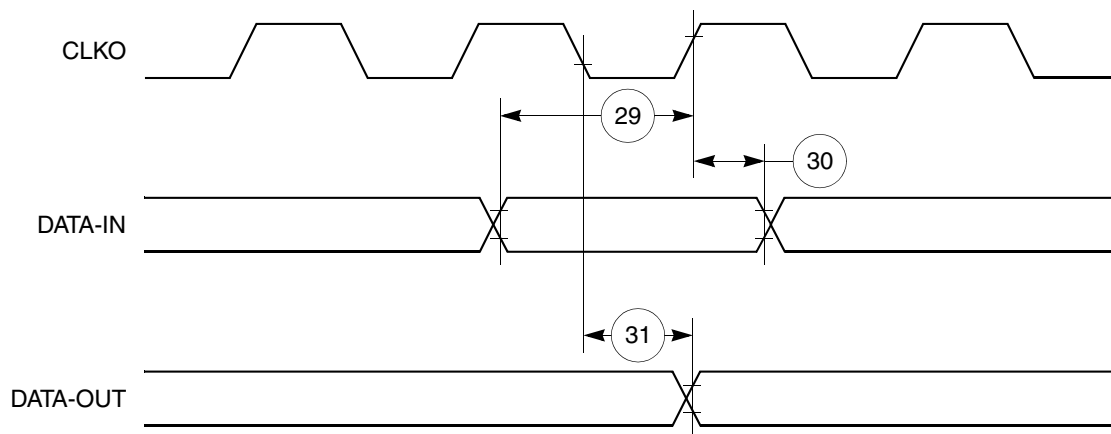


Figure 43. Parallel I/O Data-In/Data-Out Timing Diagram

11.2 Port C Interrupt AC Electrical Specifications

Table 15 provides the timings for port C interrupts.

Table 15. Port C Interrupt Timing

Num	Characteristic	≥ 33.34 MHz ¹		Unit
		Min	Max	
35	Port C interrupt pulse width low (edge-triggered mode)	55	—	ns
36	Port C interrupt minimum time between active edges	55	—	ns

¹ External bus frequency of greater than or equal to 33.34 MHz.

Figure 44 shows the port C interrupt detection timing.

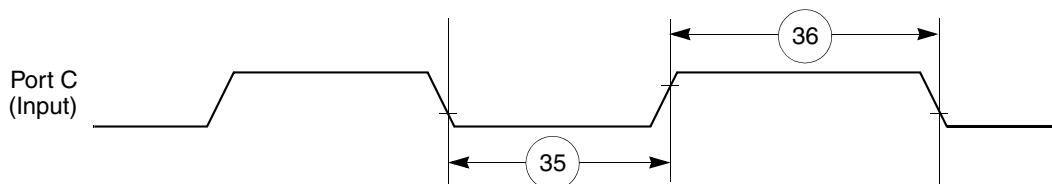


Figure 44. Port C Interrupt Detection Timing

11.3 IDMA Controller AC Electrical Specifications

Table 16 provides the IDMA controller timings as shown in Figure 45 through Figure 48.

Table 16. IDMA Controller Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
40	\overline{DREQ} setup time to clock high	7	—	ns
41	\overline{DREQ} hold time from clock high	3	—	ns

Table 19. SI Timing (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
84	L1CLK edge to L1CLKO valid (DSC = 1)	—	30.00	ns
85	$\overline{L1RQ}$ valid before falling edge of L1TSYNC ⁴	1.00	—	L1TCLK
86	L1GR setup time ²	42.00	—	ns
87	L1GR hold time	42.00	—	ns
88	L1CLK edge to L1SYNC valid (FSD = 00) CNT = 0000, BYT = 0, DSC = 0)	—	0.00	ns

¹ The ratio SYNCCLK/L1RCLK must be greater than 2.5/1.

² These specs are valid for IDL mode only.

³ Where $P = 1/CLKOUT$. Thus, for a 25-MHz CLK01 rate, $P = 40$ ns.

⁴ These strobes and TxD on the first bit of the frame become valid after L1CLK edge or L1SYNC, whichever comes later.

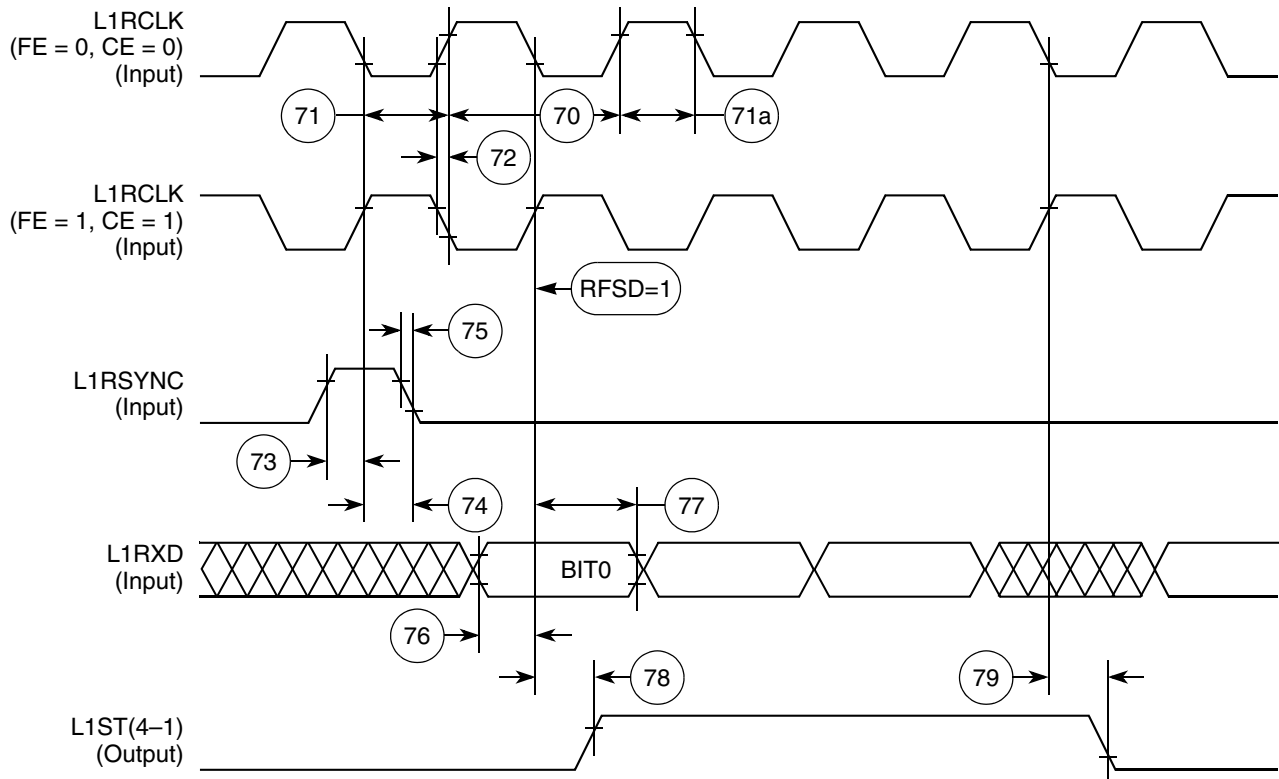


Figure 51. SI Receive Timing Diagram with Normal Clocking (DSC = 0)

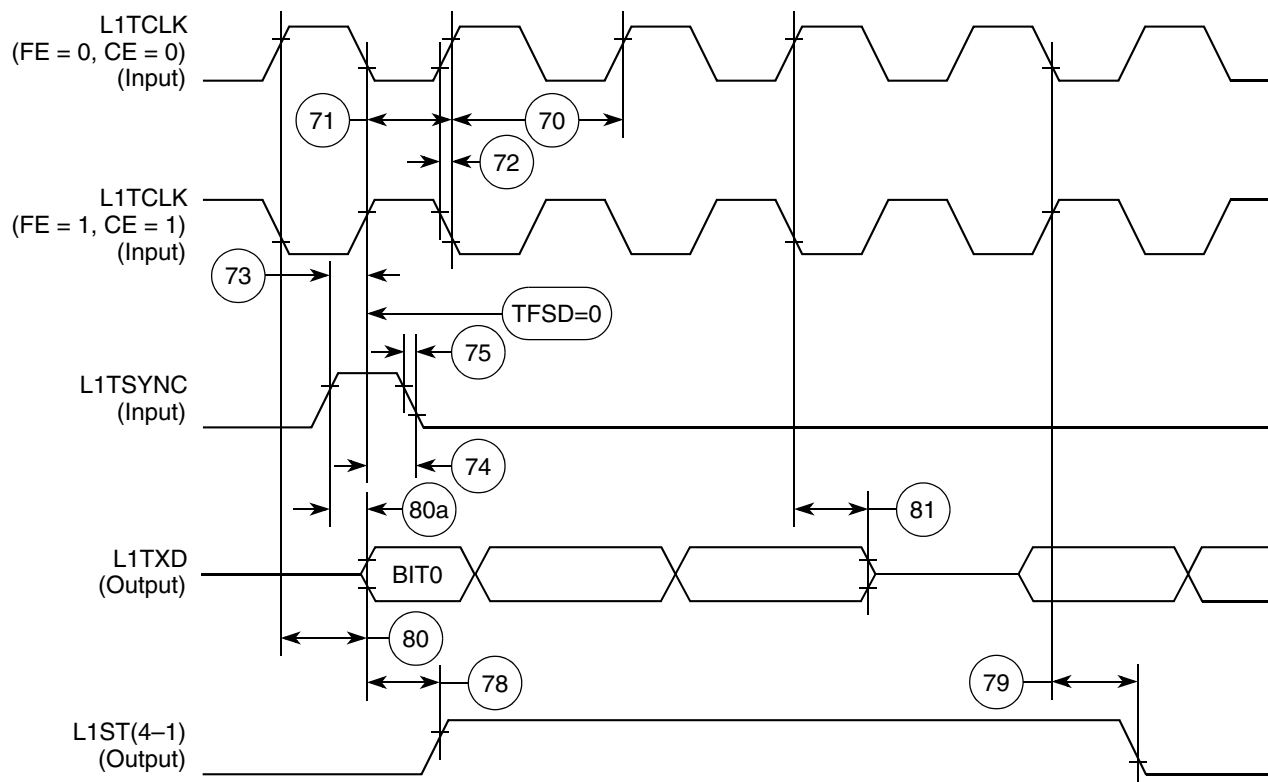


Figure 53. SI Transmit Timing Diagram (DSC = 0)

11.10 SPI Master AC Electrical Specifications

Table 24 provides the SPI master timings as shown in Figure 65 and Figure 66.

Table 24. SPI Master Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
160	MASTER cycle time	4	1024	t_{cyc}
161	MASTER clock (SCK) high or low time	2	512	t_{cyc}
162	MASTER data setup time (inputs)	50	—	ns
163	Master data hold time (inputs)	0	—	ns
164	Master data valid (after SCK edge)	—	20	ns
165	Master data hold time (outputs)	0	—	ns
166	Rise time output	—	15	ns
167	Fall time output	—	15	ns

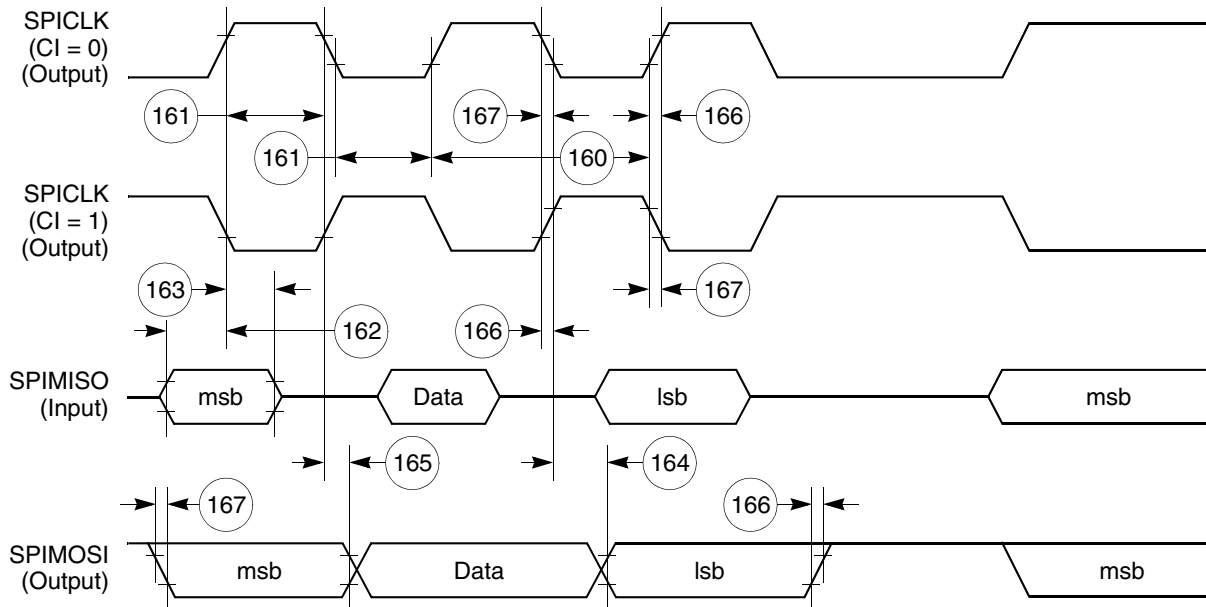


Figure 65. SPI Master (CP = 0) Timing Diagram

Figure 70 shows signal timings during UTOPIA receive operations.

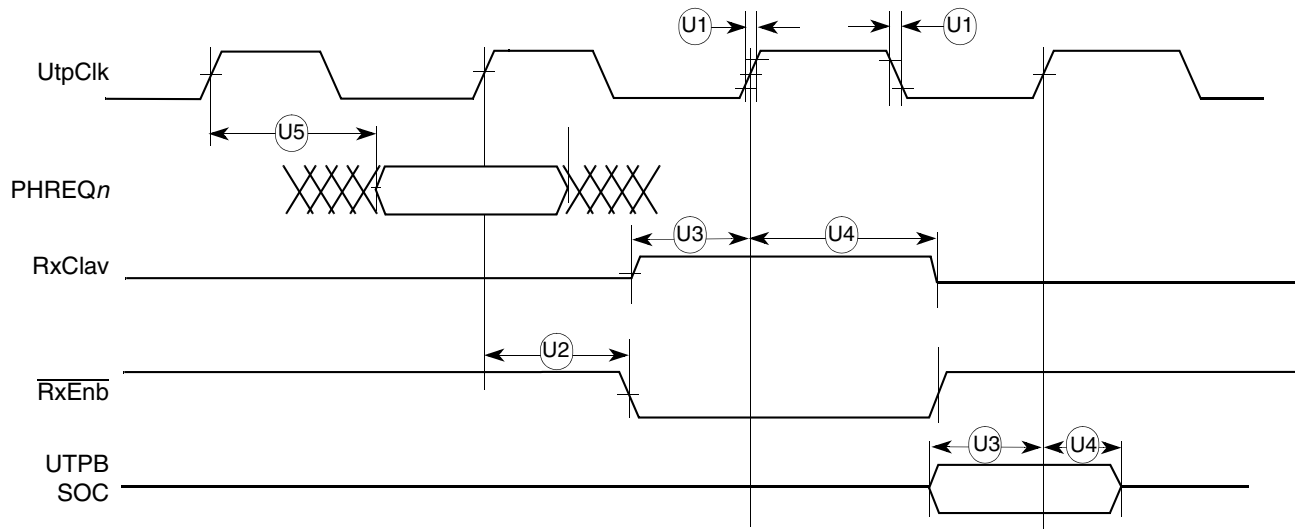


Figure 70. UTOPIA Receive Timing

Figure 71 shows signal timings during UTOPIA transmit operations.

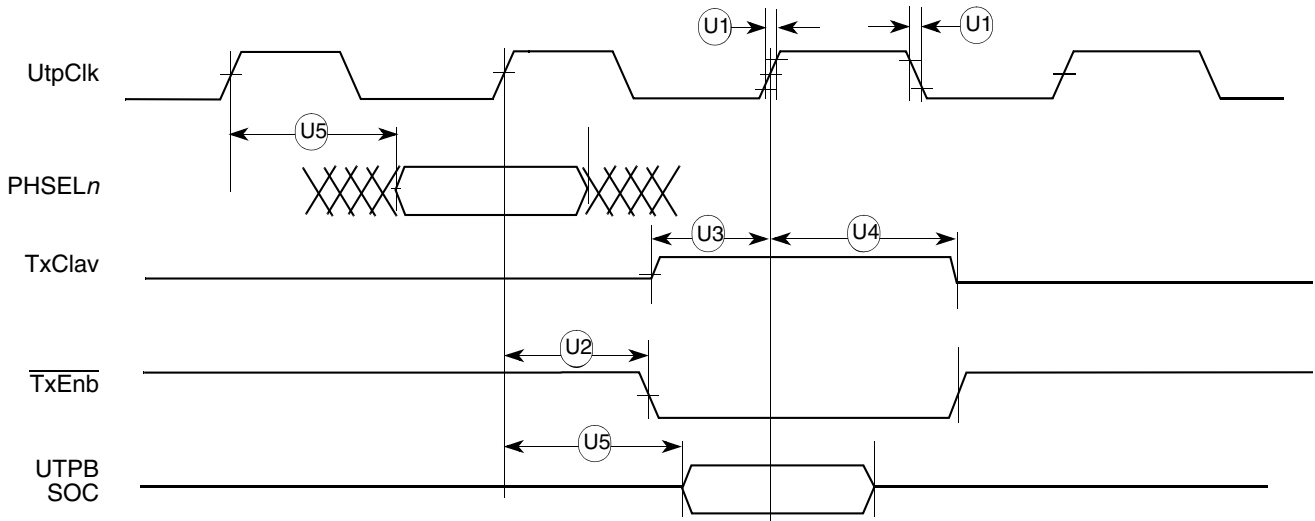


Figure 71. UTOPIA Transmit Timing

13 FEC Electrical Characteristics

This section provides the AC electrical specifications for the Fast Ethernet controller (FEC). Note that the timing specifications for the MII signals are independent of system clock frequency (part speed designation). Also, MII signals use TTL signal levels compatible with devices operating at either 5.0 V or 3.3 V.

13.1 MII Receive Signal Timing (MII_RXD[3:0], MII_RX_DV, MII_RX_ER, MII_RX_CLK)

The receiver functions correctly up to a MII_RX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed the MII_RX_CLK frequency – 1%.

Table 29 provides information on the MII receive signal timing.

Table 29. MII Receive Signal Timing

Num	Characteristic	Min	Max	Unit
M1	MII_RXD[3:0], MII_RX_DV, MII_RX_ER to MII_RX_CLK setup	5	—	ns
M2	MII_RX_CLK to MII_RXD[3:0], MII_RX_DV, MII_RX_ER hold	5	—	ns
M3	MII_RX_CLK pulse width high	35%	65%	MII_RX_CLK period
M4	MII_RX_CLK pulse width low	35%	65%	MII_RX_CLK period

Figure 72 shows MII receive signal timing.

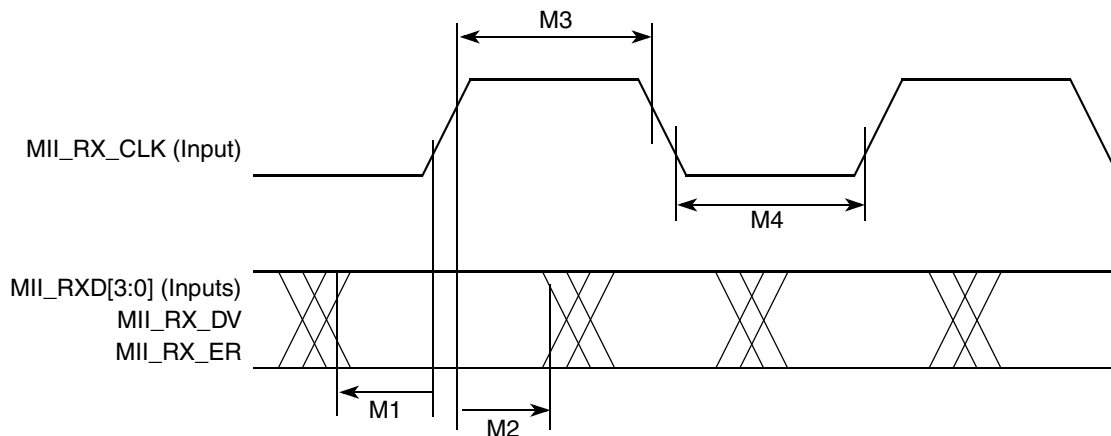


Figure 72. MII Receive Signal Timing Diagram

Table 34 identifies the packages and operating frequencies available for the MPC860.

Table 34. MPC860 Family Package/Frequency Availability

Package Type	Freq. (MHz) / Temp. (Tj)	Package	Order Number	
Ball grid array ZP suffix—leaded ZQ suffix—leaded VR suffix—lead-free	50 0° to 95°C	ZP/ZQ ¹	MPC855TZQ50D4 MPC860DEZQ50D4 MPC860DTZQ50D4 MPC860ENZQ50D4 MPC860SRZQ50D4 MPC860TZQ50D4 MPC860DPZQ50D4 MPC860PZQ50D4	
		Tape and Reel	MPC855TZQ50D4R2 MPC860DEZQ50D4R2 MPC860ENZQ50D4R2 MPC860SRZQ50D4R2 MPC860TZQ50D4R2 MPC860DPZQ50D4R2 MPC855TVR50D4R2 MPC860ENVR50D4R2 MPC860SRVR50D4R2 MPC860TVR50D4R2	
		VR	MPC855TVR50D4 MPC860DEV50D4 MPC860DPVR50D4 MPC860DTPVR50D4 MPC860ENVR50D4 MPC860PVR50D4 MPC860SRVR50D4 MPC860TVR50D4	
		66 0° to 95°C	ZP/ZQ ¹	MPC855TZQ66D4 MPC860DEZQ66D4 MPC860DTZQ66D4 MPC860ENZQ66D4 MPC860SRZQ66D4 MPC860TZQ66D4 MPC860DPZQ66D4 MPC860PZQ66D4
			Tape and Reel	MPC860SRZQ66D4R2 MPC860PZQ66D4R2
			VR	MPC855TVR66D4 MPC860DEV66D4 MPC860DPVR66D4 MPC860DTPVR66D4 MPC860ENVR66D4 MPC860PVR66D4 MPC860SRVR66D4 MPC860TVR66D4