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### Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

### Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

#### Details

Product Status	Active
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	66MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (4), 10/100Mbps (1)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 95°C (TJ)
Security Features	-
Package / Case	357-BBGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	<a href="https://www.e-xfl.com/pro/item?MUrl=&amp;PartUrl=mpc860pvr66d4">https://www.e-xfl.com/pro/item?MUrl=&amp;PartUrl=mpc860pvr66d4</a>

- System integration unit (SIU)
  - Bus monitor
  - Software watchdog
  - Periodic interrupt timer (PIT)
  - Low-power stop mode
  - Clock synthesizer
  - Decrementer, time base, and real-time clock (RTC)
  - Reset controller
  - IEEE 1149.1™ Std. test access port (JTAG)
- Interrupts
  - Seven external interrupt request (IRQ) lines
  - 12 port pins with interrupt capability
  - 23 internal interrupt sources
  - Programmable priority between SCCs
  - Programmable highest priority request
- 10/100 Mbps Ethernet support, fully compliant with the IEEE 802.3u® Standard (not available when using ATM over UTOPIA interface)
- ATM support compliant with ATM forum UNI 4.0 specification
  - Cell processing up to 50–70 Mbps at 50-MHz system clock
  - Cell multiplexing/demultiplexing
  - Support of AAL5 and AAL0 protocols on a per-VC basis. AAL0 support enables OAM and software implementation of other protocols.
  - ATM pace control (APC) scheduler, providing direct support for constant bit rate (CBR) and unspecified bit rate (UBR) and providing control mechanisms enabling software support of available bit rate (ABR)
  - Physical interface support for UTOPIA (10/100-Mbps is not supported with this interface) and byte-aligned serial (for example, T1/E1/ADSL)
  - UTOPIA-mode ATM supports level-1 master with cell-level handshake, multi-PHY (up to four physical layer devices), connection to 25-, 51-, or 155-Mbps framers, and UTOPIA/system clock ratios of 1/2 or 1/3.
  - Serial-mode ATM connection supports transmission convergence (TC) function for T1/E1/ADSL lines, cell delineation, cell payload scrambling/descrambling, automatic idle/unassigned cell insertion/stripping, header error control (HEC) generation, checking, and statistics.
- Communications processor module (CPM)
  - RISC communications processor (CP)
  - Communication-specific commands (for example, GRACEFUL STOP TRANSMIT, ENTER HUNT MODE, and RESTART TRANSMIT)
  - Supports continuous mode transmission and reception on all serial channels

## Features

- Allows dynamic changes
- Can be internally connected to six serial channels (four SCCs and two SMCs)
- Parallel interface port (PIP)
  - Centronics interface support
  - Supports fast connection between compatible ports on the MPC860 or the MC68360
- PCMCIA interface
  - Master (socket) interface, release 2.1 compliant
  - Supports two independent PCMCIA sockets
  - Supports eight memory or I/O windows
- Low power support
  - Full on—all units fully powered
  - Doze—core functional units disabled except time base decremter, PLL, memory controller, RTC, and CPM in low-power standby
  - Sleep—all units disabled except RTC and PIT, PLL active for fast wake up
  - Deep sleep—all units disabled including PLL except RTC and PIT
  - Power down mode—all units powered down except PLL, RTC, PIT, time base, and decremter
- Debug interface
  - Eight comparators: four operate on instruction address, two operate on data address, and two operate on data
  - Supports conditions: = ≠ < >
  - Each watchpoint can generate a break-point internally.
- 3.3-V operation with 5-V TTL compatibility except EXTAL and EXTCLK
- 357-pin ball grid array (BGA) package

Figure 1 shows the undershoot and overshoot voltages at the interface of the MPC860.

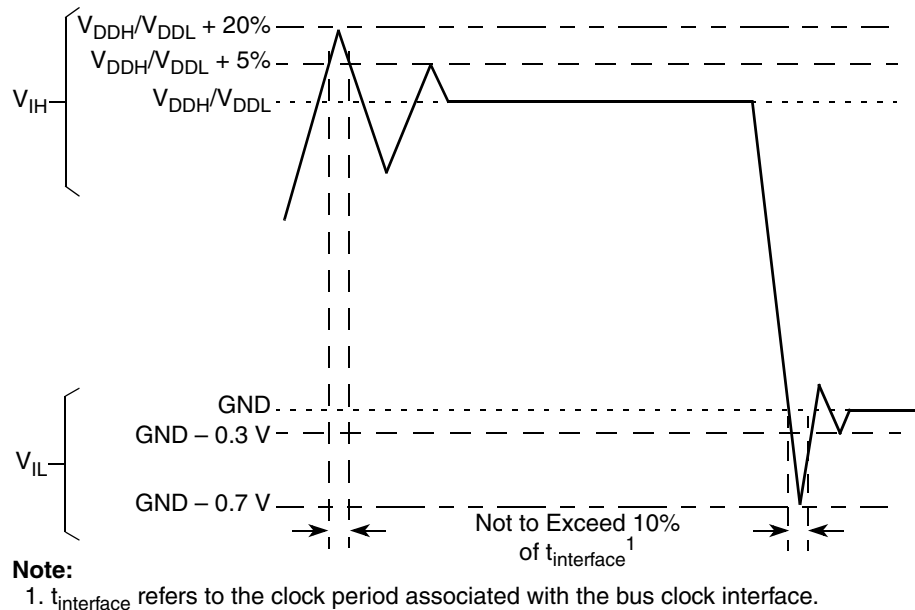


Figure 1. Undershoot/Overshoot Voltage for  $V_{\text{DDH}}$  and  $V_{\text{DDL}}$

## 4 Thermal Characteristics

Table 3. Package Description

Package Designator	Package Code (Case No.)	Package Description
ZP	5050 (1103-01)	PBGA 357 25*25*0.9P1.27
ZQ/VR	5058 (1103D-02)	PBGA 357 25*25*1.2P1.27

Table 6. DC Electrical Specifications (continued)

Characteristic	Symbol	Min	Max	Unit
Input leakage current, $V_{in} = 3.6$ V (except TMS, $\overline{TRST}$ , DSCK, and DSDI pins)	$I_{In}$	—	10	$\mu$ A
Input leakage current, $V_{in} = 0$ V (except TMS, $\overline{TRST}$ , DSCK, and DSDI pins)	$I_{In}$	—	10	$\mu$ A
Input capacitance <sup>2</sup>	$C_{in}$	—	20	pF
Output high voltage, $I_{OH} = -2.0$ mA, $V_{DDH} = 3.0$ V (except XTAL, XFC, and open-drain pins)	$V_{OH}$	2.4	—	V
Output low voltage $I_{OL} = 2.0$ mA, CLKOUT $I_{OL} = 3.2$ mA <sup>3</sup> $I_{OL} = 5.3$ mA <sup>4</sup> $I_{OL} = 7.0$ mA, TXD1/PA14, TXD2/PA12 $I_{OL} = 8.9$ mA, $\overline{TS}$ , $\overline{TA}$ , $\overline{TEA}$ , $\overline{BI}$ , $\overline{BB}$ , $\overline{HRESET}$ , $\overline{SRESET}$	$V_{OL}$	—	0.5	V

<sup>1</sup>  $V_{IL}(\max)$  for the I<sup>2</sup>C interface is 0.8 V rather than the 1.5 V as specified in the I<sup>2</sup>C standard.

<sup>2</sup> Input capacitance is periodically sampled.

<sup>3</sup> A(0:31), TSIZ0/ $\overline{REG}$ , TSIZ1, D(0:31), DP(0:3)/ $\overline{IRQ}$ (3:6), RD/ $\overline{WR}$ ,  $\overline{BURST}$ ,  $\overline{RSV}/\overline{IRQ2}$ , IP\_B(0:1)/IWP(0:1)/VFLS(0:1), IP\_B2/IOIS16\_B/AT2, IP\_B3/IWP2/VF2, IP\_B4/LWP0/VF0, IP\_B5/LWP1/VF1, IP\_B6/DSDI/AT0, IP\_B7/PTR/AT3, RXD1/PA15, RXD2/PA13, L1TXDB/PA11, L1RXDB/PA10, L1TXDA/PA9, L1RXDA/PA8, TIN1/L1RCLKA/BRGO1/CLK1/PA7, BRGCLK1/ $\overline{TOUT1}/\overline{CLK2}/\overline{PA6}$ , TIN2/L1TCLKA/BRGO2/CLK3/PA5,  $\overline{TOUT2}/\overline{CLK4}/\overline{PA4}$ , TIN3/BRGO3/CLK5/PA3, BRGCLK2/L1RCLKB/ $\overline{TOUT3}/\overline{CLK6}/\overline{PA2}$ , TIN4/BRGO4/CLK7/PA1, L1TCLKB/ $\overline{TOUT4}/\overline{CLK8}/\overline{PA0}$ ,  $\overline{REJECT1}/\overline{SPISEL}/\overline{PB31}$ , SPICLK/ $\overline{PB30}$ , SPI MOSI/ $\overline{PB29}$ , BRGO4/ $\overline{SPIMISO}/\overline{PB28}$ , BRGO1/I2CSDA/ $\overline{PB27}$ , BRGO2/I2CSCL/ $\overline{PB26}$ , SMTXD1/ $\overline{PB25}$ , SMRXD1/ $\overline{PB24}$ ,  $\overline{SMSYN1}/\overline{SDACK1}/\overline{PB23}$ ,  $\overline{SMSYN2}/\overline{SDACK2}/\overline{PB22}$ , SMTXD2/L1CLKOB/ $\overline{PB21}$ , SMRXD2/L1CLKOA/ $\overline{PB20}$ , L1ST1/ $\overline{RTS1}/\overline{PB19}$ , L1ST2/ $\overline{RTS2}/\overline{PB18}$ , L1ST3/L1RQB/ $\overline{PB17}$ , L1ST4/L1RQA/ $\overline{PB16}$ , BRGO3/ $\overline{PB15}$ ,  $\overline{RSTRT1}/\overline{PB14}$ , L1ST1/ $\overline{RTS1}/\overline{DREQ0}/\overline{PC15}$ , L1ST2/ $\overline{RTS2}/\overline{DREQ1}/\overline{PC14}$ , L1ST3/L1RQB/ $\overline{PC13}$ , L1ST4/L1RQA/ $\overline{PC12}$ ,  $\overline{CTS1}/\overline{PC11}$ ,  $\overline{TGATE1}/\overline{CD1}/\overline{PC10}$ ,  $\overline{CTS2}/\overline{PC9}$ ,  $\overline{TGATE2}/\overline{CD2}/\overline{PC8}$ ,  $\overline{SDACK2}/\overline{L1TSYNCA}/\overline{PC7}$ , L1RSYNCA/ $\overline{PC6}$ ,  $\overline{SDACK1}/\overline{L1TSYNCA}/\overline{PC5}$ , L1RSYNCA/ $\overline{PC4}$ , PD15, PD14, PD13, PD12, PD11, PD10, PD9, PD8, PD5, PD6, PD7, PD4, PD3, MII\_MDC, MII\_TX\_ER, MII\_EN, MII\_MDIO, and MII\_TXD[0:3]

<sup>4</sup>  $\overline{BDIP}/\overline{GPL\_B}(5)$ ,  $\overline{BR}$ ,  $\overline{BG}$ ,  $\overline{FRZ}/\overline{IRQ6}$ ,  $\overline{CS}(0:5)$ ,  $\overline{CS}(6)/\overline{CE}(1)_B$ ,  $\overline{CS}(7)/\overline{CE}(2)_B$ ,  $\overline{WE0}/\overline{BS\_B0}/\overline{IORD}$ ,  $\overline{WE1}/\overline{BS\_B1}/\overline{IOWR}$ ,  $\overline{WE2}/\overline{BS\_B2}/\overline{PCOE}$ ,  $\overline{WE3}/\overline{BS\_B3}/\overline{PCWE}$ ,  $\overline{BS\_A}(0:3)$ ,  $\overline{GPL\_A0}/\overline{GPL\_B0}$ ,  $\overline{OE}/\overline{GPL\_A1}/\overline{GPL\_B1}$ ,  $\overline{GPL\_A}(2:3)/\overline{GPL\_B}(2:3)/\overline{CS}(2:3)$ , UPWAITA/ $\overline{GPL\_A4}$ , UPWAITB/ $\overline{GPL\_B4}$ ,  $\overline{GPL\_A5}$ , ALE\_A,  $\overline{CE1\_A}$ ,  $\overline{CE2\_A}$ , ALE\_B/DSCK/AT1, OP(0:1), OP2/MODCK1/ $\overline{STS}$ , OP3/MODCK2/DSDO, and BADDR(28:30)

## 9 Bus Signal Timing

Table 7 provides the bus operation timing for the MPC860 at 33, 40, 50, and 66 MHz.

The maximum bus speed supported by the MPC860 is 66 MHz. Higher-speed parts must be operated in half-speed bus mode (for example, an MPC860 used at 80 MHz must be configured for a 40-MHz bus).

The timing for the MPC860 bus shown assumes a 50-pF load for maximum delays and a 0-pF load for minimum delays.

**Table 7. Bus Operation Timings**

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B1	CLKOUT period	30.30	30.30	25.00	30.30	20.00	30.30	15.15	30.30	ns
B1a	EXTCLK to CLKOUT phase skew (EXTCLK > 15 MHz and MF <= 2)	-0.90	0.90	-0.90	0.90	-0.90	0.90	-0.90	0.90	ns
B1b	EXTCLK to CLKOUT phase skew (EXTCLK > 10 MHz and MF < 10)	-2.30	2.30	-2.30	2.30	-2.30	2.30	-2.30	2.30	ns
B1c	CLKOUT phase jitter (EXTCLK > 15 MHz and MF <= 2) <sup>1</sup>	-0.60	0.60	-0.60	0.60	-0.60	0.60	-0.60	0.60	ns
B1d	CLKOUT phase jitter <sup>1</sup>	-2.00	2.00	-2.00	2.00	-2.00	2.00	-2.00	2.00	ns
B1e	CLKOUT frequency jitter (MF < 10) <sup>1</sup>	—	0.50	—	0.50	—	0.50	—	0.50	%
B1f	CLKOUT frequency jitter (10 < MF < 500) <sup>1</sup>	—	2.00	—	2.00	—	2.00	—	2.00	%
B1g	CLKOUT frequency jitter (MF > 500) <sup>1</sup>	—	3.00	—	3.00	—	3.00	—	3.00	%
B1h	Frequency jitter on EXTCLK <sup>2</sup>	—	0.50	—	0.50	—	0.50	—	0.50	%
B2	CLKOUT pulse width low	12.12	—	10.00	—	8.00	—	6.06	—	ns
B3	CLKOUT width high	12.12	—	10.00	—	8.00	—	6.06	—	ns
B4	CLKOUT rise time <sup>3</sup>	—	4.00	—	4.00	—	4.00	—	4.00	ns
B5 <sup>33</sup>	CLKOUT fall time <sup>3</sup>	—	4.00	—	4.00	—	4.00	—	4.00	ns
B7	CLKOUT to A(0:31), BADDR(28:30), RD/WR, BURST, D(0:31), DP(0:3) invalid	7.58	—	6.25	—	5.00	—	3.80	—	ns
B7a	CLKOUT to TSIZ(0:1), REG, RSV, AT(0:3), BDIP, PTR invalid	7.58	—	6.25	—	5.00	—	3.80	—	ns
B7b	CLKOUT to BR, BG, FRZ, VFLS(0:1), VF(0:2) IWP(0:2), LWP(0:1), STS invalid <sup>4</sup>	7.58	—	6.25	—	5.00	—	3.80	—	ns
B8	CLKOUT to A(0:31), BADDR(28:30) RD/WR, BURST, D(0:31), DP(0:3) valid	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.04	ns
B8a	CLKOUT to TSIZ(0:1), REG, RSV, AT(0:3) BDIP, PTR valid	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.04	ns
B8b	CLKOUT to BR, BG, VFLS(0:1), VF(0:2), IWP(0:2), FRZ, LWP(0:1), STS valid <sup>4</sup>	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.04	ns

Table 7. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B29d	$\overline{WE}(0:3)$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 0	43.45	—	35.5	—	28.00	—	20.73	—	ns
B29e	$\overline{CS}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 0	43.45	—	35.5	—	28.00	—	29.73	—	ns
B29f	$\overline{WE}(0:3)$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 1	8.86	—	6.88	—	5.00	—	3.18	—	ns
B29g	$\overline{CS}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 1	8.86	—	6.88	—	5.00	—	3.18	—	ns
B29h	$\overline{WE}(0:3)$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 1	38.67	—	31.38	—	24.50	—	17.83	—	ns
B29i	$\overline{CS}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 1	38.67	—	31.38	—	24.50	—	17.83	—	ns
B30	$\overline{CS}$ , $\overline{WE}(0:3)$ negated to A(0:31), BADDR(28:30) invalid GPCM write access <sup>8</sup>	5.58	—	4.25	—	3.00	—	1.79	—	ns
B30a	$\overline{WE}(0:3)$ negated to A(0:31), BADDR(28:30) invalid GPCM, write access, TRLX = 0, CSNT = 1, $\overline{CS}$ negated to A(0:31) invalid GPCM write access, TRLX = 0, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 0	13.15	—	10.50	—	8.00	—	5.58	—	ns
B30b	$\overline{WE}(0:3)$ negated to A(0:31), invalid GPCM BADDR(28:30) invalid GPCM write access, TRLX = 1, CSNT = 1. $\overline{CS}$ negated to A(0:31), Invalid GPCM, write access, TRLX = 1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 0	43.45	—	35.50	—	28.00	—	20.73	—	ns
B30c	$\overline{WE}(0:3)$ negated to A(0:31), BADDR(28:30) invalid GPCM write access, TRLX = 0, CSNT = 1. $\overline{CS}$ negated to A(0:31) invalid GPCM write access, TRLX = 0, CSNT = 1, ACS = 10, ACS = 11, EBDF = 1	8.36	—	6.38	—	4.50	—	2.68	—	ns
B30d	$\overline{WE}(0:3)$ negated to A(0:31), BADDR(28:30) invalid GPCM write access, TRLX = 1, CSNT = 1. $\overline{CS}$ negated to A(0:31) invalid GPCM write access TRLX = 1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 1	38.67	—	31.38	—	24.50	—	17.83	—	ns
B31	CLKOUT falling edge to $\overline{CS}$ valid—as requested by control bit CST4 in the corresponding word in UPM	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns

Table 7. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B35	A(0:31), BADDR(28:30) to $\overline{CS}$ valid—as requested by control bit BST4 in the corresponding word in UPM	5.58	—	4.25	—	3.00	—	1.79	—	ns
B35a	A(0:31), BADDR(28:30), and D(0:31) to $\overline{BS}$ valid—as requested by control bit BST1 in the corresponding word in UPM	13.15	—	10.50	—	8.00	—	5.58	—	ns
B35b	A(0:31), BADDR(28:30), and D(0:31) to $\overline{BS}$ valid—as requested by control bit BST2 in the corresponding word in UPM	20.73	—	16.75	—	13.00	—	9.36	—	ns
B36	A(0:31), BADDR(28:30), and D(0:31) to $\overline{GPL}$ valid—as requested by control bit GxT4 in the corresponding word in UPM	5.58	—	4.25	—	3.00	—	1.79	—	ns
B37	UPWAIT valid to CLKOUT falling edge <sup>9</sup>	6.00	—	6.00	—	6.00	—	6.00	—	ns
B38	CLKOUT falling edge to UPWAIT valid <sup>9</sup>	1.00	—	1.00	—	1.00	—	1.00	—	ns
B39	$\overline{AS}$ valid to CLKOUT rising edge <sup>10</sup>	7.00	—	7.00	—	7.00	—	7.00	—	ns
B40	A(0:31), TSIZ(0:1), RD/ $\overline{WR}$ , $\overline{BURST}$ , valid to CLKOUT rising edge	7.00	—	7.00	—	7.00	—	7.00	—	ns
B41	$\overline{TS}$ valid to CLKOUT rising edge (setup time)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B42	CLKOUT rising edge to $\overline{TS}$ valid (hold time)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B43	$\overline{AS}$ negation to memory controller signals negation	—	TBD	—	TBD	—	TBD	—	TBD	ns

<sup>1</sup> Phase and frequency jitter performance results are only valid if the input jitter is less than the prescribed value.

<sup>2</sup> If the rate of change of the frequency of EXTAL is slow (that is, it does not jump between the minimum and maximum values in one cycle) or the frequency of the jitter is fast (that is, it does not stay at an extreme value for a long time) then the maximum allowed jitter on EXTAL can be up to 2%.

<sup>3</sup> The timings specified in B4 and B5 are based on full strength clock.

<sup>4</sup> The timing for  $\overline{BR}$  output is relevant when the MPC860 is selected to work with external bus arbiter. The timing for  $\overline{BG}$  output is relevant when the MPC860 is selected to work with internal bus arbiter.

<sup>5</sup> The timing required for  $\overline{BR}$  input is relevant when the MPC860 is selected to work with internal bus arbiter. The timing for  $\overline{BG}$  input is relevant when the MPC860 is selected to work with external bus arbiter.

<sup>6</sup> The D(0:31) and DP(0:3) input timings B18 and B19 refer to the rising edge of the CLKOUT in which the  $\overline{TA}$  input signal is asserted.

<sup>7</sup> The D(0:31) and DP(0:3) input timings B20 and B21 refer to the falling edge of the CLKOUT. This timing is valid only for read accesses controlled by chip-selects under control of the UPM in the memory controller, for data beats where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

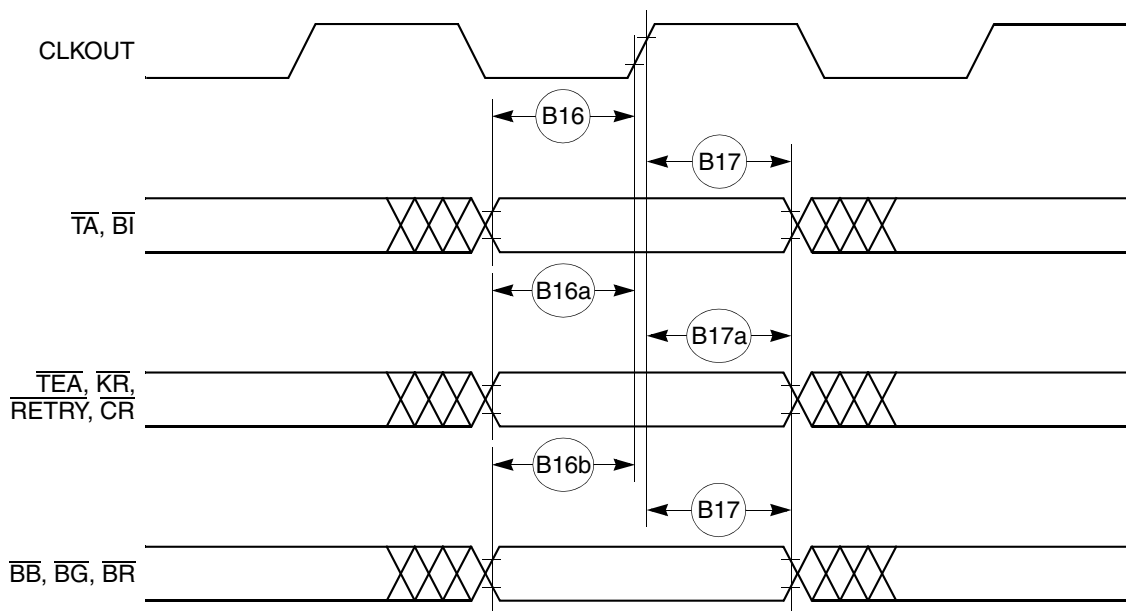
<sup>8</sup> The timing B30 refers to  $\overline{CS}$  when ACS = 00 and to  $\overline{WE}$ (0:3) when CSNT = 0.

<sup>9</sup> The signal UPWAIT is considered asynchronous to the CLKOUT and synchronized internally. The timings specified in B37 and B38 are specified to enable the freeze of the UPM output signals as described in [Figure 18](#).

<sup>10</sup> The  $\overline{AS}$  signal is considered asynchronous to the CLKOUT. The timing B39 is specified in order to allow the behavior specified in [Figure 21](#).

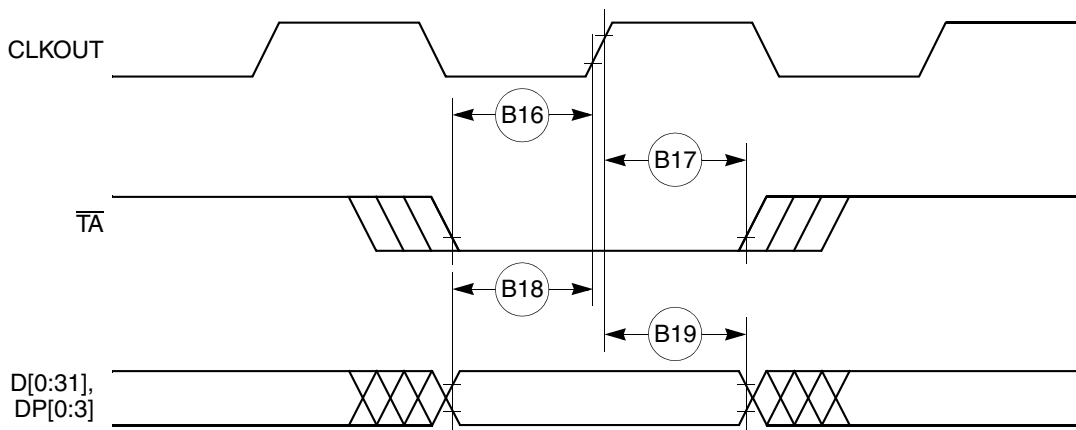


Figure 7 provides the timing for the synchronous input signals.



**Figure 7. Synchronous Input Signals Timing**

Figure 8 provides normal case timing for input data. It also applies to normal read accesses under the control of the UPM in the memory controller.



**Figure 8. Input Data Timing in Normal Case**

Figure 14 through Figure 16 provide the timing for the external bus write controlled by various GPCM factors.

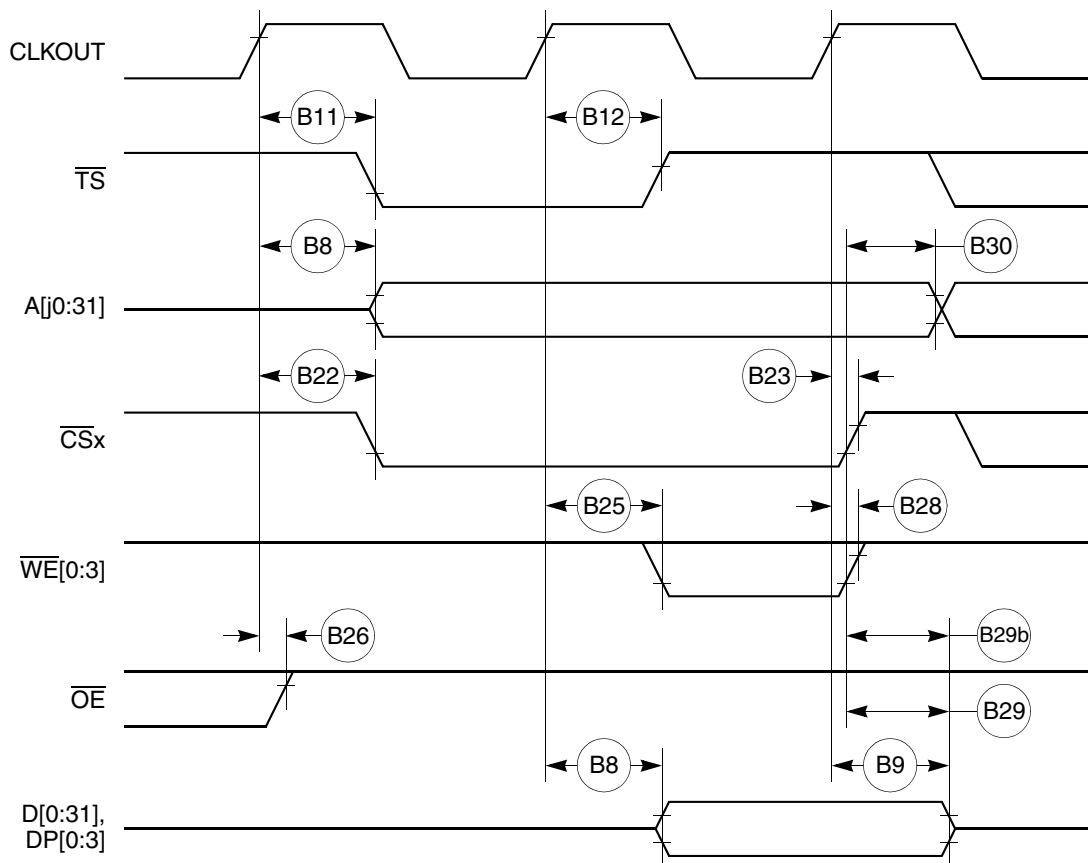


Figure 14. External Bus Write Timing (GPCM Controlled—TRLX = 0 or 1, CSNT = 0)

Table 9 shows the PCMCIA timing for the MPC860.

**Table 9. PCMCIA Timing**

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
P44	A(0:31), $\overline{\text{REG}}$ valid to PCMCIA Strobe asserted <sup>1</sup>	20.73	—	16.75	—	13.00	—	9.36	—	ns
P45	A(0:31), $\overline{\text{REG}}$ valid to ALE negation <sup>1</sup>	28.30	—	23.00	—	18.00	—	13.15	—	ns
P46	CLKOUT to $\overline{\text{REG}}$ valid	7.58	15.58	6.25	14.25	5.00	13.00	3.79	11.84	ns
P47	CLKOUT to $\overline{\text{REG}}$ invalid	8.58	—	7.25	—	6.00	—	4.84	—	ns
P48	CLKOUT to $\overline{\text{CE1}}$ , $\overline{\text{CE2}}$ asserted	7.58	15.58	6.25	14.25	5.00	13.00	3.79	11.84	ns
P49	CLKOUT to $\overline{\text{CE1}}$ , $\overline{\text{CE2}}$ negated	7.58	15.58	6.25	14.25	5.00	13.00	3.79	11.84	ns
P50	CLKOUT to $\overline{\text{PCOE}}$ , $\overline{\text{IORD}}$ , $\overline{\text{PCWE}}$ , $\overline{\text{IOWR}}$ assert time	—	11.00		11.00	—	11.00	—	11.00	ns
P51	CLKOUT to $\overline{\text{PCOE}}$ , $\overline{\text{IORD}}$ , $\overline{\text{PCWE}}$ , $\overline{\text{IOWR}}$ negate time	2.00	11.00	2.00	11.00	2.00	11.00	2.00	11.00	ns
P52	CLKOUT to ALE assert time	7.58	15.58	6.25	14.25	5.00	13.00	3.79	10.04	ns
P53	CLKOUT to ALE negate time	—	15.58		14.25	—	13.00	—	11.84	ns
P54	$\overline{\text{PCWE}}$ , $\overline{\text{IOWR}}$ negated to D(0:31) invalid <sup>1</sup>	5.58	—	4.25	—	3.00	—	1.79	—	ns
P55	$\overline{\text{WAITA}}$ and $\overline{\text{WAITB}}$ valid to CLKOUT rising edge <sup>1</sup>	8.00	—	8.00	—	8.00	—	8.00	—	ns
P56	CLKOUT rising edge to $\overline{\text{WAITA}}$ and $\overline{\text{WAITB}}$ invalid <sup>1</sup>	2.00	—	2.00	—	2.00	—	2.00	—	ns

<sup>1</sup> PSST = 1. Otherwise add PSST times cycle time.

PSHT = 0. Otherwise add PSHT times cycle time.

These synchronous timings define when the  $\overline{\text{WAITx}}$  signals are detected in order to freeze (or relieve) the PCMCIA current cycle. The  $\overline{\text{WAITx}}$  assertion will be effective only if it is detected 2 cycles before the PSL timer expiration. See Chapter 16, “PCMCIA Interface,” in the *MPC860 PowerQUICC™ Family User's Manual*.

Figure 25 provides the PCMCIA access cycle timing for the external bus read.

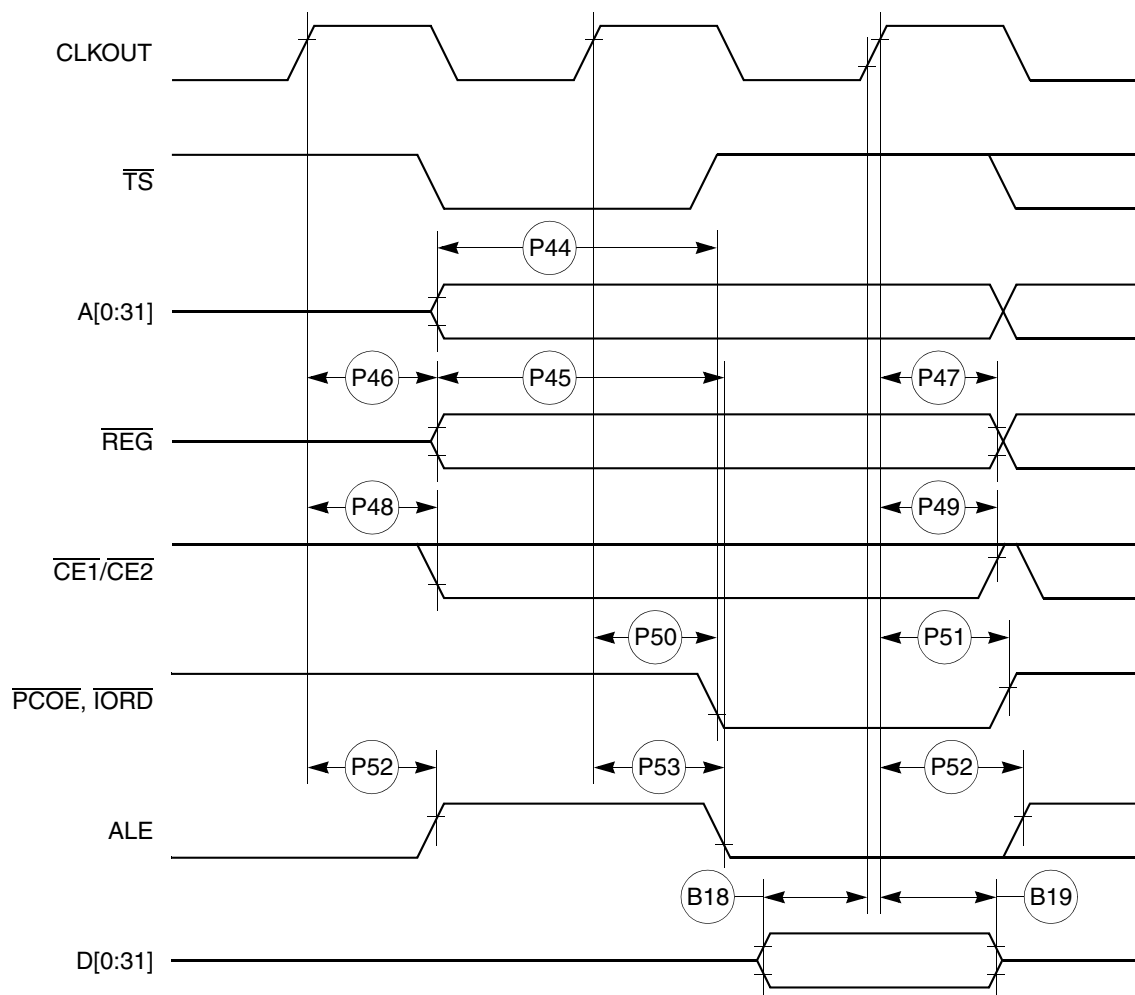


Figure 25. PCMCIA Access Cycle Timing External Bus Read

Figure 26 provides the PCMCIA access cycle timing for the external bus write.

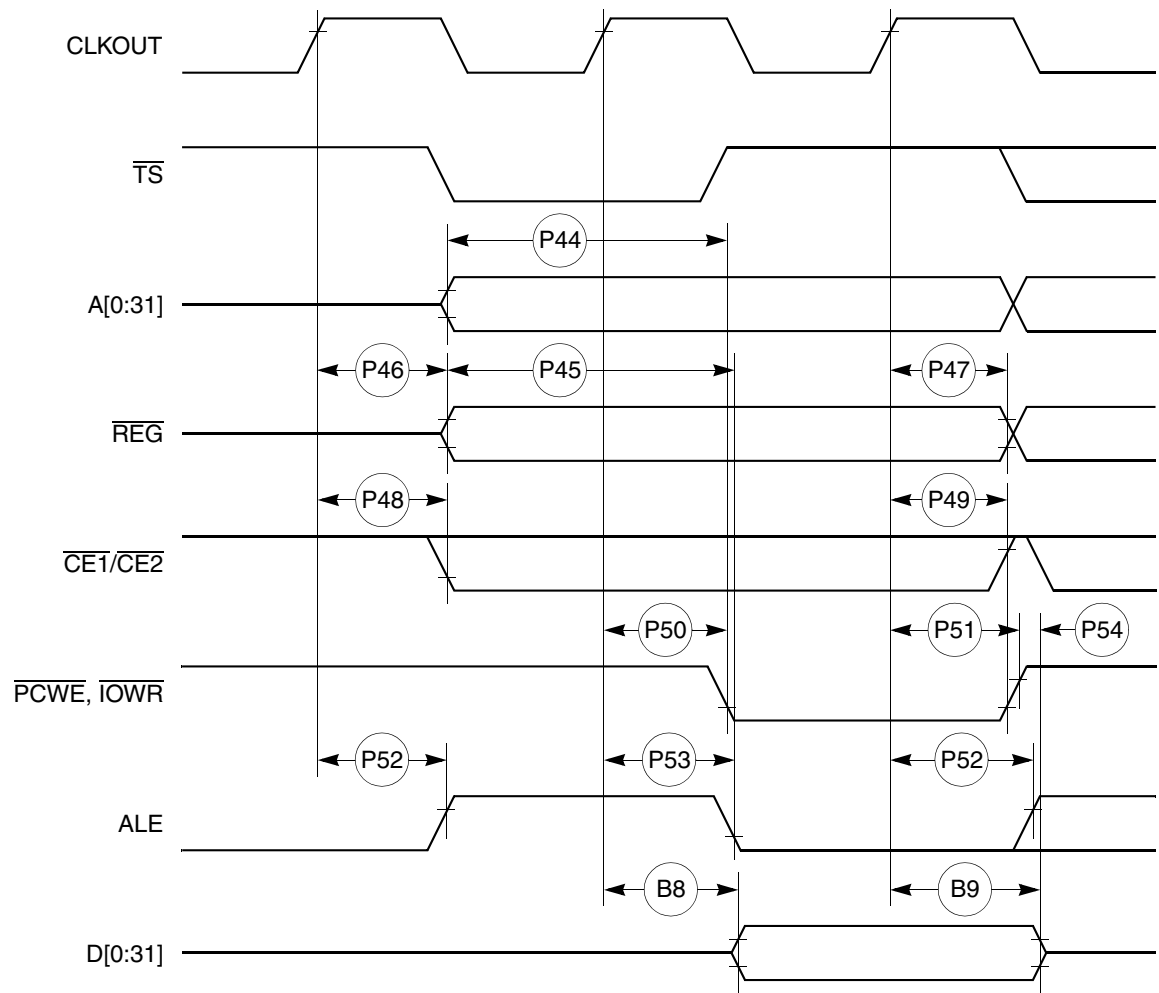


Figure 26. PCMCIA Access Cycle Timing External Bus Write

Figure 27 provides the PCMCIA  $\overline{\text{WAIT}}$  signal detection timing.

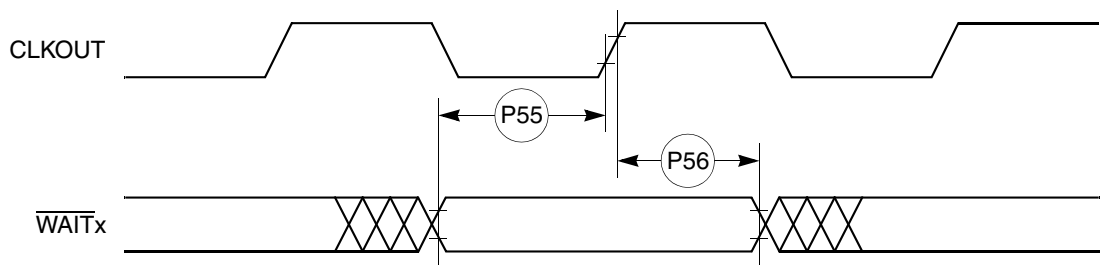


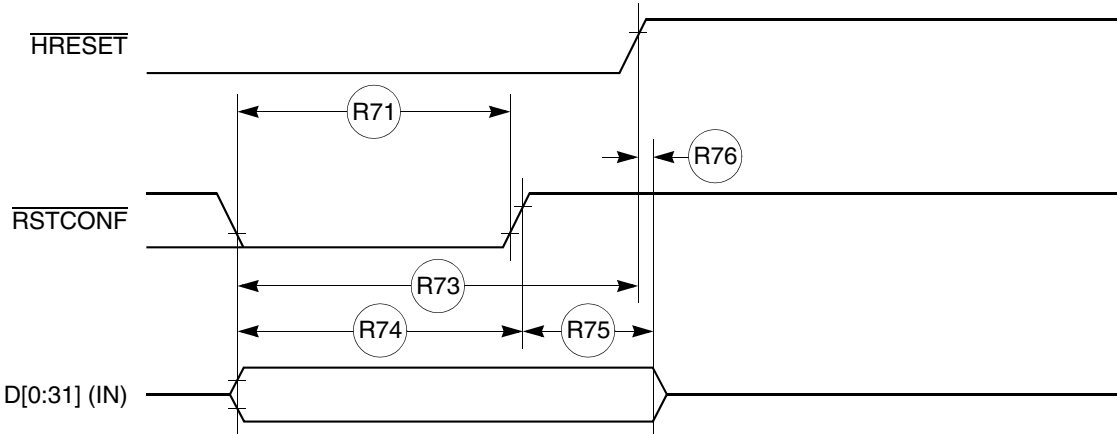
Figure 27. PCMCIA  $\overline{\text{WAIT}}$  Signal Detection Timing

Table 12 shows the reset timing for the MPC860.

**Table 12. Reset Timing**

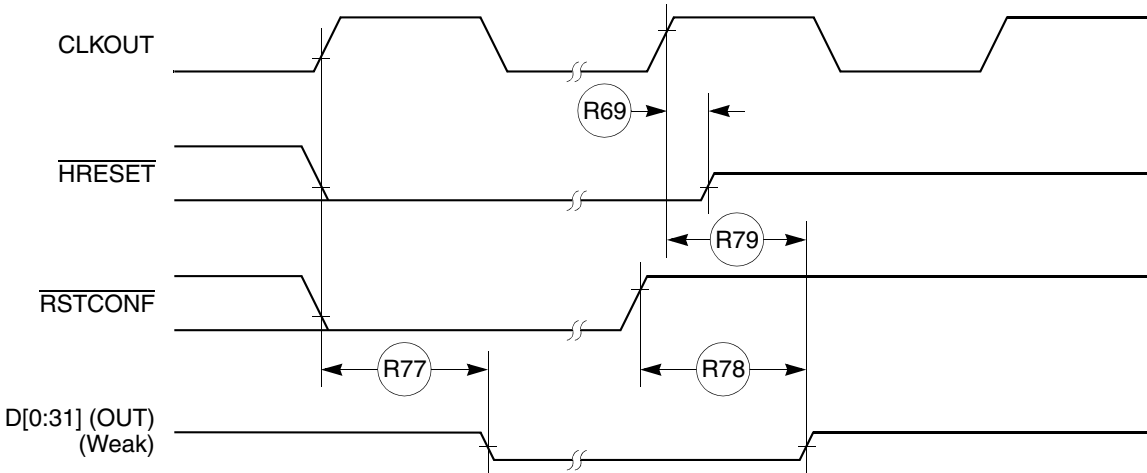
Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
R69	CLKOUT to $\overline{\text{HRESET}}$ high impedance	—	20.00	—	20.00	—	20.00	—	20.00	ns
R70	CLKOUT to $\overline{\text{SRESET}}$ high impedance	—	20.00	—	20.00	—	20.00	—	20.00	ns
R71	$\overline{\text{RSTCONF}}$ pulse width	515.15	—	425.00	—	340.00	—	257.58	—	ns
R72	—	—	—	—	—	—	—	—	—	
R73	Configuration data to $\overline{\text{HRESET}}$ rising edge setup time	504.55	—	425.00	—	350.00	—	277.27	—	ns
R74	Configuration data to $\overline{\text{RSTCONF}}$ rising edge setup time	350.00	—	350.00	—	350.00	—	350.00	—	ns
R75	Configuration data hold time after $\overline{\text{RSTCONF}}$ negation	0.00	—	0.00	—	0.00	—	0.00	—	ns
R76	Configuration data hold time after $\overline{\text{HRESET}}$ negation	0.00	—	0.00	—	0.00	—	0.00	—	ns
R77	$\overline{\text{HRESET}}$ and $\overline{\text{RSTCONF}}$ asserted to data out drive	—	25.00	—	25.00	—	25.00	—	25.00	ns
R78	$\overline{\text{RSTCONF}}$ negated to data out high impedance	—	25.00	—	25.00	—	25.00	—	25.00	ns
R79	CLKOUT of last rising edge before chip three-state $\overline{\text{HRESET}}$ to data out high impedance	—	25.00	—	25.00	—	25.00	—	25.00	ns
R80	DSDI, DSCK setup	90.91	—	75.00	—	60.00	—	45.45	—	ns
R81	DSDI, DSCK hold time	0.00	—	0.00	—	0.00	—	0.00	—	ns
R82	$\overline{\text{SRESET}}$ negated to CLKOUT rising edge for DSDI and DSCK sample	242.42	—	200.00	—	160.00	—	121.21	—	ns

Figure 32 shows the reset timing for the data bus configuration.



**Figure 32. Reset Timing—Configuration from Data Bus**

Figure 33 provides the reset timing for the data bus weak drive during configuration.



**Figure 33. Reset Timing—Data Bus Weak Drive During Configuration**

# 11.4 Baud Rate Generator AC Electrical Specifications

Table 17 provides the baud rate generator timings as shown in Figure 49.

Table 17. Baud Rate Generator Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
50	BRGO rise and fall time	—	10	ns
51	BRGO duty cycle	40	60	%
52	BRGO cycle	40	—	ns

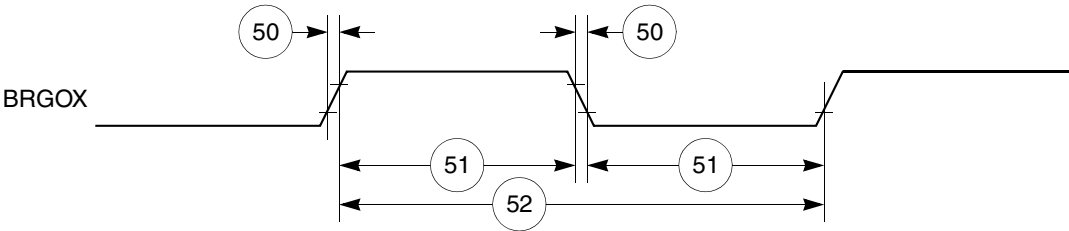


Figure 49. Baud Rate Generator Timing Diagram

# 11.5 Timer AC Electrical Specifications

Table 18 provides the general-purpose timer timings as shown in Figure 50.

Table 18. Timer Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
61	TIN/TGATE rise and fall time	10	—	ns
62	TIN/TGATE low time	1	—	CLK
63	TIN/TGATE high time	2	—	CLK
64	TIN/TGATE cycle time	3	—	CLK
65	CLKO low to TOUT valid	3	25	ns



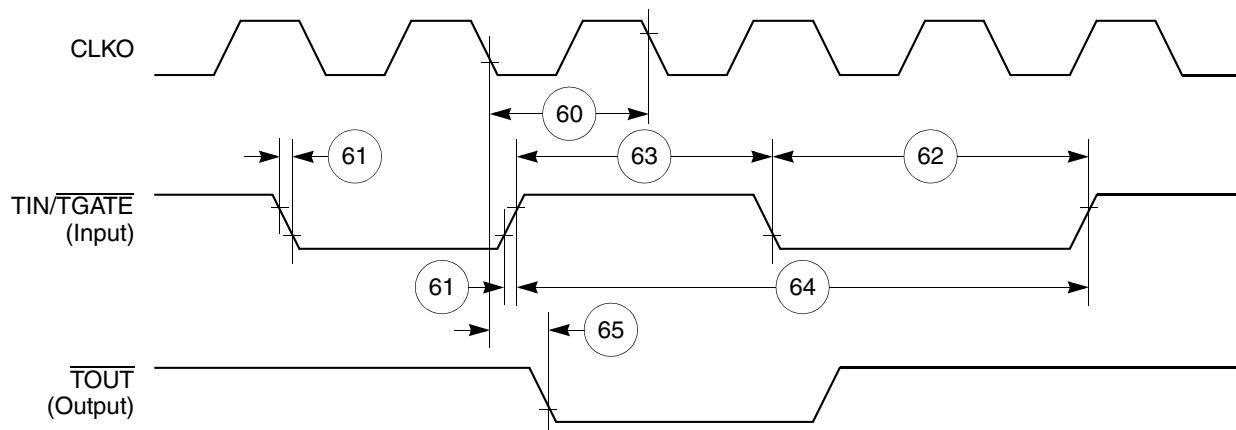


Figure 50. CPM General-Purpose Timers Timing Diagram

## 11.6 Serial Interface AC Electrical Specifications

Table 19 provides the serial interface timings as shown in Figure 51 through Figure 55.

Table 19. SI Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
70	L1RCLK, L1TCLK frequency (DSC = 0) <sup>1, 2</sup>	—	SYNCCLK/2.5	MHz
71	L1RCLK, L1TCLK width low (DSC = 0) <sup>2</sup>	P + 10	—	ns
71a	L1RCLK, L1TCLK width high (DSC = 0) <sup>3</sup>	P + 10	—	ns
72	L1TXD, L1ST(1–4), $\overline{\text{L1RQ}}$ , L1CLKO rise/fall time	—	15.00	ns
73	L1RSYNC, L1TSYNC valid to L1CLK edge (SYNC setup time)	20.00	—	ns
74	L1CLK edge to L1RSYNC, L1TSYNC, invalid (SYNC hold time)	35.00	—	ns
75	L1RSYNC, L1TSYNC rise/fall time	—	15.00	ns
76	L1RXD valid to L1CLK edge (L1RXD setup time)	17.00	—	ns
77	L1CLK edge to L1RXD invalid (L1RXD hold time)	13.00	—	ns
78	L1CLK edge to L1ST(1–4) valid <sup>4</sup>	10.00	45.00	ns
78A	L1SYNC valid to L1ST(1–4) valid	10.00	45.00	ns
79	L1CLK edge to L1ST(1–4) invalid	10.00	45.00	ns
80	L1CLK edge to L1TXD valid	10.00	55.00	ns
80A	L1TSYNC valid to L1TXD valid <sup>4</sup>	10.00	55.00	ns
81	L1CLK edge to L1TXD high impedance	0.00	42.00	ns
82	L1RCLK, L1TCLK frequency (DSC = 1)	—	16.00 or SYNCCLK/2	MHz
83	L1RCLK, L1TCLK width low (DSC = 1)	P + 10	—	ns
83a	L1RCLK, L1TCLK width high (DSC = 1) <sup>3</sup>	P + 10	—	ns

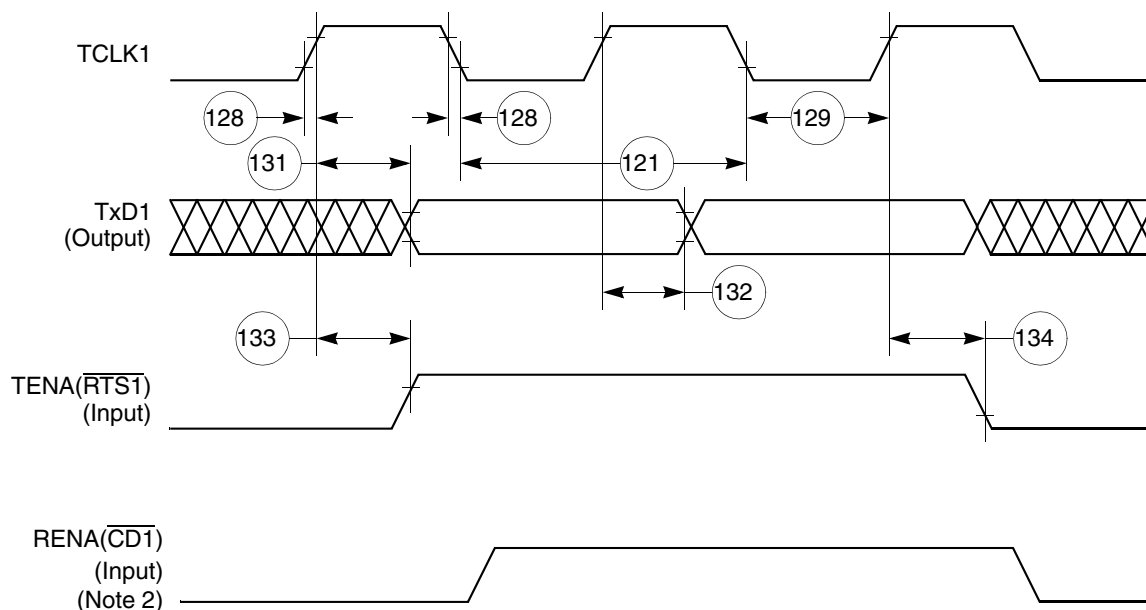


Figure 61. Ethernet Transmit Timing Diagram

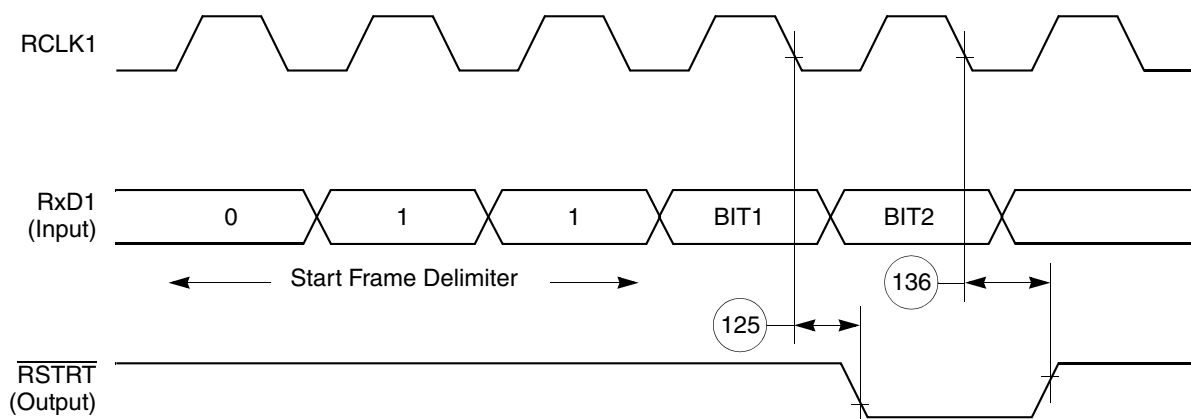


Figure 62. CAM Interface Receive Start Timing Diagram



Figure 63. CAM Interface  $\overline{\text{REJECT}}$  Timing Diagram

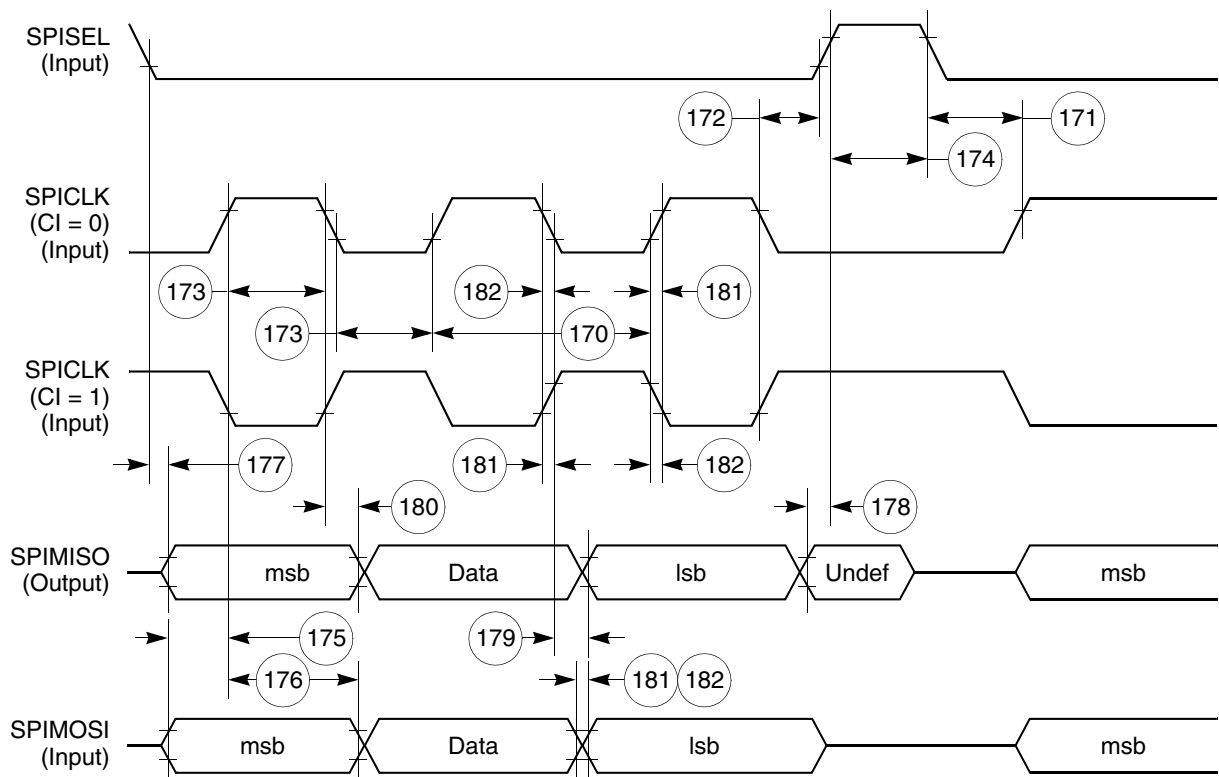


Figure 67. SPI Slave (CP = 0) Timing Diagram

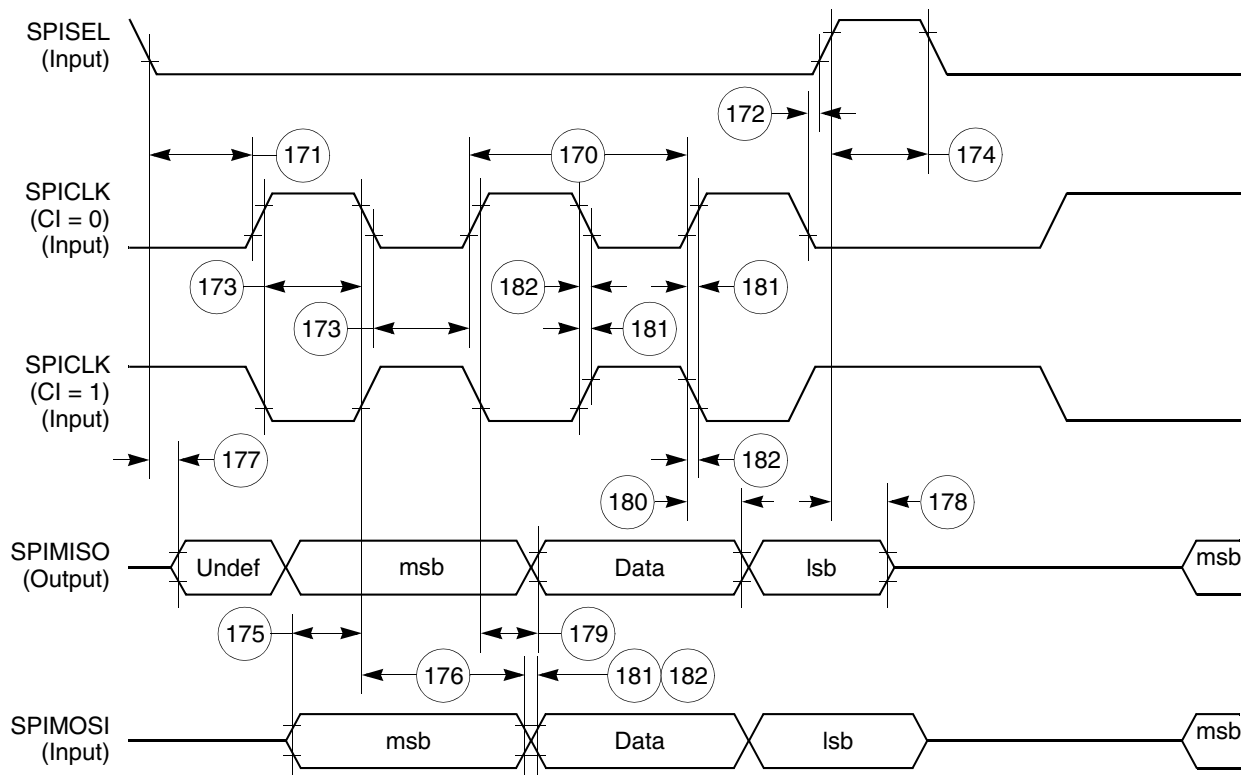


Figure 68. SPI Slave (CP = 1) Timing Diagram

Figure 75 shows the MII serial management channel timing diagram.

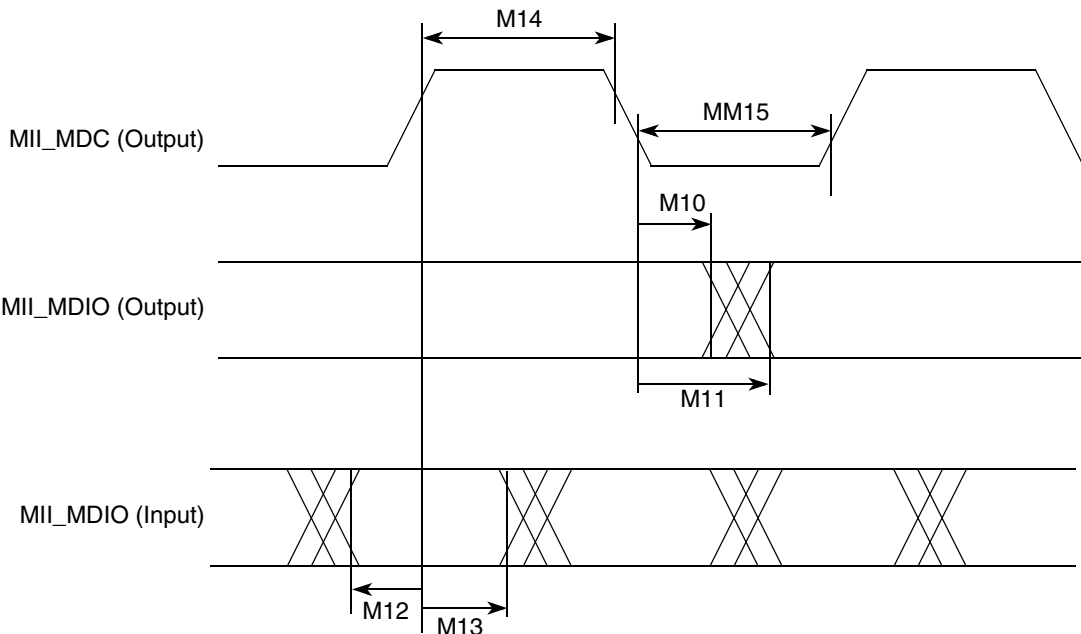


Figure 75. MII Serial Management Channel Timing Diagram

# 14 Mechanical Data and Ordering Information

## 14.1 Ordering Information

Table 33 provides information on the MPC860 Revision D.4 derivative devices.

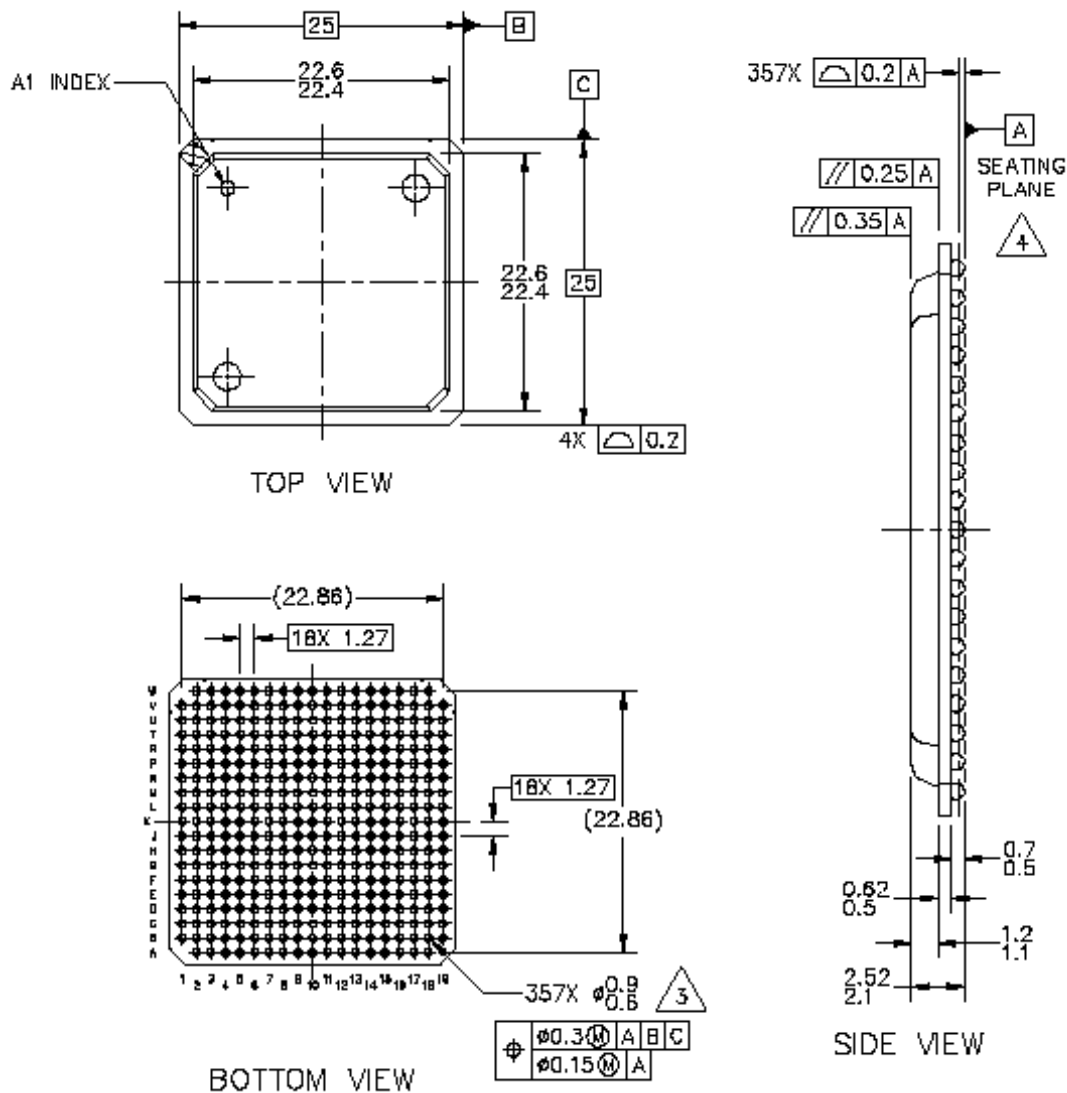
Table 33. MPC860 Family Revision D.4 Derivatives

Device	Number of SCCs <sup>1</sup>	Ethernet Support <sup>2</sup> (Mbps)	Multichannel HDLC Support	ATM Support
MPC855T	1	10/100	Yes	Yes
MPC860DE	2	10	N/A	N/A
MPC860DT		10/100	Yes	Yes
MPC860DP		10/100	Yes	Yes
MPC860EN	4	10	N/A	N/A
MPC860SR		10	Yes	Yes
MPC860T		10/100	Yes	Yes
MPC860P		10/100	Yes	Yes

<sup>1</sup> Serial communications controller (SCC)

<sup>2</sup> Up to 4 channels at 40 MHz or 2 channels at 25 MHz

Figure 78 shows the mechanical dimensions of the ZQ PBGA package.



**Figure 78. Mechanical Dimensions and Bottom Surface Nomenclature of the ZQ PBGA Package**