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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | MPC8xx |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 80MHz |
| Co-Processors/DSP | Communications; CPM |
| RAM Controllers | DRAM |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 10Mbps (4), 10/100Mbps (1) |
| SATA | - |
| USB | - |
| Voltage - I/O | 3.3V |
| Operating Temperature | 0°C ~ 95°C (TA) |
| Security Features | - |
| Package / Case | 357-BBGA |
| Supplier Device Package | 357-PBGA (25x25) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc860pvr80d4r2 |

# 1 Overview

The MPC860 power quad integrated communications controller (PowerQUICC™) is a versatile one-chip integrated microprocessor and peripheral combination designed for a variety of controller applications. It particularly excels in communications and networking systems. The PowerQUICC unit is referred to as the MPC860 in this hardware specification.

The MPC860 implements Power Architecture™ technology and contains a superset of Freescale's MC68360 quad integrated communications controller (QUICC), referred to here as the QUICC, RISC communications proccessor module (CPM). The CPU on the MPC860 is a 32-bit core built on Power Architecture technology that incorporates memory management units (MMUs) and instruction and data caches.. The CPM from the MC68360 QUICC has been enhanced by the addition of the inter-integrated controller ($I^2C$) channel. The memory controller has been enhanced, enabling the MPC860 to support any type of memory, including high-performance memories and new types of DRAMs. A PCMCIA socket controller supports up to two sockets. A real-time clock has also been integrated.

Table 1 shows the functionality supported by the MPC860 family.

**Table 1. MPC860 Family Functionality**

| Part | Cache (Kbytes) | | Ethernet | | ATM | SCC | Reference[1] |
|---|---|---|---|---|---|---|---|
| | Instruction Cache | Data Cache | 10T | 10/100 | | | |
| MPC860DE | 4 | 4 | Up to 2 | — | — | 2 | 1 |
| MPC860DT | 4 | 4 | Up to 2 | 1 | Yes | 2 | 1 |
| MPC860DP | 16 | 8 | Up to 2 | 1 | Yes | 2 | 1 |
| MPC860EN | 4 | 4 | Up to 4 | — | — | 4 | 1 |
| MPC860SR | 4 | 4 | Up to 4 | — | Yes | 4 | 1 |
| MPC860T | 4 | 4 | Up to 4 | 1 | Yes | 4 | 1 |
| MPC860P | 16 | 8 | Up to 4 | 1 | Yes | 4 | 1 |
| MPC855T | 4 | 4 | 1 | 1 | Yes | 1 | 2 |

[1] Supporting documentation for these devices refers to the following:
1. MPC860 PowerQUICC Family User's Manual (MPC860UM, Rev. 3)
2. MPC855T User's Manual (MPC855TUM, Rev. 1)

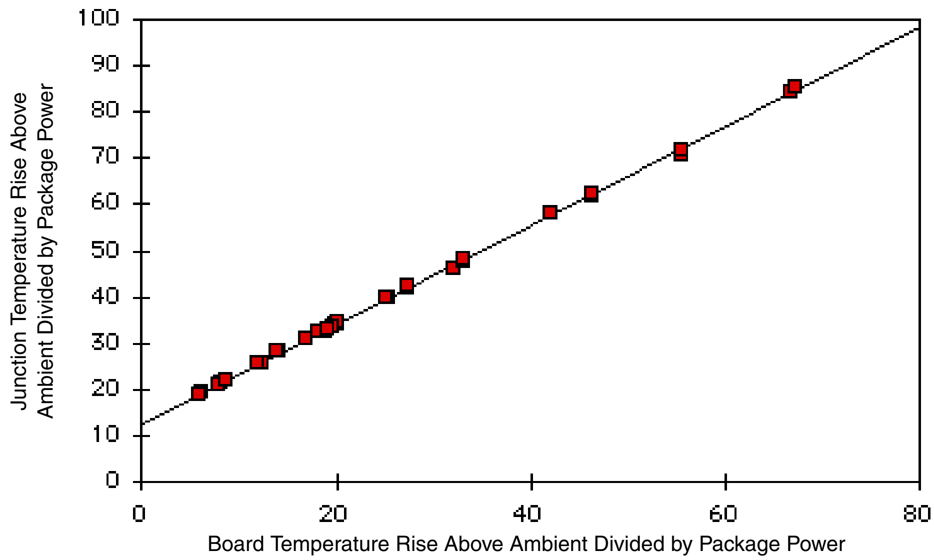



**Figure 2. Effect of Board Temperature Rise on Thermal Behavior**

If the board temperature is known, an estimate of the junction temperature in the environment can be made using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

$R_{\theta JB}$ = junction-to-board thermal resistance (ºC/W)

$T_B$ = board temperature (ºC)

$P_D$ = power dissipation in package

If the board temperature is known and the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. For this method to work, the board and board mounting must be similar to the test board used to determine the junction-to-board thermal resistance, namely a 2s2p (board with a power and a ground plane) and by attaching the thermal balls to the ground plane.

## 7.4 Estimation Using Simulation

When the board temperature is not known, a thermal simulation of the application is needed. The simple two-resistor model can be used with the thermal simulation of the application [2], or a more accurate and complex model of the package can be used in the thermal simulation.

## 7.5 Experimental Determination

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter ($\Psi_{JT}$) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

# 9 Bus Signal Timing

Table 7 provides the bus operation timing for the MPC860 at 33, 40, 50, and 66 MHz.

The maximum bus speed supported by the MPC860 is 66 MHz. Higher-speed parts must be operated in half-speed bus mode (for example, an MPC860 used at 80 MHz must be configured for a 40-MHz bus).

The timing for the MPC860 bus shown assumes a 50-pF load for maximum delays and a 0-pF load for minimum delays.

**Table 7. Bus Operation Timings**

| Num | Characteristic | 33 MHz | | 40 MHz | | 50 MHz | | 66 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| B1 | CLKOUT period | 30.30 | 30.30 | 25.00 | 30.30 | 20.00 | 30.30 | 15.15 | 30.30 | ns |
| B1a | EXTCLK to CLKOUT phase skew (EXTCLK > 15 MHz and MF <= 2) | –0.90 | 0.90 | –0.90 | 0.90 | –0.90 | 0.90 | –0.90 | 0.90 | ns |
| B1b | EXTCLK to CLKOUT phase skew (EXTCLK > 10 MHz and MF < 10) | –2.30 | 2.30 | –2.30 | 2.30 | –2.30 | 2.30 | –2.30 | 2.30 | ns |
| B1c | CLKOUT phase jitter (EXTCLK > 15 MHz and MF <= 2)[1] | –0.60 | 0.60 | –0.60 | 0.60 | –0.60 | 0.60 | –0.60 | 0.60 | ns |
| B1d | CLKOUT phase jitter[1] | –2.00 | 2.00 | –2.00 | 2.00 | –2.00 | 2.00 | –2.00 | 2.00 | ns |
| B1e | CLKOUT frequency jitter (MF < 10)[1] | — | 0.50 | — | 0.50 | — | 0.50 | — | 0.50 | % |
| B1f | CLKOUT frequency jitter (10 < MF < 500)[1] | — | 2.00 | — | 2.00 | — | 2.00 | — | 2.00 | % |
| B1g | CLKOUT frequency jitter (MF > 500)[1] | — | 3.00 | — | 3.00 | — | 3.00 | — | 3.00 | % |
| B1h | Frequency jitter on EXTCLK[2] | — | 0.50 | — | 0.50 | — | 0.50 | — | 0.50 | % |
| B2 | CLKOUT pulse width low | 12.12 | — | 10.00 | — | 8.00 | — | 6.06 | — | ns |
| B3 | CLKOUT width high | 12.12 | — | 10.00 | — | 8.00 | — | 6.06 | — | ns |
| B4 | CLKOUT rise time[3] | — | 4.00 | — | 4.00 | — | 4.00 | — | 4.00 | ns |
| B5[33] | CLKOUT fall time[3] | — | 4.00 | — | 4.00 | — | 4.00 | — | 4.00 | ns |
| B7 | CLKOUT to A(0:31), BADDR(28:30), RD/$\overline{\text{WR}}$, $\overline{\text{BURST}}$, D(0:31), DP(0:3) invalid | 7.58 | — | 6.25 | — | 5.00 | — | 3.80 | — | ns |
| B7a | CLKOUT to TSIZ(0:1), $\overline{\text{REG}}$, $\overline{\text{RSV}}$, AT(0:3), $\overline{\text{BDIP}}$, PTR invalid | 7.58 | — | 6.25 | — | 5.00 | — | 3.80 | — | ns |
| B7b | CLKOUT to $\overline{\text{BR}}$, $\overline{\text{BG}}$, FRZ, VFLS(0:1), VF(0:2) IWP(0:2), LWP(0:1), $\overline{\text{STS}}$ invalid [4] | 7.58 | — | 6.25 | — | 5.00 | — | 3.80 | — | ns |
| B8 | CLKOUT to A(0:31), BADDR(28:30) RD/$\overline{\text{WR}}$, $\overline{\text{BURST}}$, D(0:31), DP(0:3) valid | 7.58 | 14.33 | 6.25 | 13.00 | 5.00 | 11.75 | 3.80 | 10.04 | ns |
| B8a | CLKOUT to TSIZ(0:1), $\overline{\text{REG}}$, $\overline{\text{RSV}}$, AT(0:3) $\overline{\text{BDIP}}$, PTR valid | 7.58 | 14.33 | 6.25 | 13.00 | 5.00 | 11.75 | 3.80 | 10.04 | ns |
| B8b | CLKOUT to $\overline{\text{BR}}$, $\overline{\text{BG}}$, VFLS(0:1), VF(0:2), IWP(0:2), FRZ, LWP(0:1), $\overline{\text{STS}}$ valid [4] | 7.58 | 14.33 | 6.25 | 13.00 | 5.00 | 11.75 | 3.80 | 10.04 | ns |

**Table 7. Bus Operation Timings (continued)**

| Num | Characteristic | 33 MHz | | 40 MHz | | 50 MHz | | 66 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| B29d | $\overline{\text{WE}}$(0:3) negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 0 | 43.45 | — | 35.5 | — | 28.00 | — | 20.73 | — | ns |
| B29e | $\overline{\text{CS}}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 0 | 43.45 | — | 35.5 | — | 28.00 | — | 29.73 | — | ns |
| B29f | $\overline{\text{WE}}$(0:3) negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 1 | 8.86 | — | 6.88 | — | 5.00 | — | 3.18 | — | ns |
| B29g | $\overline{\text{CS}}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 1 | 8.86 | — | 6.88 | — | 5.00 | — | 3.18 | — | ns |
| B29h | $\overline{\text{WE}}$(0:3) negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 1 | 38.67 | — | 31.38 | — | 24.50 | — | 17.83 | — | ns |
| B29i | $\overline{\text{CS}}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 1 | 38.67 | — | 31.38 | — | 24.50 | — | 17.83 | — | ns |
| B30 | $\overline{\text{CS}}$, $\overline{\text{WE}}$(0:3) negated to A(0:31), BADDR(28:30) invalid GPCM write access [8] | 5.58 | — | 4.25 | — | 3.00 | — | 1.79 | — | ns |
| B30a | $\overline{\text{WE}}$(0:3) negated to A(0:31), BADDR(28:30) invalid GPCM, write access, TRLX = 0, CSNT = 1, $\overline{\text{CS}}$ negated to A(0:31) invalid GPCM write access, TRLX = 0, CSNT = 1 ACS = 10, or ACS = 11, EBDF = 0 | 13.15 | — | 10.50 | — | 8.00 | — | 5.58 | — | ns |
| B30b | $\overline{\text{WE}}$(0:3) negated to A(0:31), invalid GPCM BADDR(28:30) invalid GPCM write access, TRLX = 1, CSNT = 1. $\overline{\text{CS}}$ negated to A(0:31), Invalid GPCM, write access, TRLX = 1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 0 | 43.45 | — | 35.50 | — | 28.00 | — | 20.73 | — | ns |
| B30c | $\overline{\text{WE}}$(0:3) negated to A(0:31), BADDR(28:30) invalid GPCM write access, TRLX = 0, CSNT = 1. $\overline{\text{CS}}$ negated to A(0:31) invalid GPCM write access, TRLX = 0, CSNT = 1, ACS = 10, ACS = 11, EBDF = 1 | 8.36 | — | 6.38 | — | 4.50 | — | 2.68 | — | ns |
| B30d | $\overline{\text{WE}}$(0:3) negated to A(0:31), BADDR(28:30) invalid GPCM write access, TRLX = 1, CSNT =1. $\overline{\text{CS}}$ negated to A(0:31) invalid GPCM write access TRLX = 1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 1 | 38.67 | — | 31.38 | — | 24.50 | — | 17.83 | — | ns |
| B31 | CLKOUT falling edge to $\overline{\text{CS}}$ valid—as requested by control bit CST4 in the corresponding word in UPM | 1.50 | 6.00 | 1.50 | 6.00 | 1.50 | 6.00 | 1.50 | 6.00 | ns |

**Table 7. Bus Operation Timings (continued)**

| Num | Characteristic | 33 MHz | | 40 MHz | | 50 MHz | | 66 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| B31a | CLKOUT falling edge to $\overline{\text{CS}}$ valid—as requested by control bit CST1 in the corresponding word in UPM | 7.58 | 14.33 | 6.25 | 13.00 | 5.00 | 11.75 | 3.80 | 10.54 | ns |
| B31b | CLKOUT rising edge to $\overline{\text{CS}}$ valid—as requested by control bit CST2 in the corresponding word in UPM | 1.50 | 8.00 | 1.50 | 8.00 | 1.50 | 8.00 | 1.50 | 8.00 | ns |
| B31c | CLKOUT rising edge to $\overline{\text{CS}}$ valid—as requested by control bit CST3 in the corresponding word in UPM | 7.58 | 14.33 | 6.25 | 13.00 | 5.00 | 11.75 | 3.80 | 10.04 | ns |
| B31d | CLKOUT falling edge to $\overline{\text{CS}}$ valid—as requested by control bit CST1 in the corresponding word in UPM, EBDF = 1 | 13.26 | 17.99 | 11.28 | 16.00 | 9.40 | 14.13 | 7.58 | 12.31 | ns |
| B32 | CLKOUT falling edge to $\overline{\text{BS}}$ valid—as requested by control bit BST4 in the corresponding word in UPM | 1.50 | 6.00 | 1.50 | 6.00 | 1.50 | 6.00 | 1.50 | 6.00 | ns |
| B32a | CLKOUT falling edge to $\overline{\text{BS}}$ valid—as requested by control bit BST1 in the corresponding word in UPM, EBDF = 0 | 7.58 | 14.33 | 6.25 | 13.00 | 5.00 | 11.75 | 3.80 | 10.54 | ns |
| B32b | CLKOUT rising edge to $\overline{\text{BS}}$ valid—as requested by control bit BST2 in the corresponding word in UPM | 1.50 | 8.00 | 1.50 | 8.00 | 1.50 | 8.00 | 1.50 | 8.00 | ns |
| B32c | CLKOUT rising edge to $\overline{\text{BS}}$ valid—as requested by control bit BST3 in the corresponding word in UPM | 7.58 | 14.33 | 6.25 | 13.00 | 5.00 | 11.75 | 3.80 | 10.54 | ns |
| B32d | CLKOUT falling edge to $\overline{\text{BS}}$ valid—as requested by control bit BST1 in the corresponding word in UPM, EBDF = 1 | 13.26 | 17.99 | 11.28 | 16.00 | 9.40 | 14.13 | 7.58 | 12.31 | ns |
| B33 | CLKOUT falling edge to $\overline{\text{GPL}}$ valid—as requested by control bit GxT4 in the corresponding word in UPM | 1.50 | 6.00 | 1.50 | 6.00 | 1.50 | 6.00 | 1.50 | 6.00 | ns |
| B33a | CLKOUT rising edge to $\overline{\text{GPL}}$ valid—as requested by control bit GxT3 in the corresponding word in UPM | 7.58 | 14.33 | 6.25 | 13.00 | 5.00 | 11.75 | 3.80 | 10.54 | ns |
| B34 | A(0:31), BADDR(28:30), and D(0:31) to $\overline{\text{CS}}$ valid—as requested by control bit CST4 in the corresponding word in UPM | 5.58 | — | 4.25 | — | 3.00 | — | 1.79 | — | ns |
| B34a | A(0:31), BADDR(28:30), and D(0:31) to $\overline{\text{CS}}$ valid—as requested by control bit CST1 in the corresponding word in UPM | 13.15 | — | 10.50 | — | 8.00 | — | 5.58 | — | ns |
| B34b | A(0:31), BADDR(28:30), and D(0:31) to $\overline{\text{CS}}$ valid—as requested by control bit CST2 in the corresponding word in UPM | 20.73 | — | 16.75 | — | 13.00 | — | 9.36 | — | ns |

Figure 7 provides the timing for the synchronous input signals.

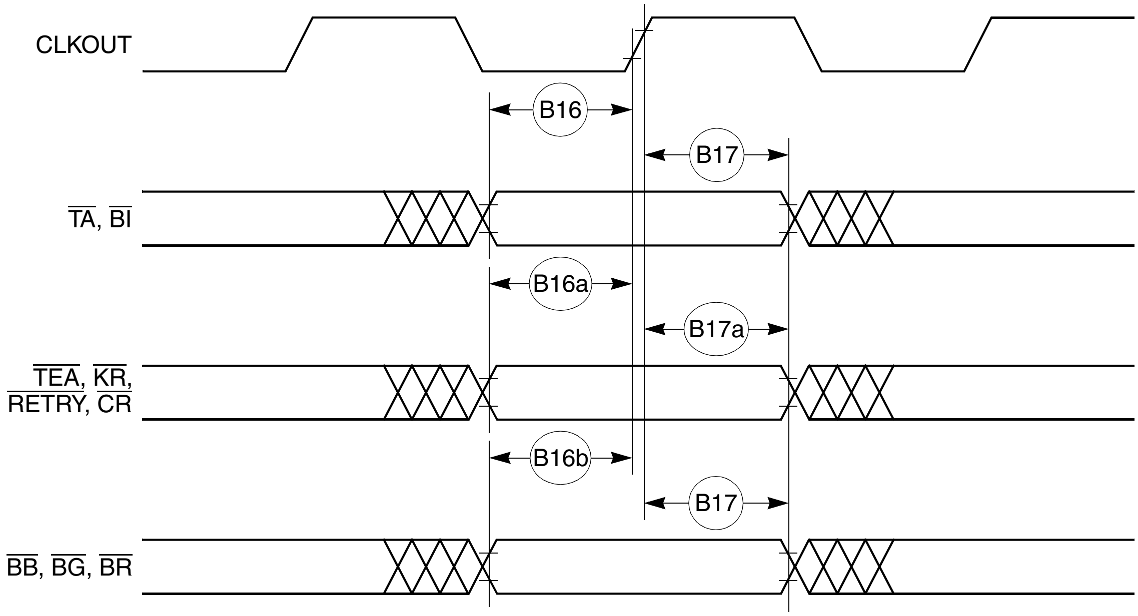



**Figure 7. Synchronous Input Signals Timing**

Figure 8 provides normal case timing for input data. It also applies to normal read accesses under the control of the UPM in the memory controller.

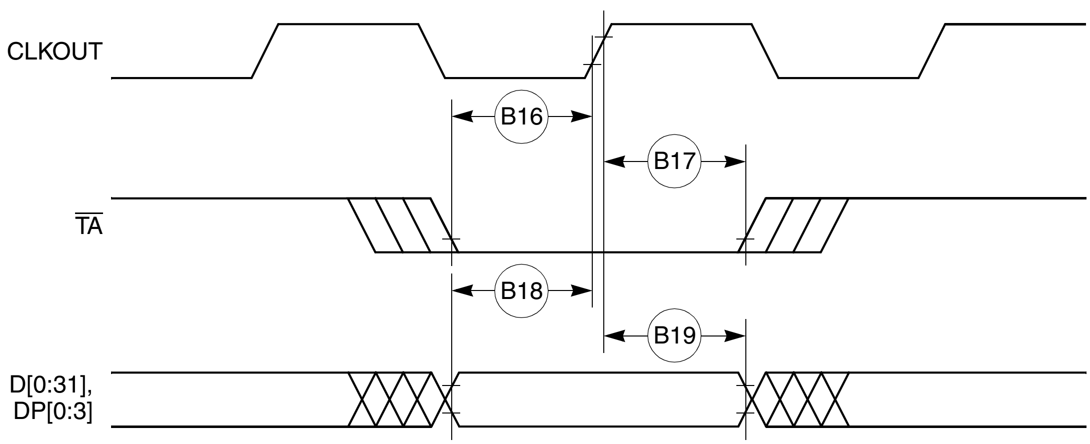



**Figure 8. Input Data Timing in Normal Case**

Figure 14 through Figure 16 provide the timing for the external bus write controlled by various GPCM factors.

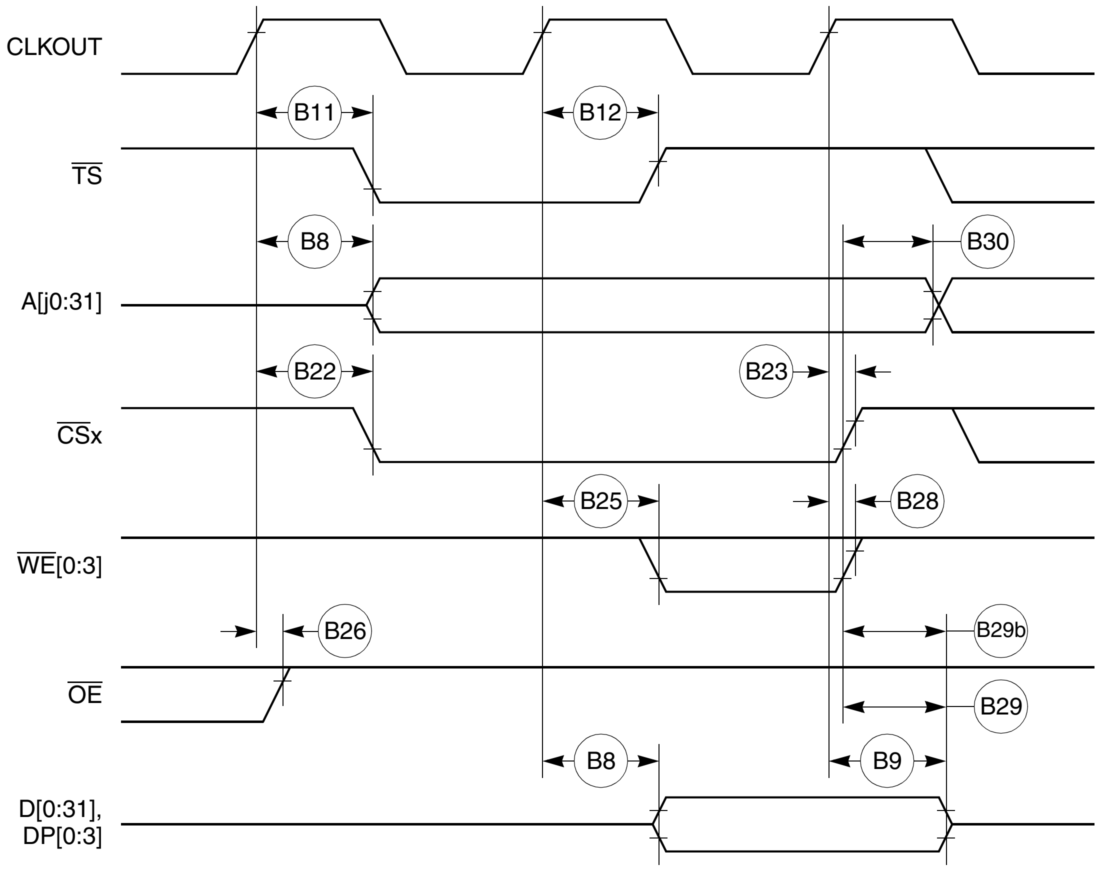



**Figure 14. External Bus Write Timing (GPCM Controlled—TRLX = 0 or 1, CSNT = 0)**

Figure 17 provides the timing for the external bus controlled by the UPM.

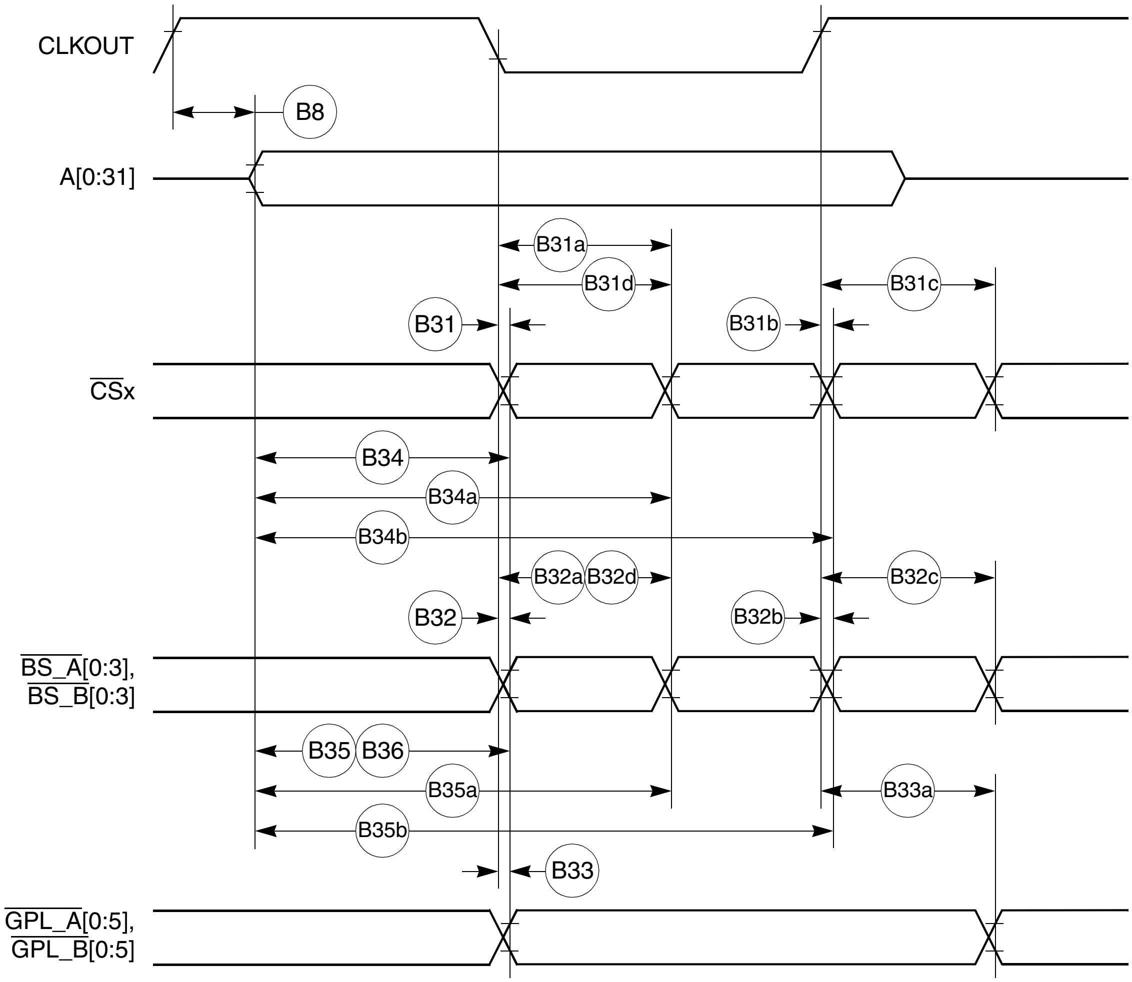



**Figure 17. External Bus Timing (UPM Controlled Signals)**

Figure 20 provides the timing for the synchronous external master access controlled by the GPCM.

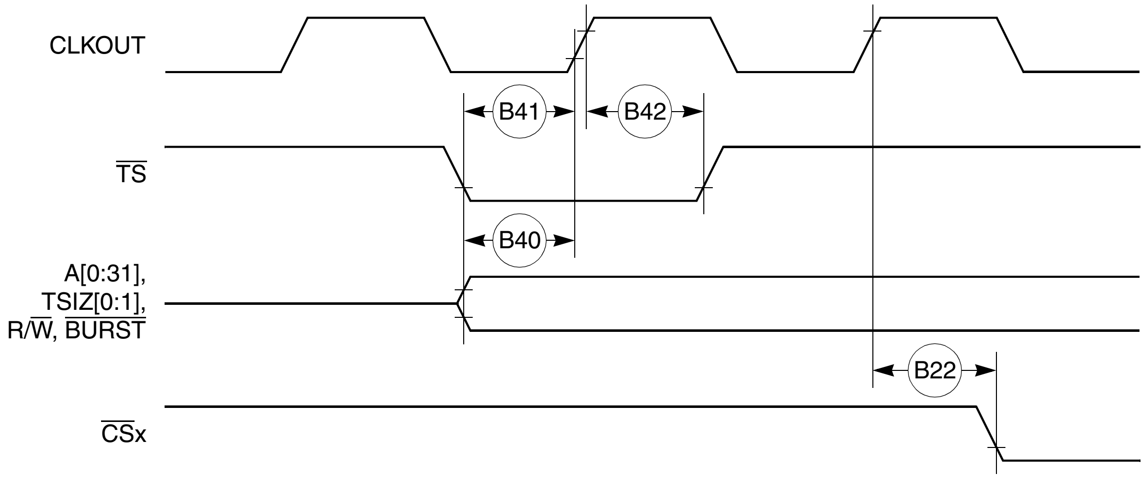



**Figure 20. Synchronous External Master Access Timing (GPCM Handled ACS = 00)**

Figure 21 provides the timing for the asynchronous external master memory access controlled by the GPCM.

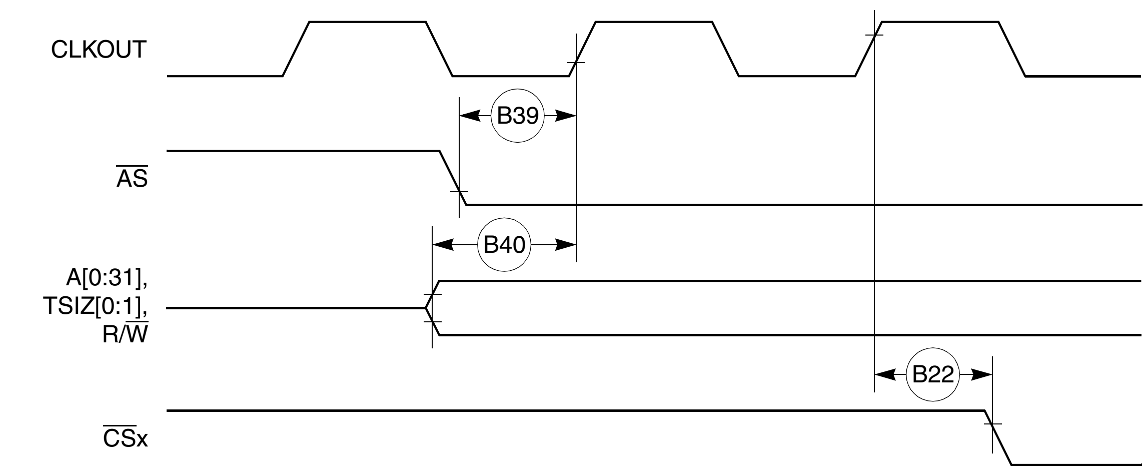



**Figure 21. Asynchronous External Master Memory Access Timing (GPCM Controlled—ACS = 00)**

Figure 22 provides the timing for the asynchronous external master control signals negation.

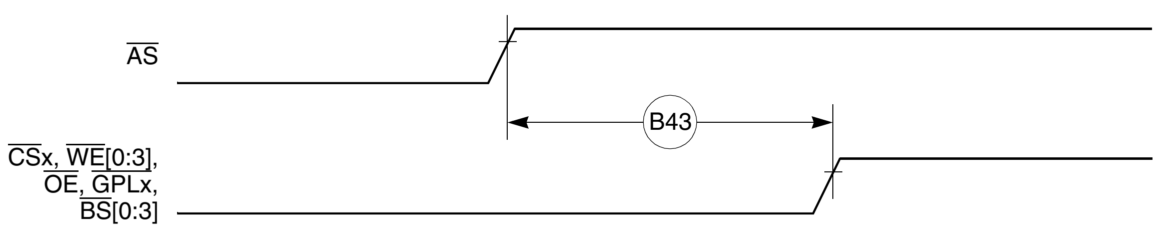



**Figure 22. Asynchronous External Master—Control Signals Negation Timing**

Figure 25 provides the PCMCIA access cycle timing for the external bus read.

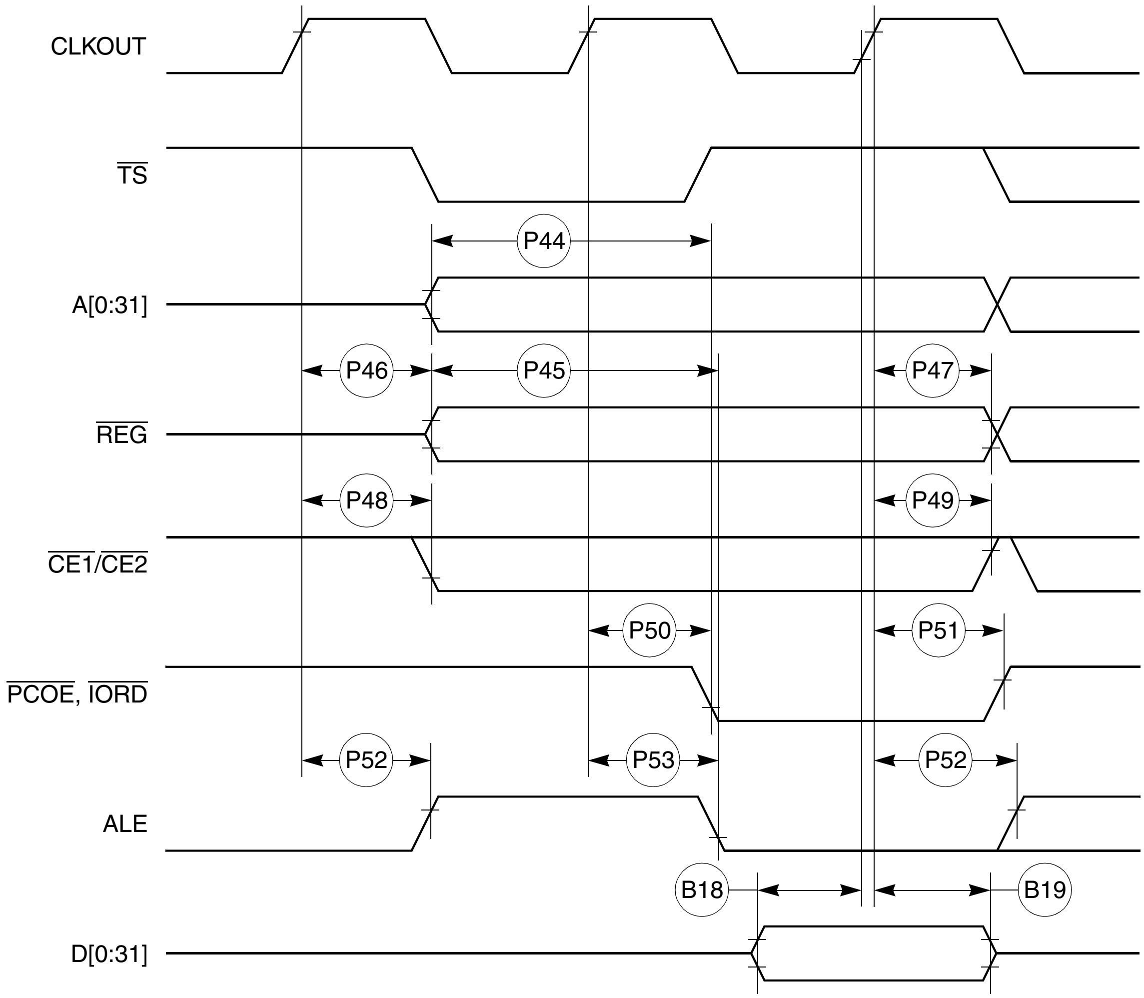



**Figure 25. PCMCIA Access Cycle Timing External Bus Read**

Figure 32 shows the reset timing for the data bus configuration.

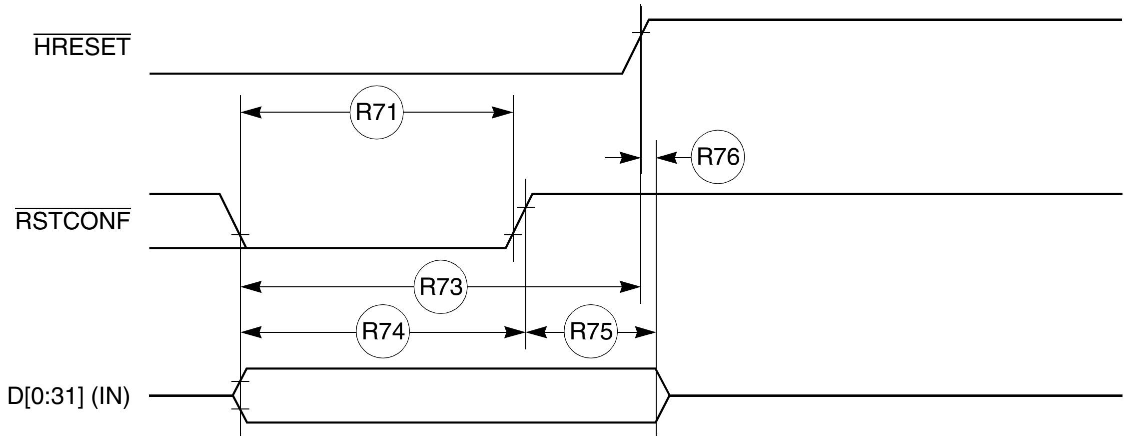



**Figure 32. Reset Timing—Configuration from Data Bus**

Figure 33 provides the reset timing for the data bus weak drive during configuration.

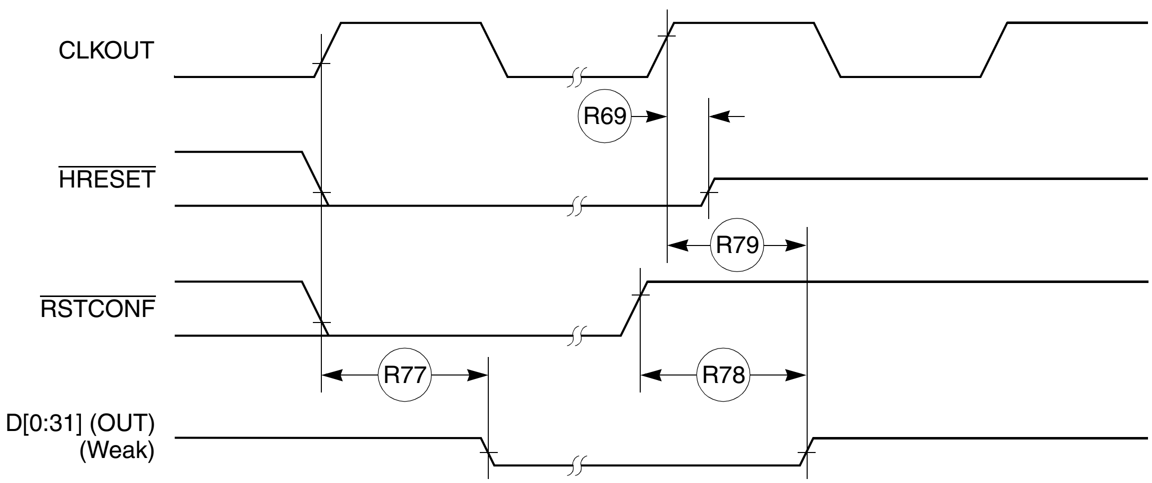



**Figure 33. Reset Timing—Data Bus Weak Drive During Configuration**

# 11 CPM Electrical Characteristics

This section provides the AC and DC electrical specifications for the communications processor module (CPM) of the MPC860.

## 11.1 PIP/PIO AC Electrical Specifications

Table 14 provides the PIP/PIO AC timings as shown in Figure 39 through Figure 43.

**Table 14. PIP/PIO Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 21 | Data-in setup time to STBI low | 0 | — | ns |
| 22 | Data-in hold time to STBI high | 2.5 – t3[1] | — | CLK |
| 23 | STBI pulse width | 1.5 | — | CLK |
| 24 | STBO pulse width | 1 CLK – 5 ns | — | ns |
| 25 | Data-out setup time to STBO low | 2 | — | CLK |
| 26 | Data-out hold time from STBO high | 5 | — | CLK |
| 27 | STBI low to STBO low (Rx interlock) | — | 2 | CLK |
| 28 | STBI low to STBO high (Tx interlock) | 2 | — | CLK |
| 29 | Data-in setup time to clock high | 15 | — | ns |
| 30 | Data-in hold time from clock high | 7.5 | — | ns |
| 31 | Clock low to data-out valid (CPU writes data, control, or direction) | — | 25 | ns |

[1] t3 = Specification 23.

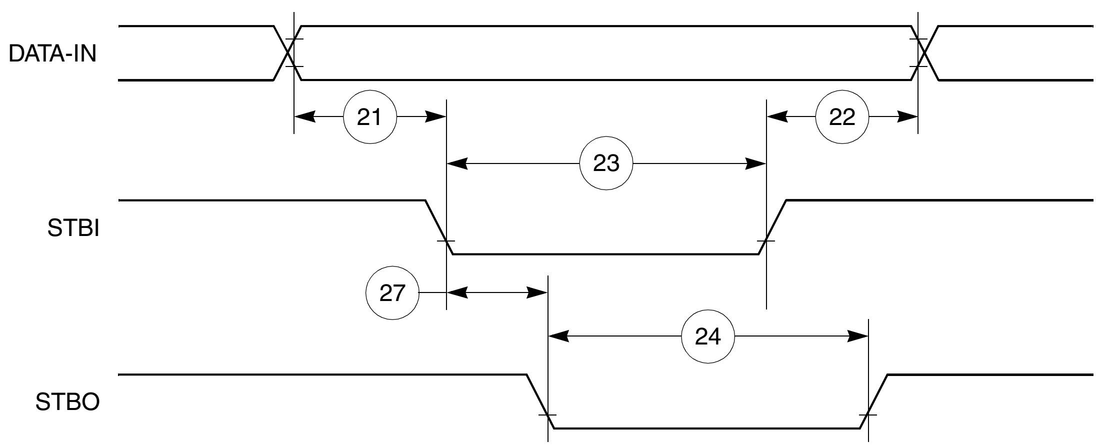



**Figure 39. PIP Rx (Interlock Mode) Timing Diagram**

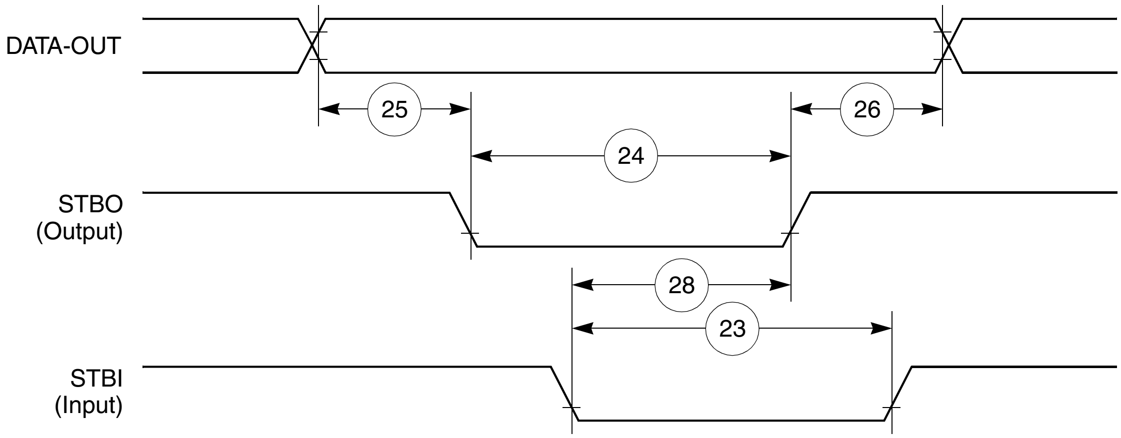



**Figure 40. PIP Tx (Interlock Mode) Timing Diagram**

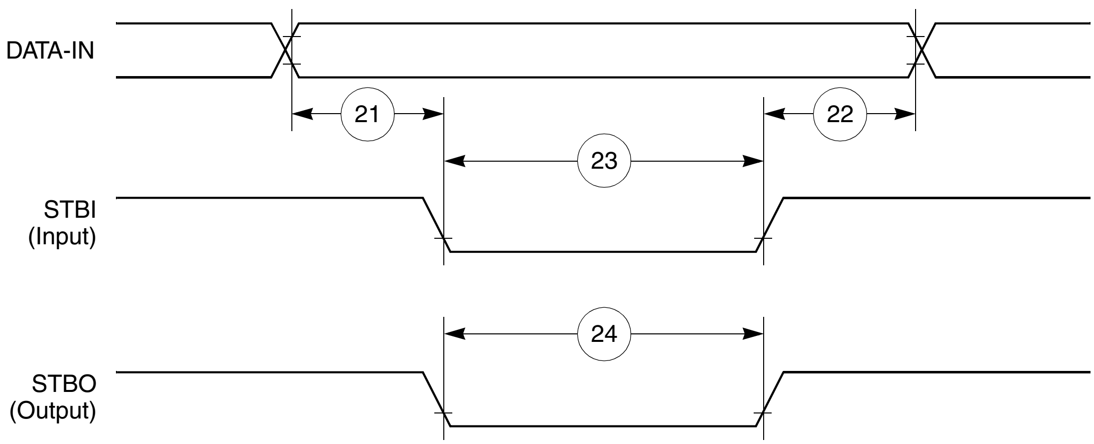



**Figure 41. PIP Rx (Pulse Mode) Timing Diagram**

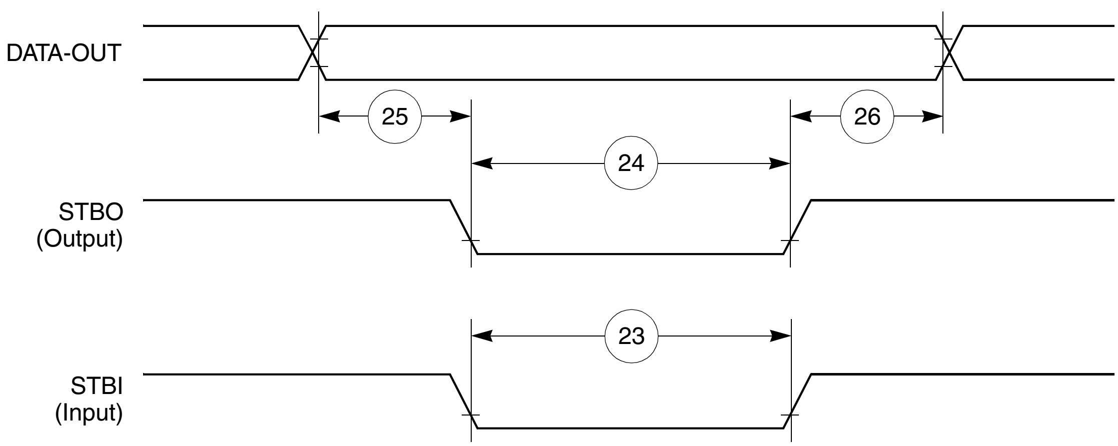



**Figure 42. PIP TX (Pulse Mode) Timing Diagram**

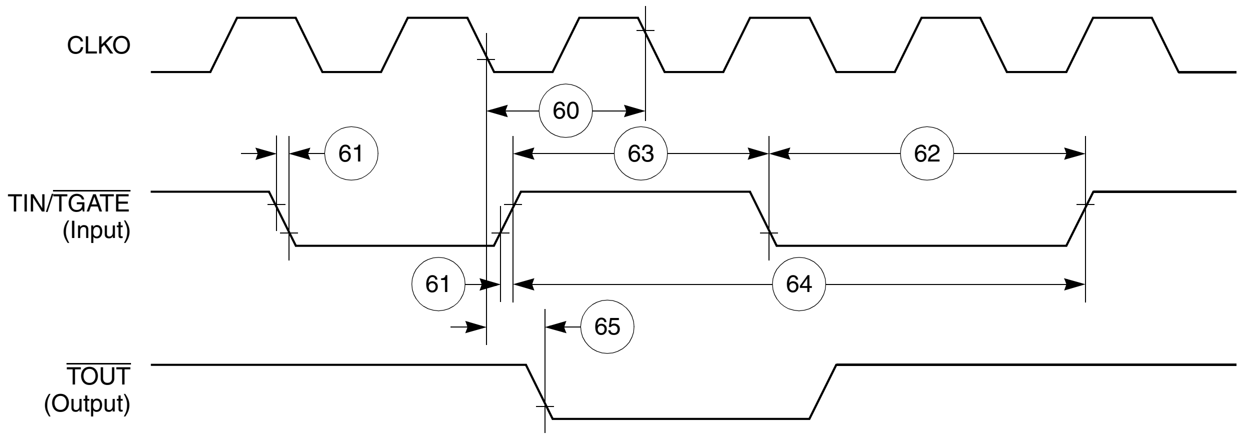



**Figure 50. CPM General-Purpose Timers Timing Diagram**

## 11.6 Serial Interface AC Electrical Specifications

Table 19 provides the serial interface timings as shown in Figure 51 through Figure 55.

**Table 19. SI Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 70 | L1RCLK, L1TCLK frequency (DSC = 0)[1, 2] | — | SYNCCLK/2.5 | MHz |
| 71 | L1RCLK, L1TCLK width low (DSC = 0)[2] | P + 10 | — | ns |
| 71a | L1RCLK, L1TCLK width high (DSC = 0)[3] | P + 10 | — | ns |
| 72 | L1TXD, L1ST(1–4), $\overline{\text{L1RQ}}$, L1CLKO rise/fall time | — | 15.00 | ns |
| 73 | L1RSYNC, L1TSYNC valid to L1CLK edge (SYNC setup time) | 20.00 | — | ns |
| 74 | L1CLK edge to L1RSYNC, L1TSYNC, invalid (SYNC hold time) | 35.00 | — | ns |
| 75 | L1RSYNC, L1TSYNC rise/fall time | — | 15.00 | ns |
| 76 | L1RXD valid to L1CLK edge (L1RXD setup time) | 17.00 | — | ns |
| 77 | L1CLK edge to L1RXD invalid (L1RXD hold time) | 13.00 | — | ns |
| 78 | L1CLK edge to L1ST(1–4) valid [4] | 10.00 | 45.00 | ns |
| 78A | L1SYNC valid to L1ST(1–4) valid | 10.00 | 45.00 | ns |
| 79 | L1CLK edge to L1ST(1–4) invalid | 10.00 | 45.00 | ns |
| 80 | L1CLK edge to L1TXD valid | 10.00 | 55.00 | ns |
| 80A | L1TSYNC valid to L1TXD valid [4] | 10.00 | 55.00 | ns |
| 81 | L1CLK edge to L1TXD high impedance | 0.00 | 42.00 | ns |
| 82 | L1RCLK, L1TCLK frequency (DSC =1 ) | — | 16.00 or SYNCCLK/2 | MHz |
| 83 | L1RCLK, L1TCLK width low (DSC = 1) | P + 10 | — | ns |
| 83a | L1RCLK, L1TCLK width high (DSC = 1)[3] | P + 10 | — | ns |

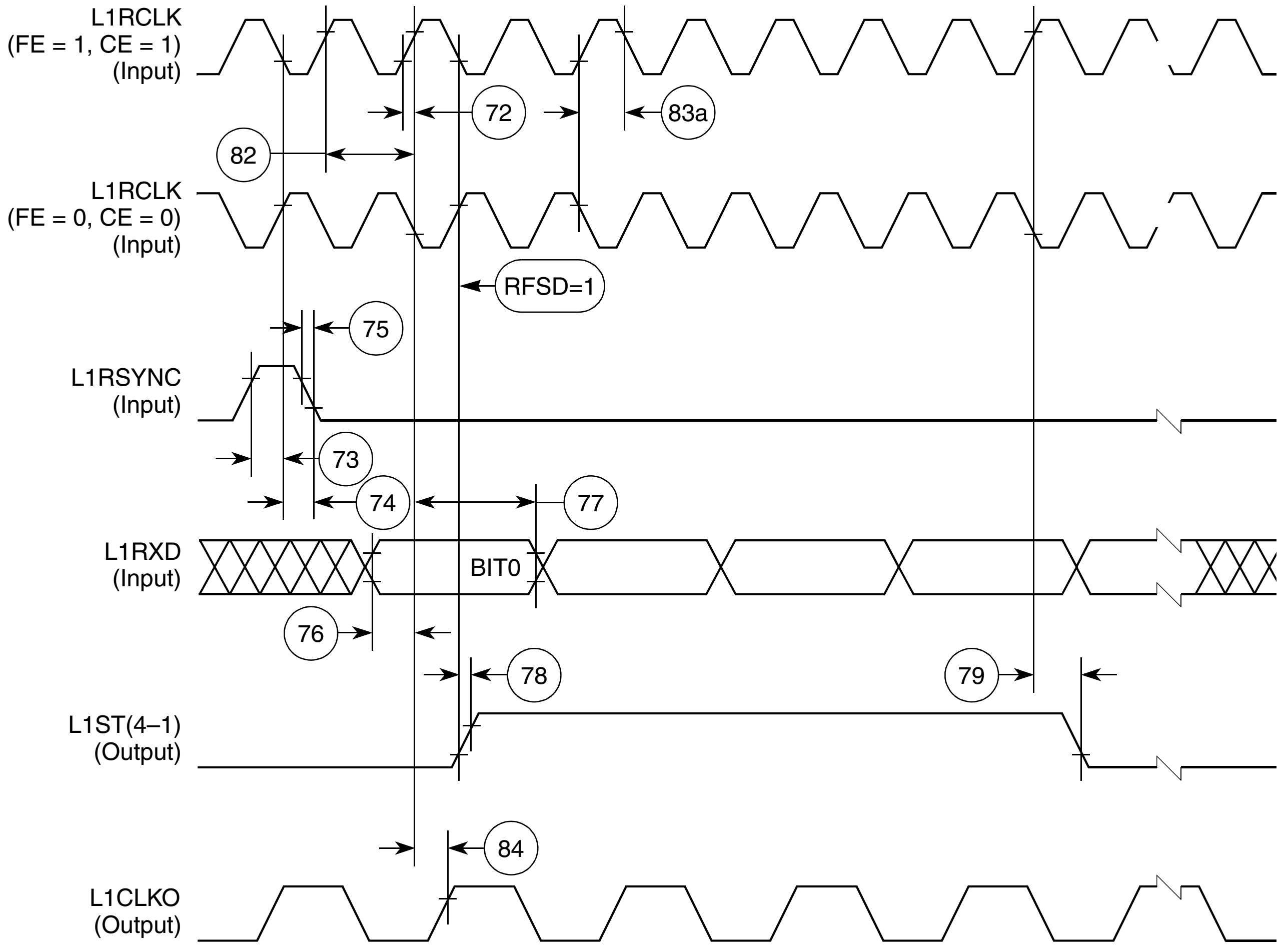



**Figure 52. SI Receive Timing with Double-Speed Clocking (DSC = 1)**

## 11.7 SCC in NMSI Mode Electrical Specifications

Table 20 provides the NMSI external clock timing.

**Table 20. NMSI External Clock Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 100 | RCLK1 and TCLK1 width high[1] | 1/SYNCCLK | — | ns |
| 101 | RCLK1 and TCLK1 width low | 1/SYNCCLK + 5 | — | ns |
| 102 | RCLK1 and TCLK1 rise/fall time | — | 15.00 | ns |
| 103 | TXD1 active delay (from TCLK1 falling edge) | 0.00 | 50.00 | ns |
| 104 | $\overline{\text{RTS1}}$ active/inactive delay (from TCLK1 falling edge) | 0.00 | 50.00 | ns |
| 105 | $\overline{\text{CTS1}}$ setup time to TCLK1 rising edge | 5.00 | — | ns |
| 106 | RXD1 setup time to RCLK1 rising edge | 5.00 | — | ns |
| 107 | RXD1 hold time from RCLK1 rising edge[2] | 5.00 | — | ns |
| 108 | $\overline{\text{CD1}}$ setup Time to RCLK1 rising edge | 5.00 | — | ns |

[1] The ratios SYNCCLK/RCLK1 and SYNCCLK/TCLK1 must be greater than or equal to 2.25/1.
[2] Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as external sync signals.

Table 21 provides the NMSI internal clock timing.

**Table 21. NMSI Internal Clock Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 100 | RCLK1 and TCLK1 frequency[1] | 0.00 | SYNCCLK/3 | MHz |
| 102 | RCLK1 and TCLK1 rise/fall time | — | — | ns |
| 103 | TXD1 active delay (from TCLK1 falling edge) | 0.00 | 30.00 | ns |
| 104 | $\overline{\text{RTS1}}$ active/inactive delay (from TCLK1 falling edge) | 0.00 | 30.00 | ns |
| 105 | $\overline{\text{CTS1}}$ setup time to TCLK1 rising edge | 40.00 | — | ns |
| 106 | RXD1 setup time to RCLK1 rising edge | 40.00 | — | ns |
| 107 | RXD1 hold time from RCLK1 rising edge[2] | 0.00 | — | ns |
| 108 | $\overline{\text{CD1}}$ setup time to RCLK1 rising edge | 40.00 | — | ns |

[1] The ratios SYNCCLK/RCLK1 and SYNCCLK/TCLK1 must be greater than or equal to 3/1.
[2] Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as external sync signals.

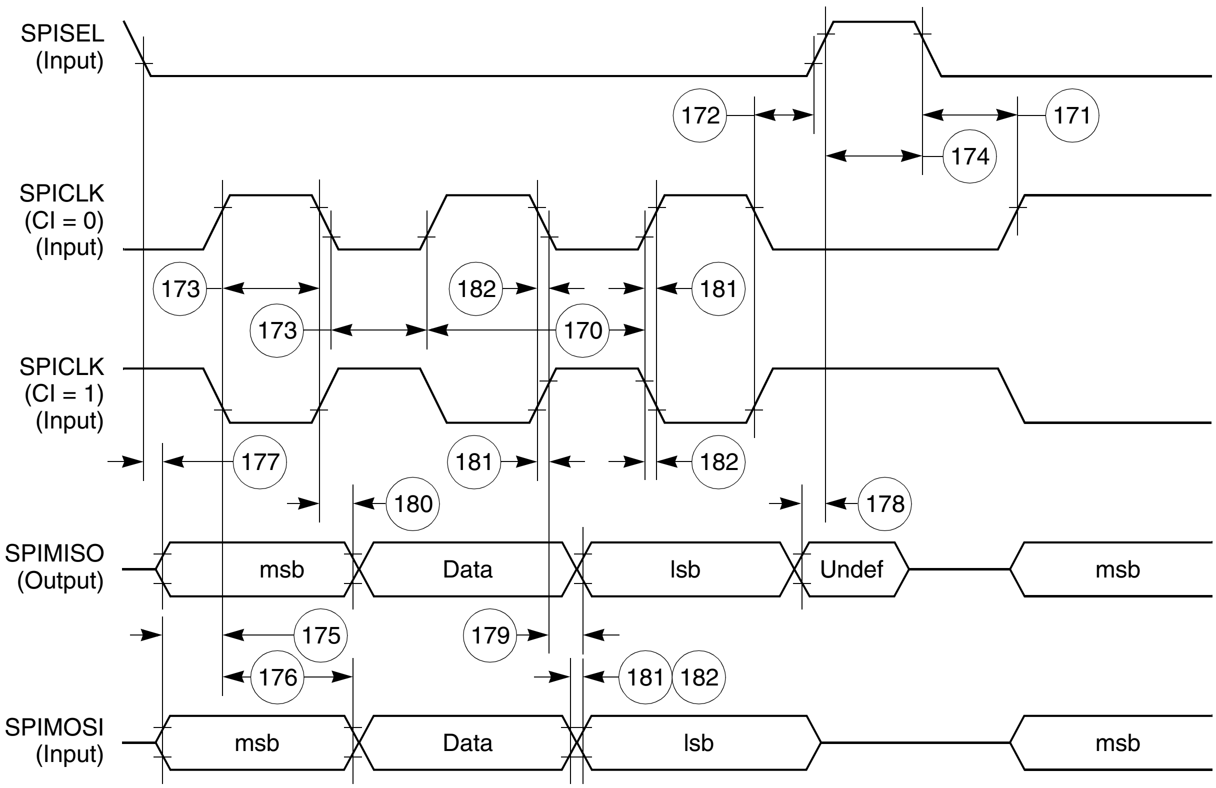



Figure 67. SPI Slave (CP = 0) Timing Diagram

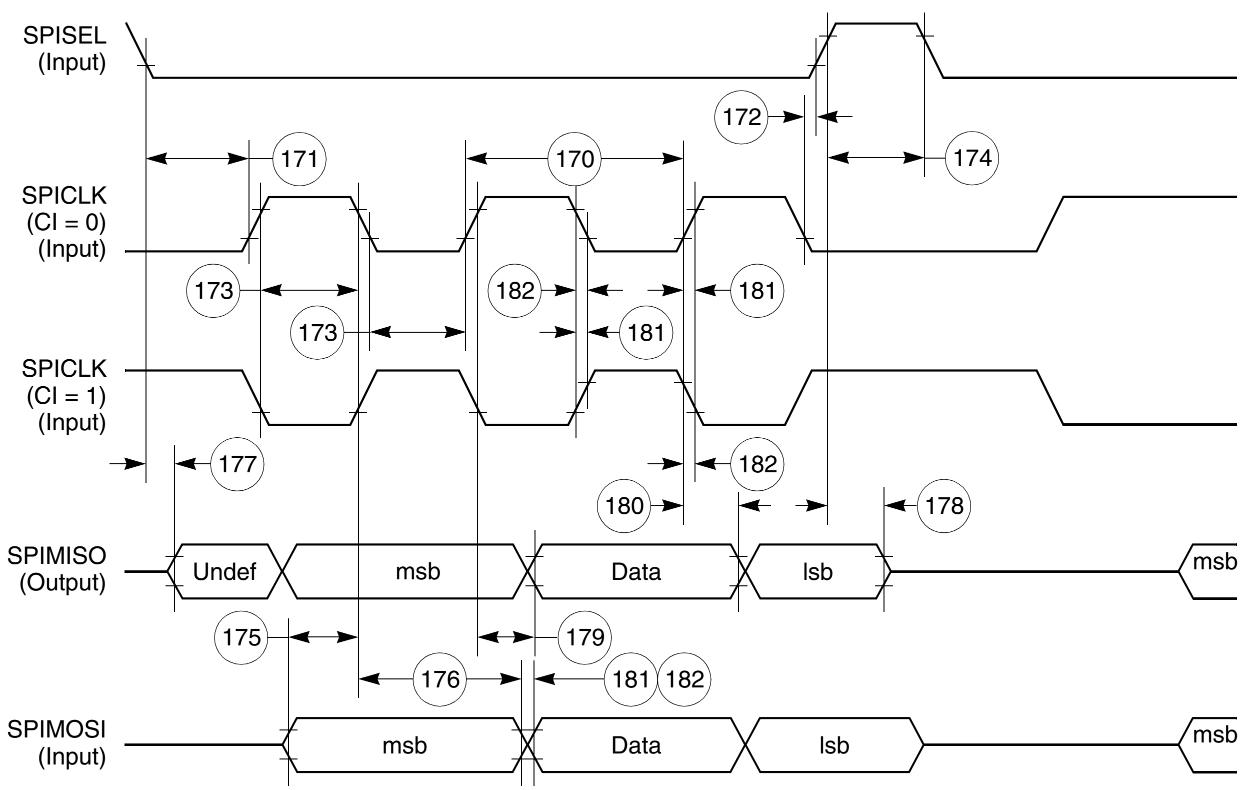



Figure 68. SPI Slave (CP = 1) Timing Diagram

## 11.12 I²C AC Electrical Specifications

Table 26 provides the I²C (SCL < 100 kHz) timings.

**Table 26. I²C Timing (SCL < 100 kHz)**

| Num | Characteristic | All Frequencies Min | All Frequencies Max | Unit |
|---|---|---|---|---|
| 200 | SCL clock frequency (slave) | 0 | 100 | kHz |
| 200 | SCL clock frequency (master)[1] | 1.5 | 100 | kHz |
| 202 | Bus free time between transmissions | 4.7 | — | μs |
| 203 | Low period of SCL | 4.7 | — | μs |
| 204 | High period of SCL | 4.0 | — | μs |
| 205 | Start condition setup time | 4.7 | — | μs |
| 206 | Start condition hold time | 4.0 | — | μs |
| 207 | Data hold time | 0 | — | μs |
| 208 | Data setup time | 250 | — | ns |
| 209 | SDL/SCL rise time | — | 1 | μs |
| 210 | SDL/SCL fall time | — | 300 | ns |
| 211 | Stop condition setup time | 4.7 | — | μs |

[1] SCL frequency is given by SCL = BRGCLK_frequency / ((BRG register + 3 × pre_scaler × 2). The ratio SYNCCLK/(BRGCLK/pre_scaler) must be greater than or equal to 4/1.

Table 27 provides the I²C (SCL > 100 kHz) timings.

**Table 27. . I²C Timing (SCL > 100 kHz)**

| Num | Characteristic | Expression | All Frequencies Min | All Frequencies Max | Unit |
|---|---|---|---|---|---|
| 200 | SCL clock frequency (slave) | fSCL | 0 | BRGCLK/48 | Hz |
| 200 | SCL clock frequency (master)[1] | fSCL | BRGCLK/16512 | BRGCLK/48 | Hz |
| 202 | Bus free time between transmissions | | 1/(2.2 * fSCL) | — | s |
| 203 | Low period of SCL | | 1/(2.2 * fSCL) | — | s |
| 204 | High period of SCL | | 1/(2.2 * fSCL) | — | s |
| 205 | Start condition setup time | | 1/(2.2 * fSCL) | — | s |
| 206 | Start condition hold time | | 1/(2.2 * fSCL) | — | s |
| 207 | Data hold time | | 0 | — | s |
| 208 | Data setup time | | 1/(40 * fSCL) | — | s |
| 209 | SDL/SCL rise time | | — | 1/(10 * fSCL) | s |
| 210 | SDL/SCL fall time | | — | 1/(33 * fSCL) | s |
| 211 | Stop condition setup time | | 1/2(2.2 * fSCL) | — | s |

[1] SCL frequency is given by SCL = BRGCLK_frequency / ((BRG register + 3) × pre_scaler × 2). The ratio SYNCCLK/(BRGCLK / pre_scaler) must be greater than or equal to 4/1.

Figure 70 shows signal timings during UTOPIA receive operations.

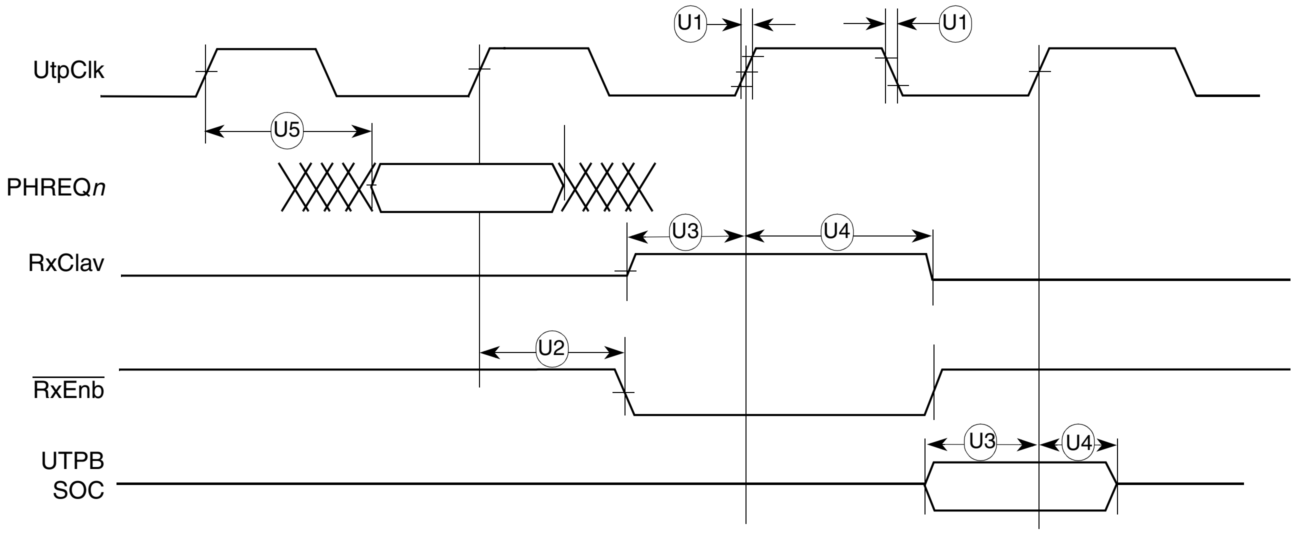



**Figure 70. UTOPIA Receive Timing**

Figure 71 shows signal timings during UTOPIA transmit operations.

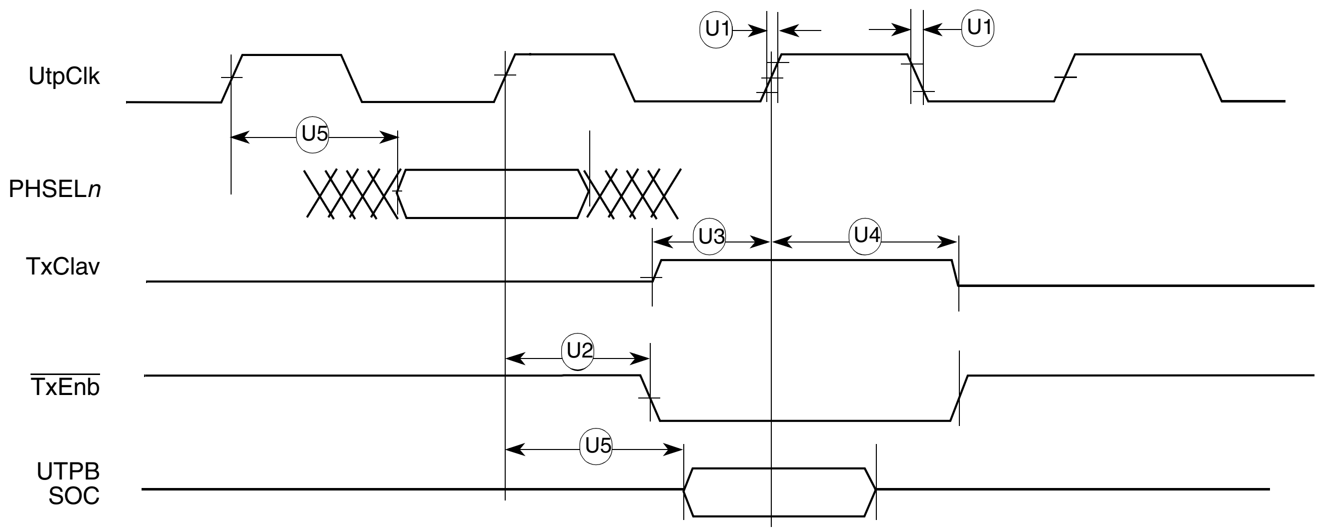
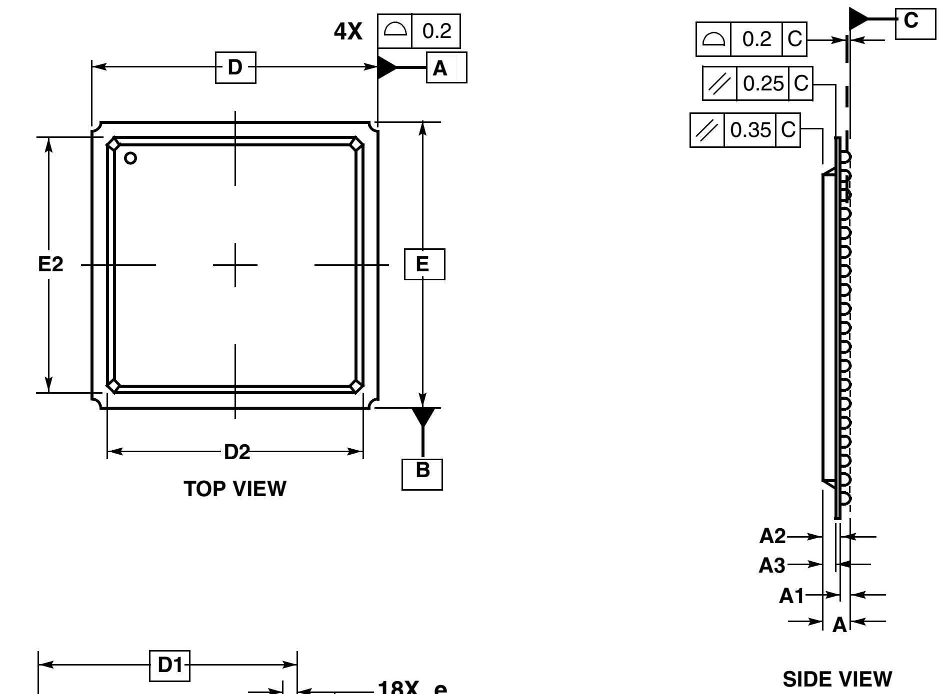
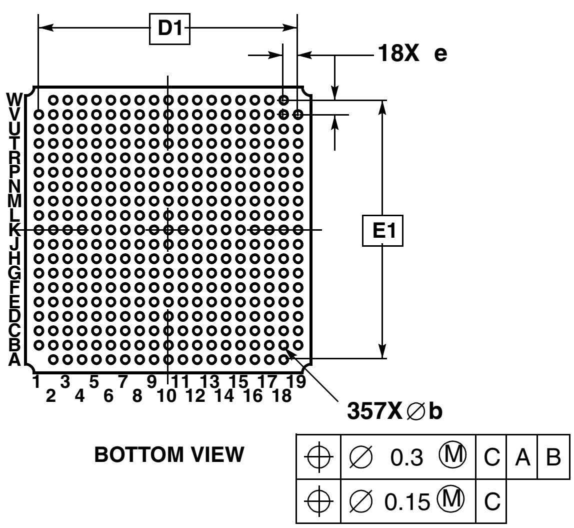



**Figure 71. UTOPIA Transmit Timing**

## 14.3 Mechanical Dimensions of the PBGA Package

Figure 77 shows the mechanical dimensions of the ZP PBGA package.




| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | --- | 2.05 |
| A1 | 0.50 | 0.70 |
| A2 | 0.95 | 1.35 |
| A3 | 0.70 | 0.90 |
| b | 0.60 | 0.90 |
| D | 25.00 BSC | |
| D1 | 22.86 BSC | |
| D2 | 22.40 | 22.60 |
| e | 1.27 BSC | |
| E | 25.00 BSC | |
| E1 | 22.86 BSC | |
| E2 | 22.40 | 22.60 |

**NOTE**

1. Dimensions and tolerance per ASME Y14.5M, 1994.
2. Dimensions in millimeters.
3. Dimension b is the maximum solder ball diameter measured parallel to data C.

**Figure 77. Mechanical Dimensions and Bottom Surface Nomenclature of the ZP PBGA Package**