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Understanding Embedded - Microprocessors

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Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Obsolete
MPC8xx
1 Core, 32-Bit
66MHz
Communications; CPM
DRAM
No
-
10Mbps (4), 10/100Mbps (1)
-
-
3.3V
0°C ~ 95°C (TA)
-
357-BBGA
357-PBGA (25x25)
https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc860pzq66d4r2

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- Up to 8 Kbytes of dual-port RAM
- 16 serial DMA (SDMA) channels
- Three parallel I/O registers with open-drain capability
- Four baud-rate generators (BRGs)
 - Independent (can be tied to any SCC or SMC)
 - Allows changes during operation
 - Autobaud support option
- Four serial communications controllers (SCCs)
 - Ethernet/IEEE 802.3[®] standard optional on SCC1–4, supporting full 10-Mbps operation (available only on specially programmed devices)
 - HDLC/SDLC (all channels supported at 2 Mbps)
 - HDLC bus (implements an HDLC-based local area network (LAN))
 - Asynchronous HDLC to support point-to-point protocol (PPP)
 - AppleTalk
 - Universal asynchronous receiver transmitter (UART)
 - Synchronous UART
 - Serial infrared (IrDA)
 - Binary synchronous communication (BISYNC)
 - Totally transparent (bit streams)
 - Totally transparent (frame-based with optional cyclic redundancy check (CRC))
- Two SMCs (serial management channels)
 - UART
 - Transparent
 - General circuit interface (GCI) controller
 - Can be connected to the time-division multiplexed (TDM) channels
- One SPI (serial peripheral interface)
 - Supports master and slave modes
 - Supports multimaster operation on the same bus
- One I²C (inter-integrated circuit) port
 - Supports master and slave modes
 - Multiple-master environment support
- Time-slot assigner (TSA)
 - Allows SCCs and SMCs to run in multiplexed and/or non-multiplexed operation
 - Supports T1, CEPT, PCM highway, ISDN basic rate, ISDN primary rate, user defined
 - 1- or 8-bit resolution
 - Allows independent transmit and receive routing, frame synchronization, and clocking



Thermal Characteristics

Figure 1 shows the undershoot and overshoot voltages at the interface of the MPC860.



1. t_{interface} refers to the clock period associated with the bus clock interface.

Figure 1. Undershoot/Overshoot Voltage for V_{DDH} and V_{DDL}

4 Thermal Characteristics

Table 3. Package Description

Package Designator	Package Code (Case No.)	Package Description
ZP	5050 (1103-01)	PBGA 357 25*25*0.9P1.27
ZQ/VR	5058 (1103D-02)	PBGA 357 25*25*1.2P1.27



Thermal Calculation and Measurement

7 Thermal Calculation and Measurement

For the following discussions, $P_D = (V_{DD} \times I_{DD}) + PI/O$, where PI/O is the power dissipation of the I/O drivers.

7.1 Estimation with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J, in °C can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

 T_A = ambient temperature (°C)

 $R_{\theta JA}$ = package junction-to-ambient thermal resistance (°C/W)

 P_D = power dissipation in package

The junction-to-ambient thermal resistance is an industry standard value which provides a quick and easy estimation of thermal performance. However, the answer is only an estimate; test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

7.2 Estimation with Junction-to-Case Thermal Resistance

Historically, the thermal resistance has frequently been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

 $R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

where:

 $R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

 $R_{\theta IC}$ = junction-to-case thermal resistance (°C/W)

 $R_{\theta CA}$ = case-to-ambient thermal resistance (°C/W)

 $R_{\theta JC}$ is device related and cannot be influenced by the user. The user adjusts the thermal environment to affect the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the airflow around the device, add a heat sink, change the mounting arrangement on the printed-circuit board, or change the thermal dissipation on the printed-circuit board surrounding the device. This thermal model is most useful for ceramic packages with heat sinks where some 90% of the heat flows through the case and the heat sink to the ambient environment. For most packages, a better model is required.

7.3 Estimation with Junction-to-Board Thermal Resistance

A simple package thermal model which has demonstrated reasonable accuracy (about 20%) is a two-resistor model consisting of a junction-to-board and a junction-to-case thermal resistance. The junction-to-case thermal resistance covers the situation where a heat sink is used or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed-circuit board. It has been observed that the thermal performance of most plastic packages, especially PBGA packages, is strongly dependent on the board temperature; see Figure 2.



Thermal Calculation and Measurement



Figure 2. Effect of Board Temperature Rise on Thermal Behavior

If the board temperature is known, an estimate of the junction temperature in the environment can be made using the following equation:

$$T_{J} = T_{B} + (R_{\theta JB} \times P_{D})$$

where:

 $R_{\theta JB}$ = junction-to-board thermal resistance (°C/W)

 $T_B = board temperature (°C)$

 P_D = power dissipation in package

If the board temperature is known and the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. For this method to work, the board and board mounting must be similar to the test board used to determine the junction-to-board thermal resistance, namely a 2s2p (board with a power and a ground plane) and by attaching the thermal balls to the ground plane.

7.4 Estimation Using Simulation

When the board temperature is not known, a thermal simulation of the application is needed. The simple two-resistor model can be used with the thermal simulation of the application [2], or a more accurate and complex model of the package can be used in the thermal simulation.

7.5 Experimental Determination

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$



	Characteristic	33	MHz	40 MHz		50 MHz		66 MHz		
Num	Characteristic	Min	Мах	Min	Мах	Min	Мах	Min	Max	Unit
B23	CLKOUT rising edge to \overline{CS} negated GPCM read access, GPCM write access ACS = 00, TRLX = 0, and CSNT = 0	2.00	8.00	2.00	8.00	2.00	8.00	2.00	8.00	ns
B24	A(0:31) and BADDR(28:30) to \overline{CS} asserted GPCM ACS = 10, TRLX = 0	5.58	—	4.25	_	3.00	_	1.79	—	ns
B24a	A(0:31) and BADDR(28:30) to \overline{CS} asserted GPCM ACS = 11, TRLX = 0	13.15	—	10.50	—	8.00	—	5.58	—	ns
B25	CLKOUT rising edge to \overline{OE} , \overline{WE} (0:3) asserted	—	9.00	—	9.00	—	9.00	—	9.00	ns
B26	CLKOUT rising edge to OE negated	2.00	9.00	2.00	9.00	2.00	9.00	2.00	9.00	ns
B27	A(0:31) and BADDR(28:30) to \overline{CS} asserted GPCM ACS = 10, TRLX = 1	35.88	_	29.25	_	23.00	_	16.94	_	ns
B27a	A(0:31) and BADDR(28:30) to \overline{CS} asserted GPCM ACS = 11, TRLX = 1	43.45	—	35.50	—	28.00	—	20.73	—	ns
B28	CLKOUT rising edge to $\overline{WE}(0:3)$ negated GPCM write access CSNT = 0	—	9.00	—	9.00	—	9.00	—	9.00	ns
B28a	CLKOUT falling edge to $\overline{WE}(0:3)$ negated GPCM write access TRLX = 0, 1, CSNT = 1, EBDF = 0	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.54	ns
B28b	CLKOUT falling edge to \overline{CS} negated GPCM write access TRLX = 0, 1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 0	—	14.33	—	13.00		11.75		10.54	ns
B28c	CLKOUT falling edge to \overline{WE} (0:3) negated GPCM write access TRLX = 0, 1, CSNT = 1 write access TRLX = 0, CSNT = 1, EBDF = 1	10.86	17.99	8.88	16.00	7.00	14.13	5.18	12.31	ns
B28d	CLKOUT falling edge to \overline{CS} negated GPCM write access TRLX = 0, 1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 1	_	17.99	_	16.00		14.13		12.31	ns
B29	$\overline{WE}(0:3)$ negated to D(0:31), DP(0:3) High-Z GPCM write access CSNT = 0, EBDF = 0	5.58	_	4.25	—	3.00	—	1.79	—	ns
B29a	$\overline{WE}(0:3)$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 0	13.15	—	10.5	—	8.00		5.58	—	ns
B29b	$\overline{\text{CS}}$ negated to D(0:31), DP(0:3), High-Z GPCM write access, ACS = 00, TRLX = 0, 1, and CSNT = 0	5.58		4.25		3.00		1.79		ns
B29c	$\overline{\text{CS}}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 0	13.15		10.5		8.00		5.58		ns

Table 7. Bus Operation Timings (continued)



	Characteristic	33	MHz	40 MHz		50 MHz		66 MHz		Unit
NUM		Min	Max	Min	Max	Min	Max	Min	Max	Unit
B35	A(0:31), BADDR(28:30) to \overline{CS} valid—as requested by control bit BST4 in the corresponding word in UPM	5.58	_	4.25	_	3.00	_	1.79	_	ns
B35a	A(0:31), BADDR(28:30), and D(0:31) to $\overline{\text{BS}}$ valid—as requested by control bit BST1 in the corresponding word in UPM	13.15	—	10.50	—	8.00	—	5.58	_	ns
B35b	A(0:31), BADDR(28:30), and D(0:31) to $\overline{\text{BS}}$ valid—as requested by control bit BST2 in the corresponding word in UPM	20.73	—	16.75	—	13.00	—	9.36		ns
B36	A(0:31), BADDR(28:30), and D(0:31) to GPL valid—as requested by control bit GxT4 in the corresponding word in UPM	5.58	—	4.25	—	3.00	—	1.79	_	ns
B37	UPWAIT valid to CLKOUT falling edge ⁹	6.00	—	6.00	—	6.00	—	6.00		ns
B38	CLKOUT falling edge to UPWAIT valid ⁹	1.00	—	1.00	_	1.00	_	1.00	_	ns
B39	AS valid to CLKOUT rising edge ¹⁰	7.00	_	7.00	_	7.00	_	7.00	_	ns
B40	A(0:31), TSIZ(0:1), RD/WR, BURST, valid to CLKOUT rising edge	7.00	—	7.00	—	7.00	—	7.00	_	ns
B41	$\overline{\text{TS}}$ valid to CLKOUT rising edge (setup time)	7.00	—	7.00	—	7.00	—	7.00	_	ns
B42	CLKOUT rising edge to \overline{TS} valid (hold time)	2.00	—	2.00	—	2.00	—	2.00	_	ns
B43	AS negation to memory controller signals negation	_	TBD	_	TBD	_	TBD	_	TBD	ns

¹ Phase and frequency jitter performance results are only valid if the input jitter is less than the prescribed value.

² If the rate of change of the frequency of EXTAL is slow (that is, it does not jump between the minimum and maximum values in one cycle) or the frequency of the jitter is fast (that is, it does not stay at an extreme value for a long time) then the maximum allowed jitter on EXTAL can be up to 2%.

³ The timings specified in B4 and B5 are based on full strength clock.

⁴ The timing for BR output is relevant when the MPC860 is selected to work with external bus arbiter. The timing for BG output is relevant when the MPC860 is selected to work with internal bus arbiter.

⁵ The timing required for BR input is relevant when the MPC860 is selected to work with internal bus arbiter. The timing for BG input is relevant when the MPC860 is selected to work with external bus arbiter.

⁶ The D(0:31) and DP(0:3) input timings B18 and B19 refer to the rising edge of the CLKOUT in which the TA input signal is asserted.

⁷ The D(0:31) and DP(0:3) input timings B20 and B21 refer to the falling edge of the CLKOUT. This timing is valid only for read accesses controlled by chip-selects under control of the UPM in the memory controller, for data beats where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

⁸ The timing B30 refers to \overline{CS} when ACS = 00 and to $\overline{WE}(0:3)$ when CSNT = 0.

⁹ The signal UPWAIT is considered asynchronous to the CLKOUT and synchronized internally. The timings specified in B37 and B38 are specified to enable the freeze of the UPM output signals as described in Figure 18.

¹⁰ The AS signal is considered asynchronous to the CLKOUT. The timing B39 is specified in order to allow the behavior specified in Figure 21.





Figure 15. External Bus Write Timing (GPCM Controlled—TRLX = 0 or 1, CSNT = 1)







Figure 16. External Bus Write Timing (GPCM Controlled—TRLX = 0 or 1, CSNT = 1)







Figure 17. External Bus Timing (UPM Controlled Signals)





Figure 20 provides the timing for the synchronous external master access controlled by the GPCM.

Figure 20. Synchronous External Master Access Timing (GPCM Handled ACS = 00)

Figure 21 provides the timing for the asynchronous external master memory access controlled by the GPCM.



Figure 22 provides the timing for the asynchronous external master control signals negation.

Figure 22. Asynchronous External Master—Control Signals Negation Timing

Table 9 shows the PCMCIA timing for the MPC860.

Table 9. PCMCIA Timing

Num	um Characteristic –		MHz	40 I	MHz	50 I	MHz	66 I	MHz	11
Num			Max	Min	Max	Min	Max	Min	Max	Unit
P44	A(0:31), REG valid to PCMCIA Strobe asserted ¹	20.73	—	16.75	—	13.00	—	9.36	—	ns
P45	A(0:31), $\overline{\text{REG}}$ valid to ALE negation ¹	28.30	—	23.00	—	18.00	—	13.15	_	ns
P46	CLKOUT to REG valid	7.58	15.58	6.25	14.25	5.00	13.00	3.79	11.84	ns
P47	CLKOUT to REG invalid	8.58	—	7.25	—	6.00	—	4.84	_	ns
P48	CLKOUT to $\overline{CE1}$, $\overline{CE2}$ asserted	7.58	15.58	6.25	14.25	5.00	13.00	3.79	11.84	ns
P49	CLKOUT to $\overline{CE1}$, $\overline{CE2}$ negated	7.58	15.58	6.25	14.25	5.00	13.00	3.79	11.84	ns
P50	CLKOUT to PCOE, IORD, PCWE, IOWR assert time	—	11.00		11.00	—	11.00	—	11.00	ns
P51	CLKOUT to PCOE, IORD, PCWE, IOWR negate time	2.00	11.00	2.00	11.00	2.00	11.00	2.00	11.00	ns
P52	CLKOUT to ALE assert time	7.58	15.58	6.25	14.25	5.00	13.00	3.79	10.04	ns
P53	CLKOUT to ALE negate time	—	15.58		14.25	_	13.00	—	11.84	ns
P54	PCWE, IOWR negated to D(0:31) invalid ¹	5.58	—	4.25	—	3.00	—	1.79	—	ns
P55	WAITA and WAITB valid to CLKOUT rising edge ¹	8.00	—	8.00	—	8.00	—	8.00	—	ns
P56	CLKOUT rising edge to WAITA and WAITB invalid ¹	2.00	—	2.00	—	2.00	—	2.00	—	ns

¹ PSST = 1. Otherwise add PSST times cycle time.

PSHT = 0. Otherwise add PSHT times cycle time.

These synchronous timings define when the WAITx signals are detected in order to freeze (or relieve) the PCMCIA current cycle. The WAITx assertion will be effective only if it is detected 2 cycles before the PSL timer expiration. See Chapter 16, "PCMCIA Interface," in the *MPC860 PowerQUICCTM Family User's Manual*.

Table 10 shows the PCMCIA port timing for the MPC860.

Table 10. PCMCIA Port Timing

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
Num		Min	Max	Min	Max	Min	Max	Min	Max	Unit
P57	CLKOUT to OPx valid	—	19.00	_	19.00	_	19.00	_	19.00	ns
P58	HRESET negated to OPx drive ¹	25.73	—	21.75	—	18.00	—	14.36	—	ns
P59	IP_Xx valid to CLKOUT rising edge	5.00	—	5.00	—	5.00	—	5.00	—	ns
P60	CLKOUT rising edge to IP_Xx invalid	1.00	—	1.00	—	1.00	—	1.00	—	ns

¹ OP2 and OP3 only.

Figure 28 provides the PCMCIA output port timing for the MPC860.

Figure 28. PCMCIA Output Port Timing

Figure 29 provides the PCMCIA output port timing for the MPC860.

Figure 29. PCMCIA Input Port Timing

Table 12 shows the reset timing for the MPC860.

Table 12. Reset Timing

Num	m Characteristic		/IHz	40 N	ΛHz	50 N	ЛНz	66 N	ΛHz	llmit
Num			Max	Min	Max	Min	Max	Min	Max	Unit
R69	CLKOUT to HRESET high impedance	—	20.00	—	20.00	—	20.00	—	20.00	ns
R70	CLKOUT to SRESET high impedance	—	20.00	—	20.00	—	20.00	—	20.00	ns
R71	RSTCONF pulse width	515.15	—	425.00		340.00	—	257.58	—	ns
R72	_	_	—	—	—	—	—	—	—	
R73	Configuration data to HRESET rising edge setup time	504.55	—	425.00	—	350.00	—	277.27	—	ns
R74	Configuration data to RSTCONF rising edge setup time	350.00	_	350.00	_	350.00	_	350.00	_	ns
R75	Configuration data hold time after RSTCONF negation	0.00	—	0.00	—	0.00	—	0.00	—	ns
R76	Configuration data hold time after HRESET negation	0.00	—	0.00	—	0.00	—	0.00	—	ns
R77	HRESET and RSTCONF asserted to data out drive	_	25.00		25.00	_	25.00	_	25.00	ns
R78	RSTCONF negated to data out high impedance	-	25.00	—	25.00	—	25.00	—	25.00	ns
R79	CLKOUT of last rising edge before chip three-state HRESET to data out high impedance	_	25.00	—	25.00	—	25.00	—	25.00	ns
R80	DSDI, DSCK setup	90.91	—	75.00	—	60.00	—	45.45	—	ns
R81	DSDI, DSCK hold time	0.00	—	0.00	—	0.00	—	0.00	—	ns
R82	SRESET negated to CLKOUT rising edge for DSDI and DSCK sample	242.42		200.00		160.00		121.21		ns

CPM Electrical Characteristics

Figure 47. SDACK Timing Diagram—Peripheral Write, Internally-Generated TA

Figure 48. SDACK Timing Diagram—Peripheral Read, Internally-Generated TA

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SCC in NMSI Mode Electrical Specifications 11.7

Table 20 provides the NMSI external clock timing.

Table 2	20. NMSI	External	Clock	Timing
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Num	Characteristic	All Freq	Unit	
Nulli	Characteristic	Min	Мах	Unit
100	RCLK1 and TCLK1 width high ¹	1/SYNCCLK	_	ns
101	RCLK1 and TCLK1 width low	1/SYNCCLK + 5		ns
102	RCLK1 and TCLK1 rise/fall time	—	15.00	ns
103	TXD1 active delay (from TCLK1 falling edge)	0.00	50.00	ns
104	RTS1 active/inactive delay (from TCLK1 falling edge)	0.00	50.00	ns
105	CTS1 setup time to TCLK1 rising edge	5.00	—	ns
106	RXD1 setup time to RCLK1 rising edge	5.00	_	ns
107	RXD1 hold time from RCLK1 rising edge ²	5.00	—	ns
108	CD1 setup Time to RCLK1 rising edge	5.00	_	ns

¹ The ratios SYNCCLK/RCLK1 and SYNCCLK/TCLK1 must be greater than or equal to 2.25/1.
 ² Also applies to CD and CTS hold time when they are used as external sync signals.

Table 21 provides the NMSI internal clock timing.

Table 21. NMSI Internal Clock Timing

Num	Characteristic	All Freq	Unit	
Num	Characteristic	Min	Мах	Unit
100	RCLK1 and TCLK1 frequency ¹	0.00	SYNCCLK/3	MHz
102	RCLK1 and TCLK1 rise/fall time	—	—	ns
103	TXD1 active delay (from TCLK1 falling edge)	0.00	30.00	ns
104	RTS1 active/inactive delay (from TCLK1 falling edge)	0.00	30.00	ns
105	CTS1 setup time to TCLK1 rising edge	40.00	—	ns
106	RXD1 setup time to RCLK1 rising edge	40.00	—	ns
107	RXD1 hold time from RCLK1 rising edge ²	0.00	_	ns
108	CD1 setup time to RCLK1 rising edge	40.00	_	ns

¹ The ratios SYNCCLK/RCLK1 and SYNCCLK/TCLK1 must be greater than or equal to 3/1.

² Also applies to \overline{CD} and \overline{CTS} hold time when they are used as external sync signals.

Figure 58. HDLC Bus Timing Diagram

11.8 Ethernet Electrical Specifications

Table 22 provides the Ethernet timings as shown in Figure 59 through Figure 63.

Num	Characteristic	All Freq		
		Min	Мах	Unit
120	CLSN width high	40		ns
121	RCLK1 rise/fall time	—	15	ns
122	RCLK1 width low	40	—	ns
123	RCLK1 clock period ¹	80	120	ns
124	RXD1 setup time	20	—	ns
125	RXD1 hold time	5	—	ns
126	RENA active delay (from RCLK1 rising edge of the last data bit)	10	—	ns
127	RENA width low	100	—	ns
128	TCLK1 rise/fall time	—	15	ns
129	TCLK1 width low	40	—	ns
130	TCLK1 clock period ¹	99	101	ns
131	TXD1 active delay (from TCLK1 rising edge)	10	50	ns
132	TXD1 inactive delay (from TCLK1 rising edge)	10	50	ns
133	TENA active delay (from TCLK1 rising edge)	10	50	ns
134	TENA inactive delay (from TCLK1 rising edge)	10	50	ns

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CPM Electrical Characteristics

SMC Transparent AC Electrical Specifications 11.9

Table 23 provides the SMC transparent timings as shown in Figure 64.

Table 23. SMC Transparent Timing

Num	Characteristic	All Freq	11	
		Min	Мах	Unit
150	SMCLK clock period ¹	100	—	ns
151	SMCLK width low	50	—	ns
151A	SMCLK width high	50	—	ns
152	SMCLK rise/fall time	—	15	ns
153	SMTXD active delay (from SMCLK falling edge)	10	50	ns
154	SMRXD/SMSYNC setup time	20	—	ns
155	RXD1/SMSYNC hold time	5	_	ns

¹ SYNCCLK must be at least twice as fast as SMCLK.

Note: 1. This delay is equal to an integer number of character-length clocks.

13 FEC Electrical Characteristics

This section provides the AC electrical specifications for the Fast Ethernet controller (FEC). Note that the timing specifications for the MII signals are independent of system clock frequency (part speed designation). Also, MII signals use TTL signal levels compatible with devices operating at either 5.0 V or 3.3 V.

13.1 MII Receive Signal Timing (MII_RXD[3:0], MII_RX_DV, MII_RX_ER, MII_RX_CLK)

The receiver functions correctly up to a MII_RX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed the MII_RX_CLK frequency - 1%.

Table 29 provides information on the MII receive signal timing.

Num	Characteristic	Min	Max	Unit
M1	MII_RXD[3:0], MII_RX_DV, MII_RX_ER to MII_RX_CLK setup	5		ns
M2	MII_RX_CLK to MII_RXD[3:0], MII_RX_DV, MII_RX_ER hold	5		ns
M3	MII_RX_CLK pulse width high	35%	65%	MII_RX_CLK period
M4	MII_RX_CLK pulse width low	35%	65%	MII_RX_CLK period

Table 29. Mll Receive Signal Timing

Figure 72 shows MII receive signal timing.

Figure 72. MII Receive Signal Timing Diagram

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FEC Electrical Characteristics

13.3 MII Async Inputs Signal Timing (MII_CRS, MII_COL)

Table 31 provides information on the MII async inputs signal timing.

Table 31. MII Async Inputs Signal Timing

Num	Characteristic	Min	Мах	Unit
M9	MII_CRS, MII_COL minimum pulse width	1.5		MII_TX_CLK period

Figure 74 shows the MII asynchronous inputs signal timing diagram.

13.4 MII Serial Management Channel Timing (MII_MDIO, MII_MDC)

Table 32 provides information on the MII serial management channel signal timing. The FEC functions correctly with a maximum MDC frequency in excess of 2.5 MHz. The exact upper bound is under investigation.

Num	Characteristic	Min	Мах	Unit
M10	MII_MDC falling edge to MII_MDIO output invalid (minimum propagation delay)	0	_	ns
M11	MII_MDC falling edge to MII_MDIO output valid (max prop delay)	_	25	ns
M12	MII_MDIO (input) to MII_MDC rising edge setup	10	—	ns
M13	MII_MDIO (input) to MII_MDC rising edge hold	0	—	ns
M14	MII_MDC pulse width high	40%	60%	MII_MDC period
M15	MII_MDC pulse width low	40%	60%	MII_MDC period

Table 32. MII Serial Management Channel Timing

Mechanical Data and Ordering Information

14.3 Mechanical Dimensions of the PBGA Package

Figure 77 shows the mechanical dimensions of the ZP PBGA package.

- 1. Dimensions and tolerance per ASME Y14.5M, 1994.
- 2. Dimensions in millimeters.
- 3. Dimension b is the maximum solder ball diameter measured parallel to data C.

22.40

E2

22.60