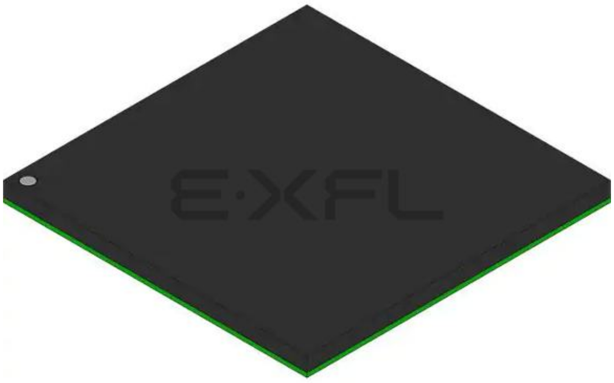
Freescale Semiconductor - MPC860SRVR50D4R2 Datasheet



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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	50MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (4)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 95°C (TA)
Security Features	-
Package / Case	357-BBGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc860srvr50d4r2

2 Features

The following list summarizes the key MPC860 features:

- Embedded single-issue, 32-bit core (implementing the Power Architecture technology) with thirty-two 32-bit general-purpose registers (GPRs)
  - The core performs branch prediction with conditional prefetch without conditional execution.
  - 4- or 8-Kbyte data cache and 4- or 16-Kbyte instruction cache (see Table 1)
    - 16-Kbyte instruction caches are four-way, set-associative with 256 sets; 4-Kbyte instruction caches are two-way, set-associative with 128 sets.
    - 8-Kbyte data caches are two-way, set-associative with 256 sets; 4-Kbyte data caches are two-way, set-associative with 128 sets.
    - Cache coherency for both instruction and data caches is maintained on 128-bit (4-word) cache blocks.
    - Caches are physically addressed, implement a least recently used (LRU) replacement algorithm, and are lockable on a cache block basis.
  - MMUs with 32-entry TLB, fully-associative instruction, and data TLBs
  - MMUs support multiple page sizes of 4-, 16-, and 512-Kbytes, and 8-Mbytes; 16 virtual address spaces and 16 protection groups
  - Advanced on-chip-emulation debug mode
- Up to 32-bit data bus (dynamic bus sizing for 8, 16, and 32 bits)
- 32 address lines
- Operates at up to 80 MHz
- Memory controller (eight banks)
  - Contains complete dynamic RAM (DRAM) controller
  - Each bank can be a chip select or $\overline{\text{RAS}}$ to support a DRAM bank.
  - Up to 15 wait states programmable per memory bank
  - Glueless interface to DRAM, SIMMS, SRAM, EPROM, Flash EPROM, and other memory devices
  - DRAM controller programmable to support most size and speed memory interfaces
  - Four $\overline{\text{CAS}}$ lines, four $\overline{\text{WE}}$ lines, and one $\overline{\text{OE}}$ line
  - Boot chip-select available at reset (options for 8-, 16-, or 32-bit memory)
  - Variable block sizes (32 Kbytes to 256 Mbytes)
  - Selectable write protection
  - On-chip bus arbitration logic
- General-purpose timers
  - Four 16-bit timers or two 32-bit timers
  - Gate mode can enable/disable counting
  - Interrupt can be masked on reference match and event capture.

- System integration unit (SIU)
    - Bus monitor
    - Software watchdog
    - Periodic interrupt timer (PIT)
    - Low-power stop mode
    - Clock synthesizer
    - Decrementer, time base, and real-time clock (RTC)
    - Reset controller
    - IEEE 1149.1™ Std. test access port (JTAG)
- Interrupts
    - Seven external interrupt request (IRQ) lines
    - 12 port pins with interrupt capability
    - 23 internal interrupt sources
    - Programmable priority between SCCs
    - Programmable highest priority request
- 10/100 Mbps Ethernet support, fully compliant with the IEEE 802.3u® Standard (not available when using ATM over UTOPIA interface)
- ATM support compliant with ATM forum UNI 4.0 specification
    - Cell processing up to 50–70 Mbps at 50-MHz system clock
    - Cell multiplexing/demultiplexing
    - Support of AAL5 and AAL0 protocols on a per-VC basis. AAL0 support enables OAM and software implementation of other protocols.
    - ATM pace control (APC) scheduler, providing direct support for constant bit rate (CBR) and unspecified bit rate (UBR) and providing control mechanisms enabling software support of available bit rate (ABR)
    - Physical interface support for UTOPIA (10/100-Mbps is not supported with this interface) and byte-aligned serial (for example, T1/E1/ADSL)
    - UTOPIA-mode ATM supports level-1 master with cell-level handshake, multi-PHY (up to four physical layer devices), connection to 25-, 51-, or 155-Mbps framers, and UTOPIA/system clock ratios of 1/2 or 1/3.
    - Serial-mode ATM connection supports transmission convergence (TC) function for T1/E1/ADSL lines, cell delineation, cell payload scrambling/descrambling, automatic idle/unassigned cell insertion/stripping, header error control (HEC) generation, checking, and statistics.
- Communications processor module (CPM)
    - RISC communications processor (CP)
    - Communication-specific commands (for example, GRACEFUL STOP TRANSMIT, ENTER HUNT MODE, and RESTART TRANSMIT)
    - Supports continuous mode transmission and reception on all serial channels

  - Allows dynamic changes
  - Can be internally connected to six serial channels (four SCCs and two SMCs)
- Parallel interface port (PIP)
  - Centronics interface support
  - Supports fast connection between compatible ports on the MPC860 or the MC68360
- PCMCIA interface
  - Master (socket) interface, release 2.1 compliant
  - Supports two independent PCMCIA sockets
  - Supports eight memory or I/O windows
- Low power support
  - Full on—all units fully powered
  - Doze—core functional units disabled except time base decrementer, PLL, memory controller, RTC, and CPM in low-power standby
  - Sleep—all units disabled except RTC and PIT, PLL active for fast wake up
  - Deep sleep—all units disabled including PLL except RTC and PIT
  - Power down mode—all units powered down except PLL, RTC, PIT, time base, and decrementer
- Debug interface
  - Eight comparators: four operate on instruction address, two operate on data address, and two operate on data
  - Supports conditions: $= \neq < >$
  - Each watchpoint can generate a break-point internally.
- 3.3-V operation with 5-V TTL compatibility except EXTAL and EXTCLK
- 357-pin ball grid array (BGA) package

3 Maximum Tolerated Ratings

This section provides the maximum tolerated voltage and temperature ranges for the MPC860. Table 2 provides the maximum ratings.

This device contains circuitry protecting against damage due to high-static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or V_{DD}).

Table 2. Maximum Tolerated Ratings

(GND = 0 V)

Rating	Symbol	Value	Unit
Supply voltage[1]	V_{DDH}	–0.3 to 4.0	V
	V_{DDL}	–0.3 to 4.0	V
	KAPWR	–0.3 to 4.0	V
	V_{DDSYN}	–0.3 to 4.0	V
Input voltage[2]	V_{in}	GND – 0.3 to V_{DDH}	V
Temperature[3] (standard)	$T_{A(min)}$	0	°C
	$T_{j(max)}$	95	°C
Temperature[3] (extended)	$T_{A(min)}$	–40	°C
	$T_{j(max)}$	95	°C
Storage temperature range	T_{stg}	–55 to 150	°C

[1] The power supply of the device must start its ramp from 0.0 V.

[2] Functional operating conditions are provided with the DC electrical specifications in Table 6. Absolute maximum ratings are stress ratings only; functional operation at the maxima is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device.
Caution: All inputs that tolerate 5 V cannot be more than 2.5 V greater than the supply voltage. This restriction applies to power-up and normal operation (that is, if the MPC860 is unpowered, voltage greater than 2.5 V must not be applied to its inputs).

[3] Minimum temperatures are guaranteed as ambient temperature, T_A. Maximum temperatures are guaranteed as junction temperature, T_j.

Table 6. DC Electrical Specifications (continued)

Characteristic	Symbol	Min	Max	Unit
Input leakage current, V_{in} = 3.6 V (except TMS, TRST, DSCK, and DSDI pins)	I_{In}	—	10	µA
Input leakage current, V_{in} = 0 V (except TMS, TRST, DSCK, and DSDI pins)	I_{In}	—	10	µA
Input capacitance[2]	C_{in}	—	20	pF
Output high voltage, I_{OH} = –2.0 mA, V_{DDH} = 3.0 V (except XTAL, XFC, and open-drain pins)	V_{OH}	2.4	—	V
Output low voltage I_{OL} = 2.0 mA, CLKOUT I_{OL} = 3.2 mA [3] I_{OL} = 5.3 mA [4] I_{OL} = 7.0 mA, TXD1/PA14, TXD2/PA12 I_{OL} = 8.9 mA, TS, TA, TEA, BI, BB, HRESET, SRESET	V_{OL}	—	0.5	V

[1] V_{IL}(max) for the I^2C interface is 0.8 V rather than the 1.5 V as specified in the I^2C standard.

[2] Input capacitance is periodically sampled.

[3] A(0:31), TSIZ0/REG, TSIZ1, D(0:31), DP(0:3)/IRQ(3:6), RD/WR, BURST, RSV/IRQ2, IP_B(0:1)/IWP(0:1)/VFLS(0:1), IP_B2/IOIS16_B/AT2, IP_B3/IWP2/VF2, IP_B4/LWP0/VF0, IP_B5/LWP1/VF1, IP_B6/DSDI/AT0, IP_B7/PTR/AT3, RXD1/PA15, RXD2/PA13, L1TXDB/PA11, L1RXDB/PA10, L1TXDA/PA9, L1RXDA/PA8, TIN1/L1RCLKA/BRGO1/CLK1/PA7, BRGCLK1/TOUT1/CLK2/PA6, TIN2/L1TCLKA/BRGO2/CLK3/PA5, TOUT2/CLK4/PA4, TIN3/BRGO3/CLK5/PA3, BRGCLK2/L1RCLKB/TOUT3/CLK6/PA2, TIN4/BRGO4/CLK7/PA1, L1TCLKB/TOUT4/CLK8/PA0, REJCT1/SPISEL/PB31, SPICLK/PB30,SPIMOSI/PB29, BRGO4/SPIMISO/PB28, BRGO1/I2CSDA/PB27, BRGO2/I2CSCL/PB26, SMTXD1/PB25, SMRXD1/PB24, SMSYN1/SDACK1/PB23, SMSYN2/SDACK2/PB22, SMTXD2/L1CLKOB/PB21, SMRXD2/L1CLKOA/PB20, L1ST1/RTS1/PB19, L1ST2/RTS2/PB18, L1ST3/L1RQB/PB17, L1ST4/L1RQA/PB16, BRGO3/PB15, RSTRT1/PB14, L1ST1/RTS1/DREQ0/PC15, L1ST2/RTS2/DREQ1/PC14, L1ST3/L1RQB/PC13, L1ST4/L1RQA/PC12, CTS1/PC11, TGATE1/CD1/PC10, CTS2/PC9, TGATE2/CD2/PC8, SDACK2/L1TSYNCB/PC7, L1RSYNCB/PC6, SDACK1/L1TSYNCA/PC5, L1RSYNCA/PC4, PD15, PD14, PD13, PD12, PD11, PD10, PD9, PD8, PD5, PD6, PD7, PD4, PD3, MII_MDC, MII_TX_ER, MII_EN, MII_MDIO, and MII_TXD[0:3]

[4] BDIP/GPL_B(5), BR, BG, FRZ/IRQ6, CS(0:5), CS(6)/CE(1)_B, CS(7)/CE(2)_B, WE0/BS_B0/IORD, WE1/BS_B1/IOWR, WE2/BS_B2/PCOE, WE3/BS_B3/PCWE, BS_A(0:3), GPL_A0/GPL_B0, OE/GPL_A1/GPL_B1, GPL_A(2:3)/GPL_B(2:3)/CS(2:3), UPWAITA/GPL_A4, UPWAITB/GPL_B4, GPL_A5, ALE_A, CE1_A, CE2_A, ALE_B/DSCK/AT1, OP(0:1), OP2/MODCK1/STS, OP3/MODCK2/DSDO, and BADDR(28:30)

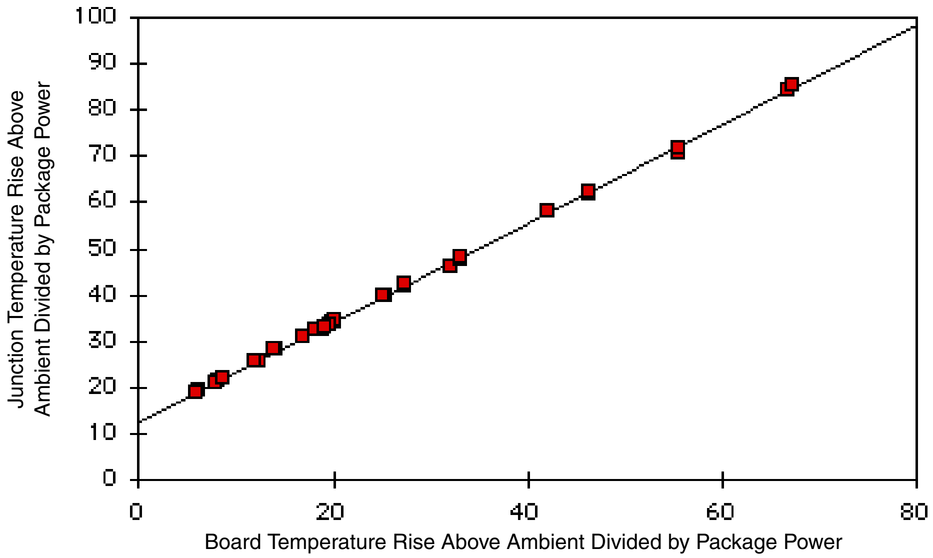


Figure 2. Effect of Board Temperature Rise on Thermal Behavior

If the board temperature is known, an estimate of the junction temperature in the environment can be made using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

$R_{\theta JB}$ = junction-to-board thermal resistance (ºC/W)
T_B = board temperature (ºC)
P_D = power dissipation in package

If the board temperature is known and the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. For this method to work, the board and board mounting must be similar to the test board used to determine the junction-to-board thermal resistance, namely a 2s2p (board with a power and a ground plane) and by attaching the thermal balls to the ground plane.

7.4 Estimation Using Simulation

When the board temperature is not known, a thermal simulation of the application is needed. The simple two-resistor model can be used with the thermal simulation of the application [2], or a more accurate and complex model of the package can be used in the thermal simulation.

7.5 Experimental Determination

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

Ψ_{JT} = thermal characterization parameter
T_T = thermocouple temperature on top of package
P_D = power dissipation in package

The thermal characterization parameter is measured per JEDEC JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

7.6 References

Semiconductor Equipment and Materials International 805 East Middlefield Rd. Mountain View, CA 94043	(415) 964-5111
MIL-SPEC and EIA/JESD (JEDEC) Specifications (Available from Global Engineering Documents)	800-854-7179 or 303-397-7956
JEDEC Specifications	http://www.jedec.org

1. C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.
2. B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212–220.

8 Layout Practices

Each V_{DD} pin on the MPC860 should be provided with a low-impedance path to the board’s supply. Each GND pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on the chip. The V_{DD} power supply should be bypassed to ground using at least four 0.1 µF-bypass capacitors located as close as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to chip V_{DD} and GND should be kept to less than half an inch per capacitor lead. A four-layer board employing two inner layers as V_{CC} and GND planes is recommended.

All output pins on the MPC860 have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized in order to minimize undershoot and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data buses. Maximum PC trace lengths of 6 inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the V_{CC} and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.

Figure 7 provides the timing for the synchronous input signals.

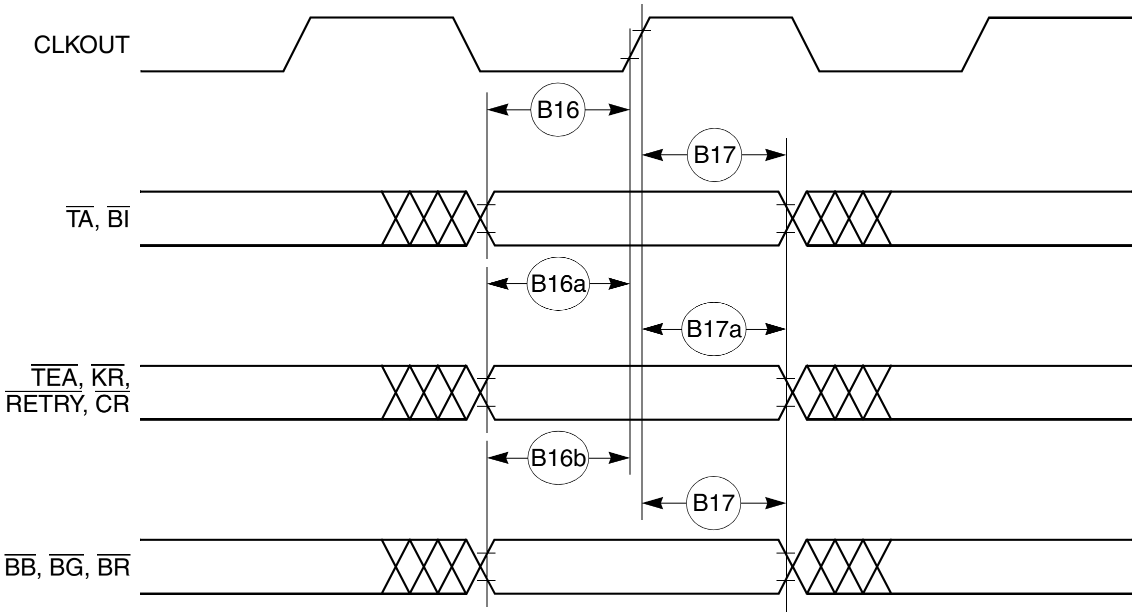


Figure 7. Synchronous Input Signals Timing

Figure 8 provides normal case timing for input data. It also applies to normal read accesses under the control of the UPM in the memory controller.

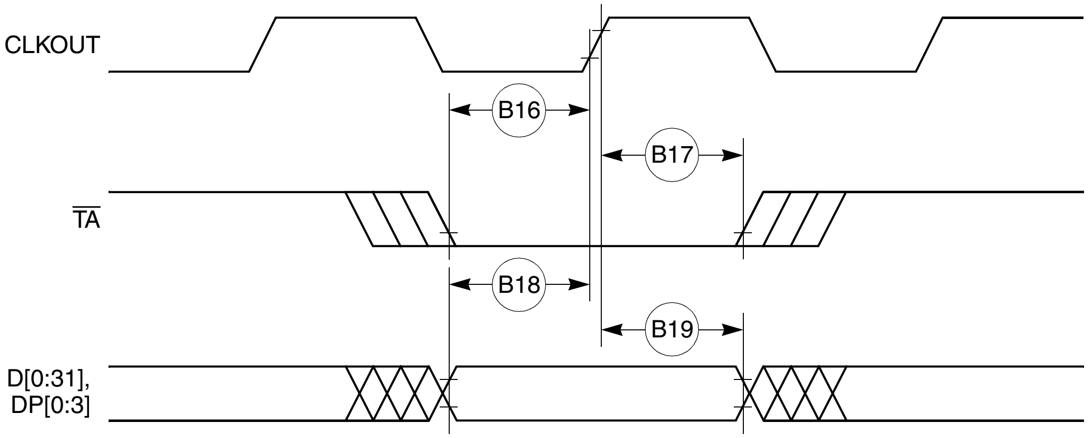


Figure 8. Input Data Timing in Normal Case

Figure 9 provides the timing for the input data controlled by the UPM for data beats where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

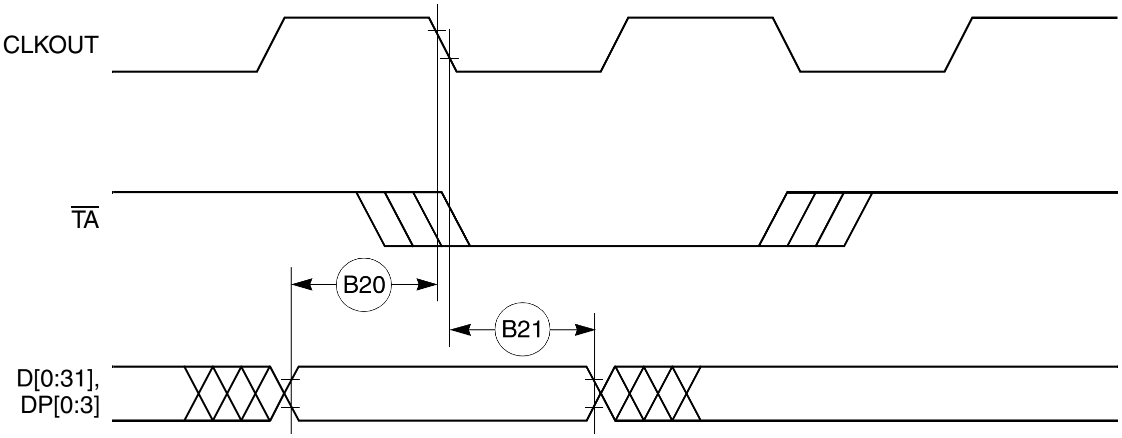


Figure 9. Input Data Timing when Controlled by UPM in the Memory Controller and DLT3 = 1

Figure 10 through Figure 13 provide the timing for the external bus read controlled by various GPCM factors.

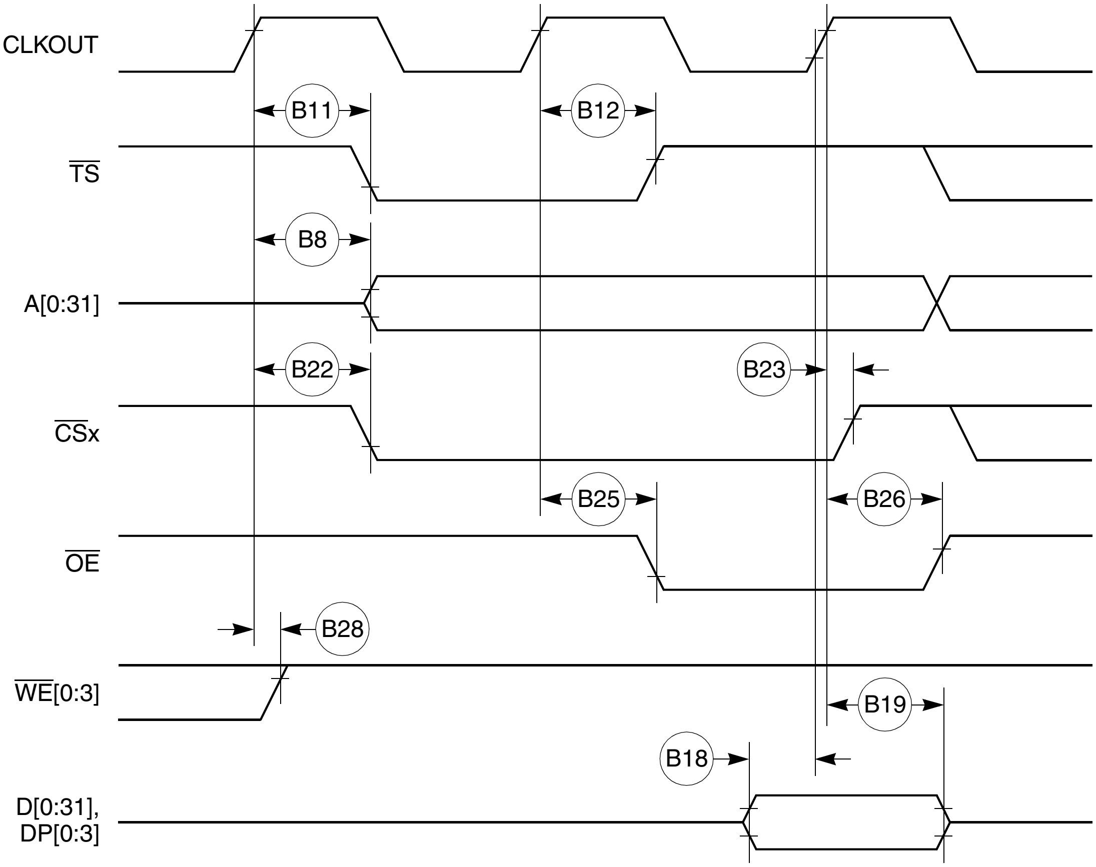


Figure 10. External Bus Read Timing (GPCM Controlled—ACS = 00)

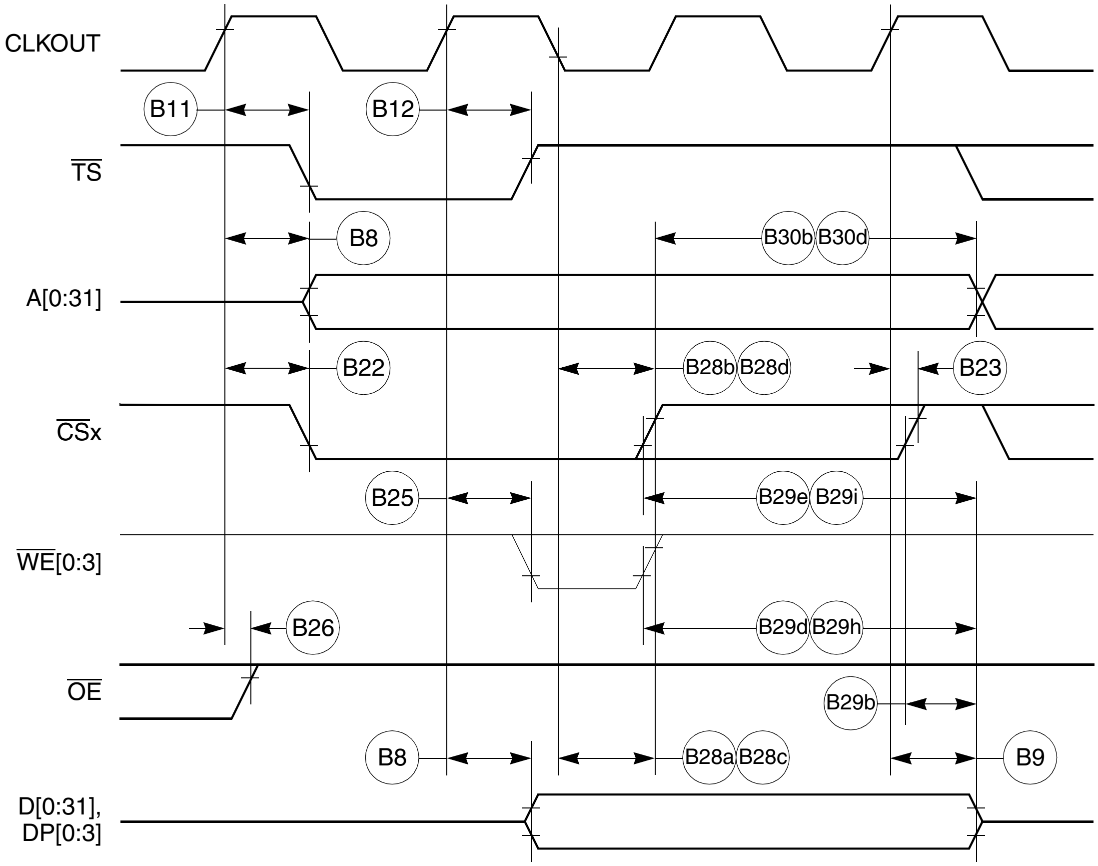


Figure 16. External Bus Write Timing (GPCM Controlled—TRLX = 0 or 1, CSNT = 1)

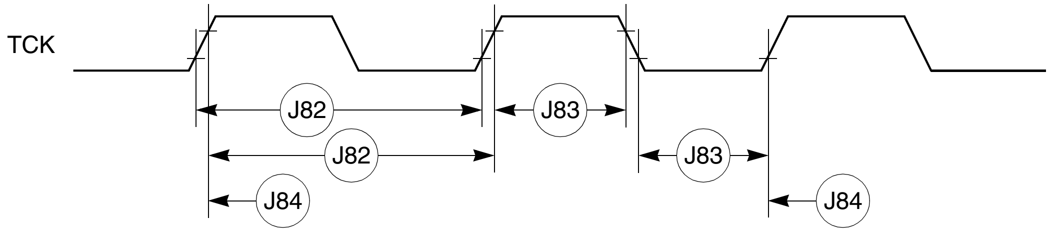


Figure 35. JTAG Test Clock Input Timing

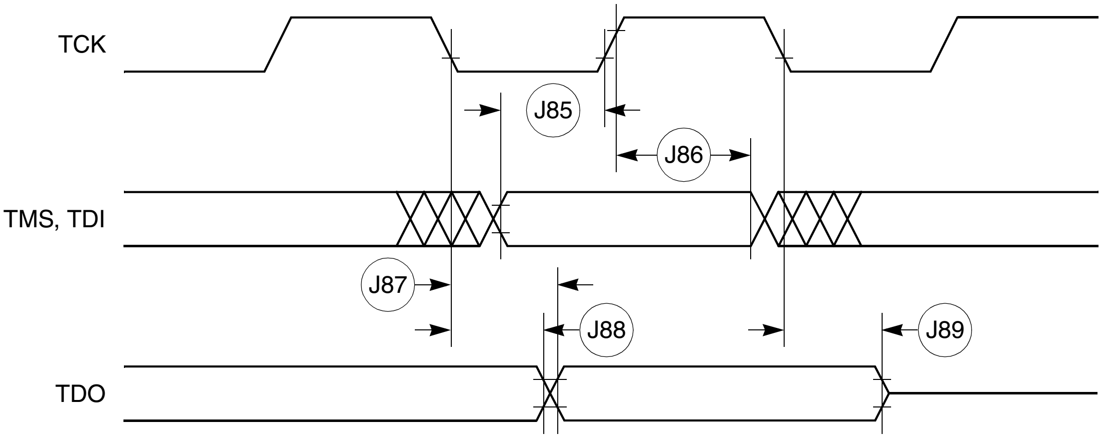


Figure 36. JTAG Test Access Port Timing Diagram

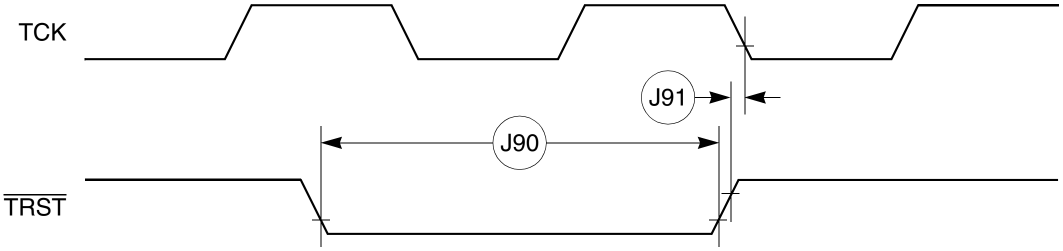


Figure 37. JTAG TRST Timing Diagram

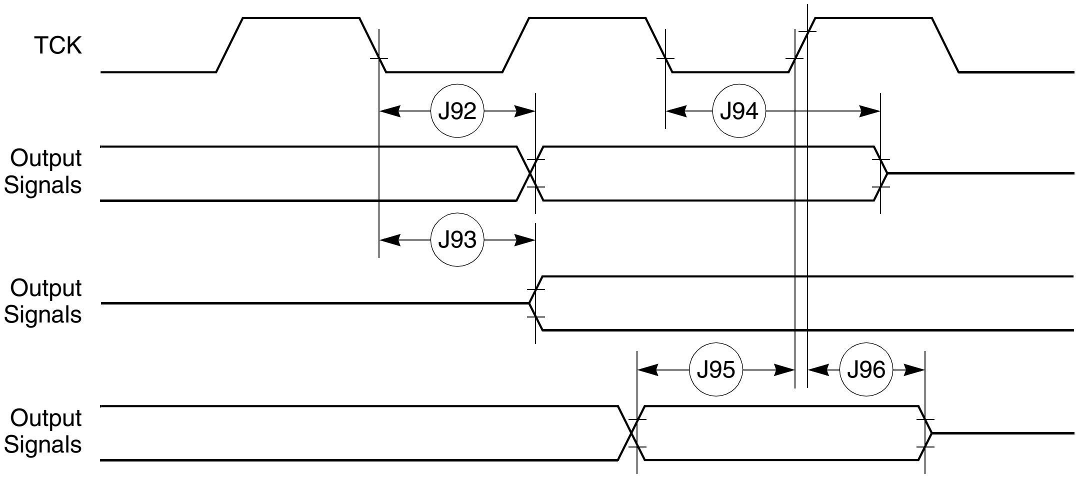


Figure 38. Boundary Scan (JTAG) Timing Diagram

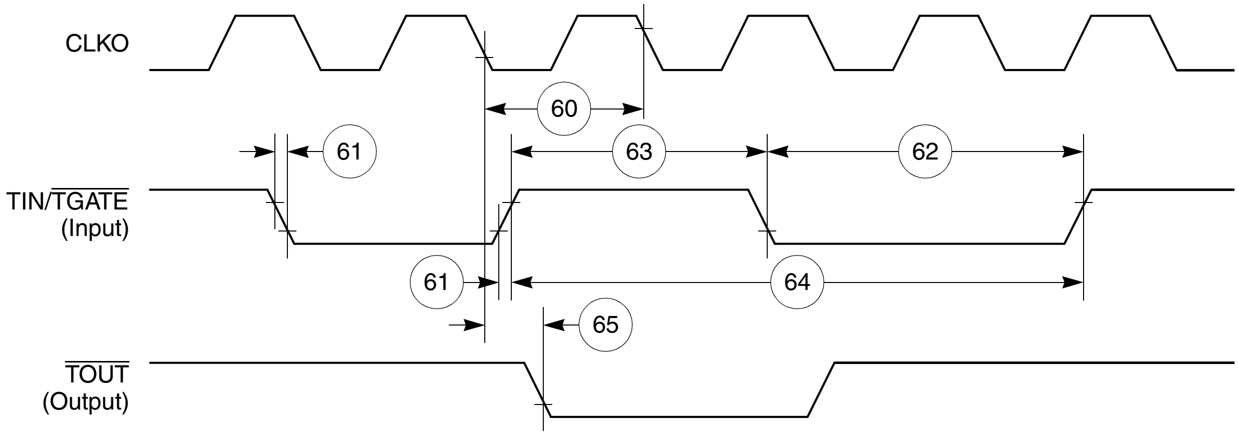


Figure 50. CPM General-Purpose Timers Timing Diagram

11.6 Serial Interface AC Electrical Specifications

Table 19 provides the serial interface timings as shown in Figure 51 through Figure 55.

Table 19. SI Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
70	L1RCLK, L1TCLK frequency (DSC = 0)[1, 2]	—	SYNCCLK/2.5	MHz
71	L1RCLK, L1TCLK width low (DSC = 0)[2]	P + 10	—	ns
71a	L1RCLK, L1TCLK width high (DSC = 0)[3]	P + 10	—	ns
72	L1TXD, L1ST(1–4), $\overline{\text{L1RQ}}$, L1CLKO rise/fall time	—	15.00	ns
73	L1RSYNC, L1TSYNC valid to L1CLK edge (SYNC setup time)	20.00	—	ns
74	L1CLK edge to L1RSYNC, L1TSYNC, invalid (SYNC hold time)	35.00	—	ns
75	L1RSYNC, L1TSYNC rise/fall time	—	15.00	ns
76	L1RXD valid to L1CLK edge (L1RXD setup time)	17.00	—	ns
77	L1CLK edge to L1RXD invalid (L1RXD hold time)	13.00	—	ns
78	L1CLK edge to L1ST(1–4) valid [4]	10.00	45.00	ns
78A	L1SYNC valid to L1ST(1–4) valid	10.00	45.00	ns
79	L1CLK edge to L1ST(1–4) invalid	10.00	45.00	ns
80	L1CLK edge to L1TXD valid	10.00	55.00	ns
80A	L1TSYNC valid to L1TXD valid [4]	10.00	55.00	ns
81	L1CLK edge to L1TXD high impedance	0.00	42.00	ns
82	L1RCLK, L1TCLK frequency (DSC =1)	—	16.00 or SYNCCLK/2	MHz
83	L1RCLK, L1TCLK width low (DSC = 1)	P + 10	—	ns
83a	L1RCLK, L1TCLK width high (DSC = 1)[3]	P + 10	—	ns

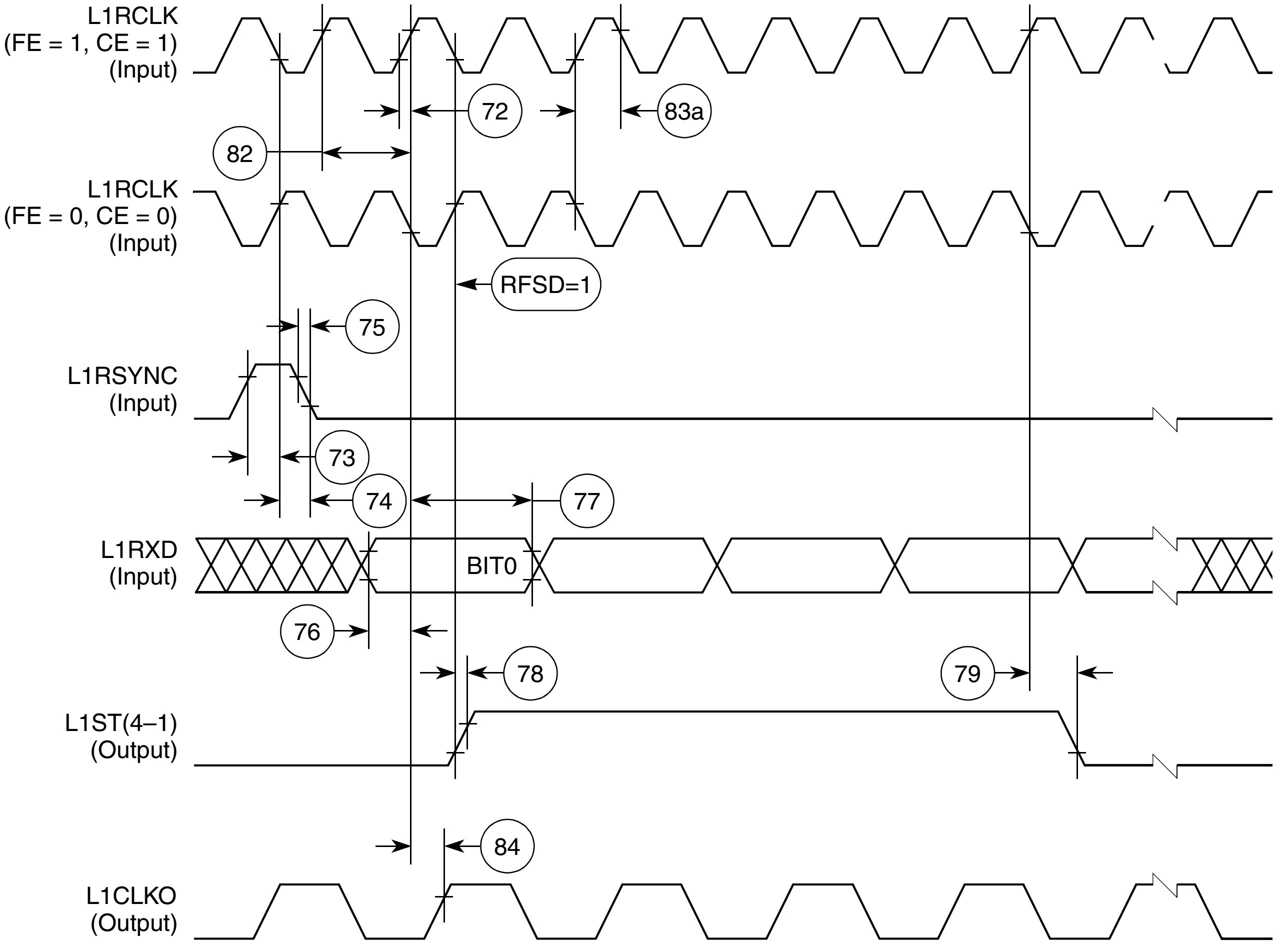


Figure 52. SI Receive Timing with Double-Speed Clocking (DSC = 1)

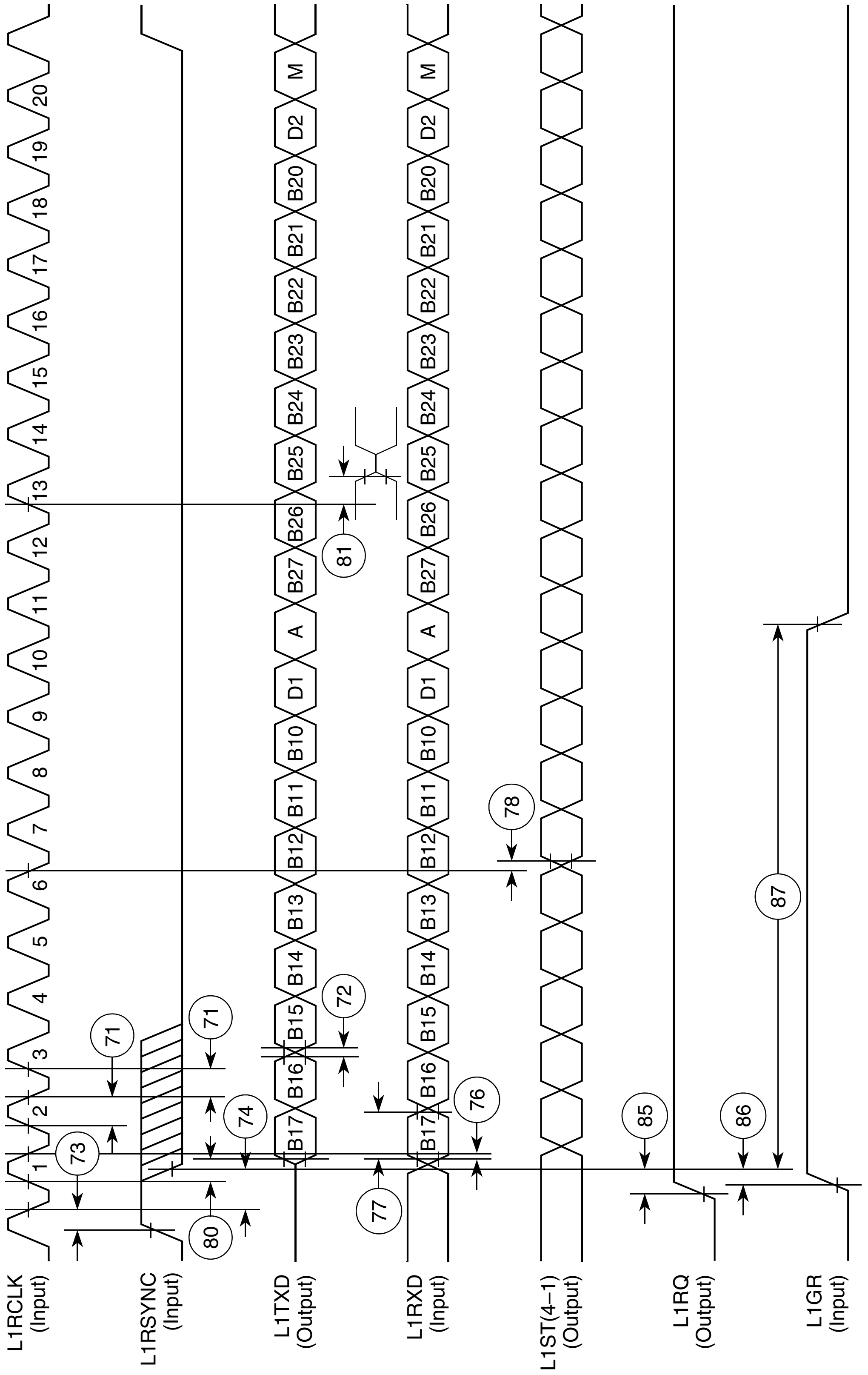


Figure 55. IDL Timing

Figure 56 through Figure 58 show the NMSI timings.

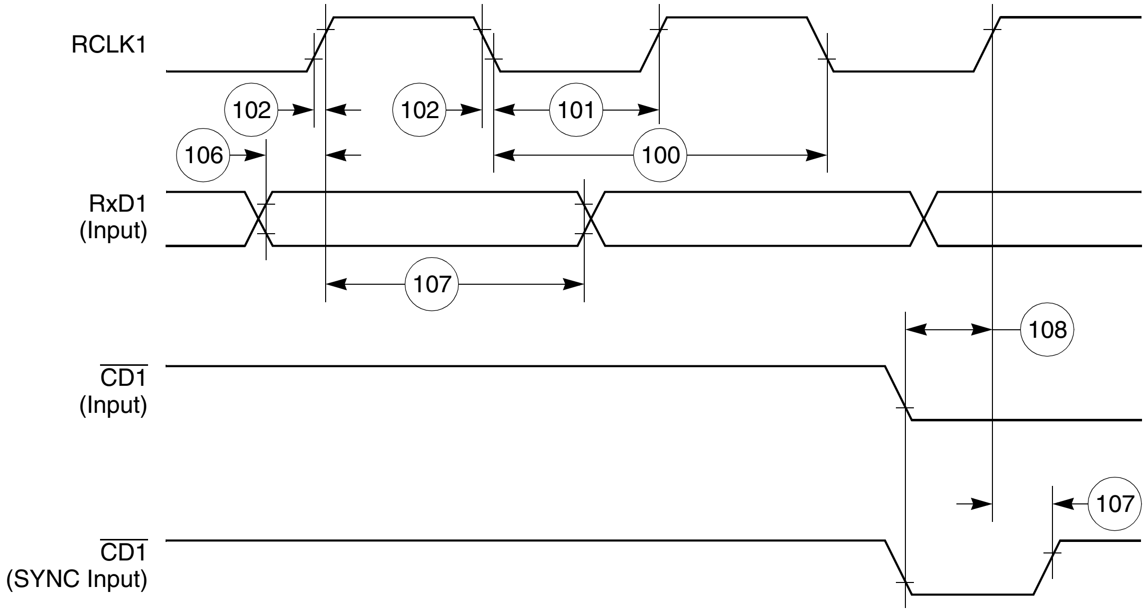


Figure 56. SCC NMSI Receive Timing Diagram

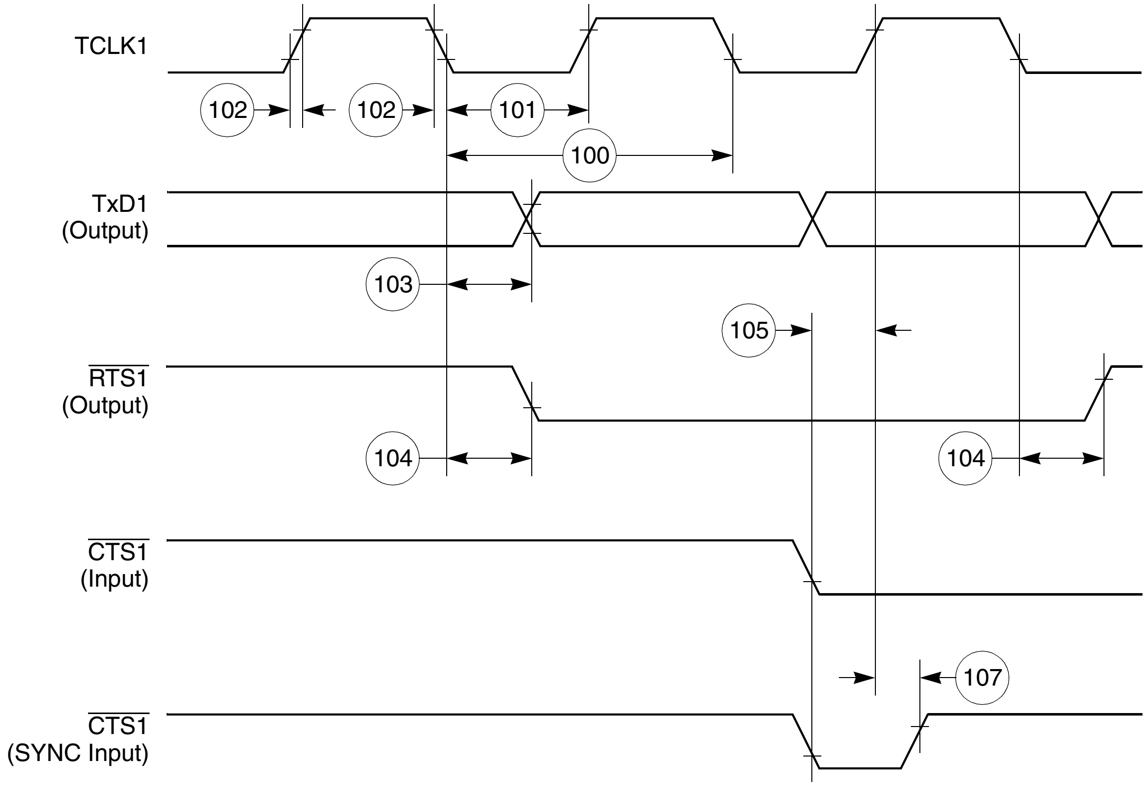


Figure 57. SCC NMSI Transmit Timing Diagram

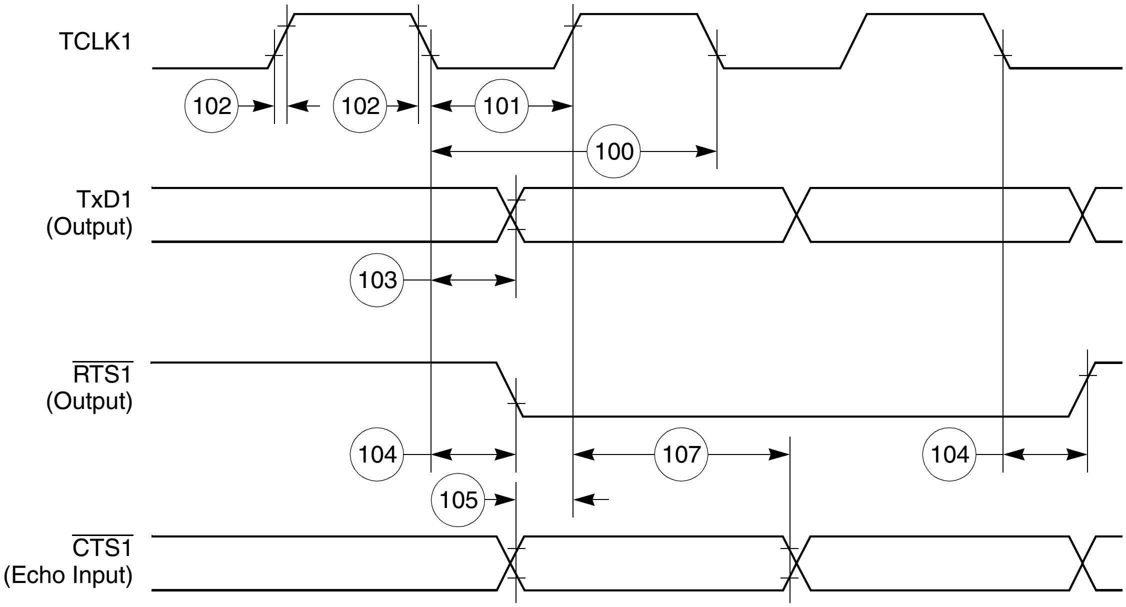


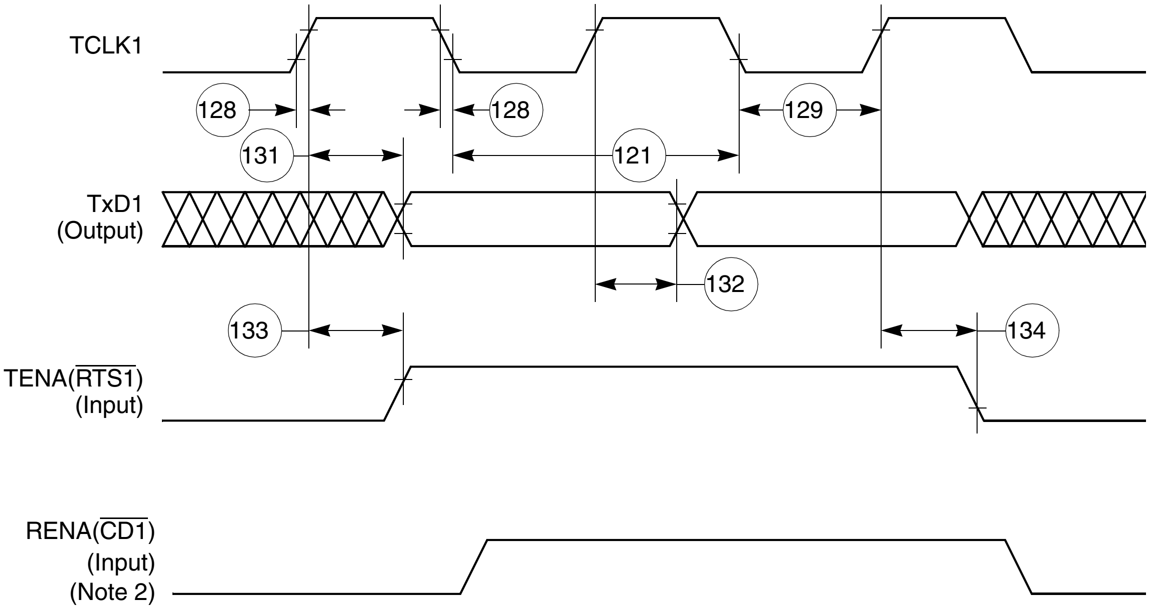
Figure 58. HDLC Bus Timing Diagram

11.8 Ethernet Electrical Specifications

Table 22 provides the Ethernet timings as shown in Figure 59 through Figure 63.

Table 22. Ethernet Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
120	CLSN width high	40	—	ns
121	RCLK1 rise/fall time	—	15	ns
122	RCLK1 width low	40	—	ns
123	RCLK1 clock period[1]	80	120	ns
124	RXD1 setup time	20	—	ns
125	RXD1 hold time	5	—	ns
126	RENA active delay (from RCLK1 rising edge of the last data bit)	10	—	ns
127	RENA width low	100	—	ns
128	TCLK1 rise/fall time	—	15	ns
129	TCLK1 width low	40	—	ns
130	TCLK1 clock period[1]	99	101	ns
131	TXD1 active delay (from TCLK1 rising edge)	10	50	ns
132	TXD1 inactive delay (from TCLK1 rising edge)	10	50	ns
133	TENA active delay (from TCLK1 rising edge)	10	50	ns
134	TENA inactive delay (from TCLK1 rising edge)	10	50	ns



Notes:

1. Transmit clock invert (TCI) bit in GSMR is set.
2. If RENA is deasserted before TENA, or RENA is not asserted at all during transmit, then the CSL bit is set in the buffer descriptor at the end of the frame transmission.

Figure 61. Ethernet Transmit Timing Diagram

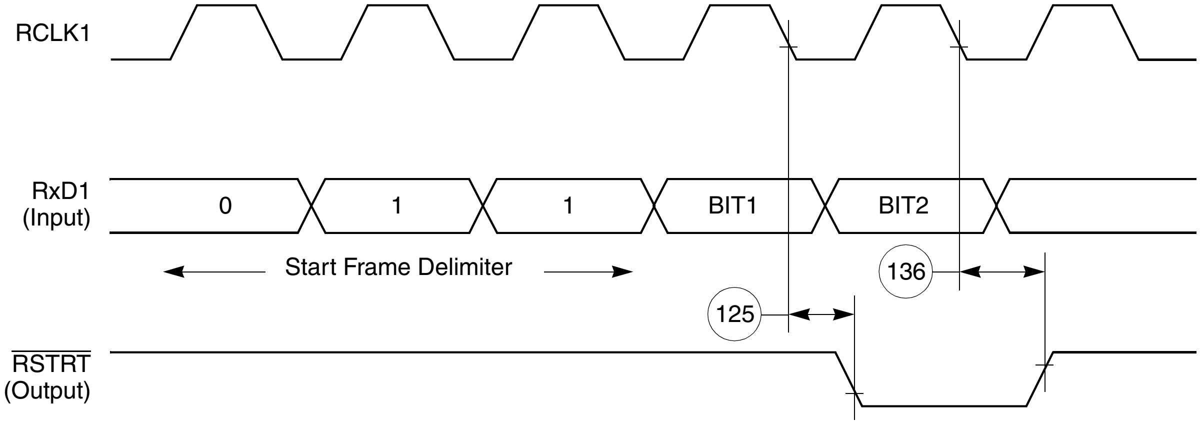


Figure 62. CAM Interface Receive Start Timing Diagram

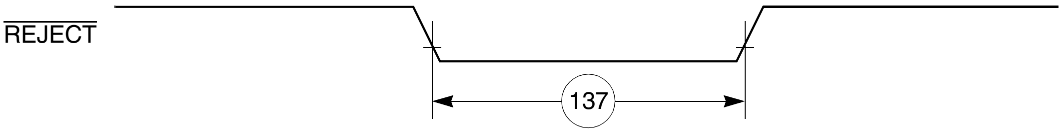


Figure 63. CAM Interface $\overline{\text{REJECT}}$ Timing Diagram

Figure 75 shows the MII serial management channel timing diagram.

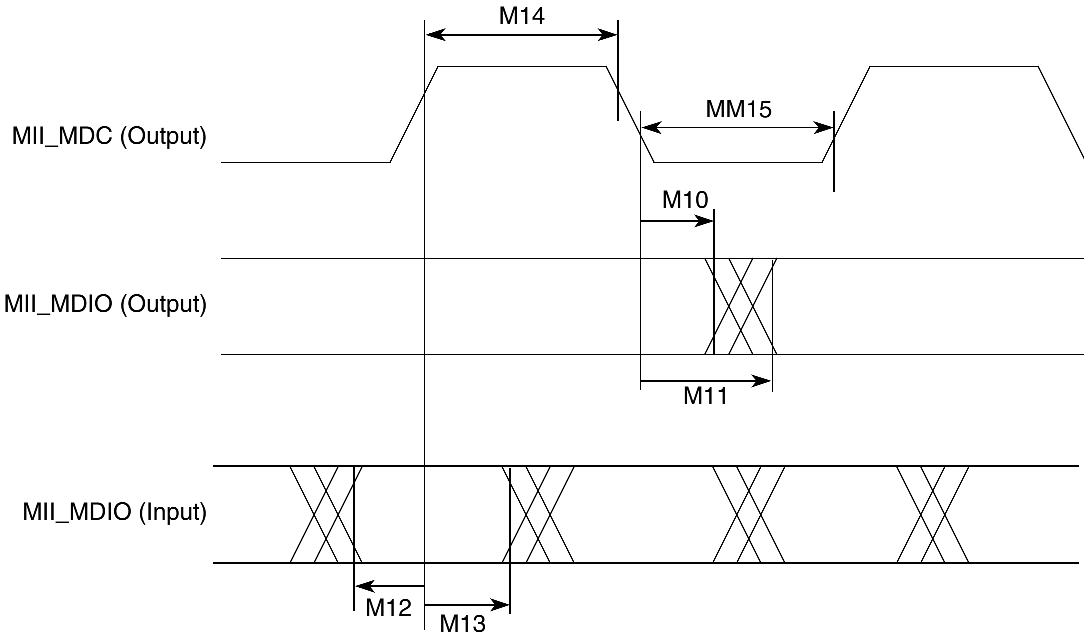


Figure 75. MII Serial Management Channel Timing Diagram

14 Mechanical Data and Ordering Information

14.1 Ordering Information

Table 33 provides information on the MPC860 Revision D.4 derivative devices.

Table 33. MPC860 Family Revision D.4 Derivatives

Device	Number of SCCs[1]	Ethernet Support[2] (Mbps)	Multichannel HDLC Support	ATM Support
MPC855T	1	10/100	Yes	Yes
MPC860DE	2	10	N/A	N/A
MPC860DT		10/100	Yes	Yes
MPC860DP		10/100	Yes	Yes
MPC860EN	4	10	N/A	N/A
MPC860SR		10	Yes	Yes
MPC860T		10/100	Yes	Yes
MPC860P		10/100	Yes	Yes

[1] Serial communications controller (SCC)

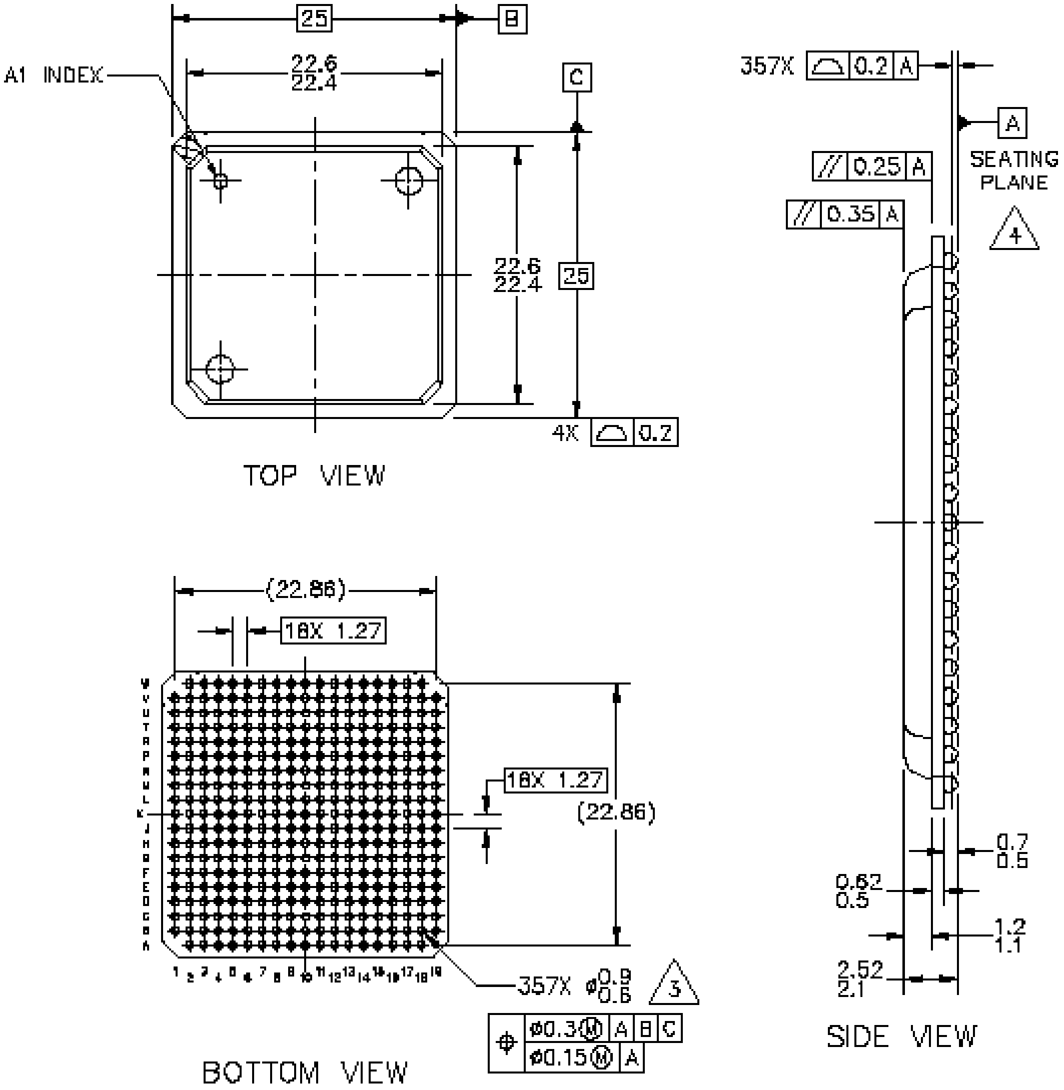
[2] Up to 4 channels at 40 MHz or 2 channels at 25 MHz

Table 34 identifies the packages and operating frequencies available for the MPC860.

Table 34. MPC860 Family Package/Frequency Availability

Package Type	Freq. (MHz) / Temp. (Tj)	Package	Order Number
Ball grid array ZP suffix—leaded ZQ suffix—leaded VR suffix—lead-free	50 0° to 95°C	ZP/ZQ[1]	MPC855TZQ50D4 MPC860DEZQ50D4 MPC860DTZQ50D4 MPC860ENZQ50D4 MPC860SRZQ50D4 MPC860TZQ50D4 MPC860DPZQ50D4 MPC860PZQ50D4
		Tape and Reel	MPC855TZQ50D4R2 MPC860DEZQ50D4R2 MPC860ENZQ50D4R2 MPC860SRZQ50D4R2 MPC860TZQ50D4R2 MPC860DPZQ50D4R2 MPC855TVR50D4R2 MPC860ENVR50D4R2 MPC860SRVR50D4R2 MPC860TVR50D4R2
		VR	MPC855TVR50D4 MPC860DEVR50D4 MPC860DPVR50D4 MPC860DTVR50D4 MPC860ENVR50D4 MPC860PVR50D4 MPC860SRVR50D4 MPC860TVR50D4
	66 0° to 95°C	ZP/ZQ[1]	MPC855TZQ66D4 MPC860DEZQ66D4 MPC860DTZQ66D4 MPC860ENZQ66D4 MPC860SRZQ66D4 MPC860TZQ66D4 MPC860DPZQ66D4 MPC860PZQ66D4
		Tape and Reel	MPC860SRZQ66D4R2 MPC860PZQ66D4R2
		VR	MPC855TVR66D4 MPC860DEVR66D4 MPC860DPVR66D4 MPC860DTVR66D4 MPC860ENVR66D4 MPC860PVR66D4 MPC860SRVR66D4 MPC860TVR66D4

Figure 78 shows the mechanical dimensions of the ZQ PBGA package.



NOTE

1. All Dimensions in millimeters.
2. Dimensions and tolerance per ASME Y14.5M, 1994.
3. Maximum Solder Ball Diameter measured parallel to Datum A.
4. Datum A, the seating plane, is defined by the spherical crowns of the solder balls.

Figure 78. Mechanical Dimensions and Bottom Surface Nomenclature of the ZQ PBGA Package