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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	50MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (4), 10/100Mbps (1)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 95°C (TA)
Security Features	-
Package / Case	357-BBGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc860tczq50d4

2 Features

The following list summarizes the key MPC860 features:

- Embedded single-issue, 32-bit core (implementing the Power Architecture technology) with thirty-two 32-bit general-purpose registers (GPRs)
    - The core performs branch prediction with conditional prefetch without conditional execution.
    - 4- or 8-Kbyte data cache and 4- or 16-Kbyte instruction cache (see Table 1)
        - 16-Kbyte instruction caches are four-way, set-associative with 256 sets; 4-Kbyte instruction caches are two-way, set-associative with 128 sets.
        - 8-Kbyte data caches are two-way, set-associative with 256 sets; 4-Kbyte data caches are two-way, set-associative with 128 sets.
        - Cache coherency for both instruction and data caches is maintained on 128-bit (4-word) cache blocks.
        - Caches are physically addressed, implement a least recently used (LRU) replacement algorithm, and are lockable on a cache block basis.
    - MMUs with 32-entry TLB, fully-associative instruction, and data TLBs
    - MMUs support multiple page sizes of 4-, 16-, and 512-Kbytes, and 8-Mbytes; 16 virtual address spaces and 16 protection groups
    - Advanced on-chip-emulation debug mode
- Up to 32-bit data bus (dynamic bus sizing for 8, 16, and 32 bits)
- 32 address lines
- Operates at up to 80 MHz
- Memory controller (eight banks)
    - Contains complete dynamic RAM (DRAM) controller
    - Each bank can be a chip select or $\overline{\text{RAS}}$ to support a DRAM bank.
    - Up to 15 wait states programmable per memory bank
    - Glueless interface to DRAM, SIMMS, SRAM, EPROM, Flash EPROM, and other memory devices
    - DRAM controller programmable to support most size and speed memory interfaces
    - Four $\overline{\text{CAS}}$ lines, four $\overline{\text{WE}}$ lines, and one $\overline{\text{OE}}$ line
    - Boot chip-select available at reset (options for 8-, 16-, or 32-bit memory)
    - Variable block sizes (32 Kbytes to 256 Mbytes)
    - Selectable write protection
    - On-chip bus arbitration logic
- General-purpose timers
    - Four 16-bit timers or two 32-bit timers
    - Gate mode can enable/disable counting
    - Interrupt can be masked on reference match and event capture.

- System integration unit (SIU)
  - Bus monitor
  - Software watchdog
  - Periodic interrupt timer (PIT)
  - Low-power stop mode
  - Clock synthesizer
  - Decrementer, time base, and real-time clock (RTC)
  - Reset controller
  - IEEE 1149.1™ Std. test access port (JTAG)
- Interrupts
  - Seven external interrupt request (IRQ) lines
  - 12 port pins with interrupt capability
  - 23 internal interrupt sources
  - Programmable priority between SCCs
  - Programmable highest priority request
- 10/100 Mbps Ethernet support, fully compliant with the IEEE 802.3u® Standard (not available when using ATM over UTOPIA interface)
- ATM support compliant with ATM forum UNI 4.0 specification
  - Cell processing up to 50–70 Mbps at 50-MHz system clock
  - Cell multiplexing/demultiplexing
  - Support of AAL5 and AAL0 protocols on a per-VC basis. AAL0 support enables OAM and software implementation of other protocols.
  - ATM pace control (APC) scheduler, providing direct support for constant bit rate (CBR) and unspecified bit rate (UBR) and providing control mechanisms enabling software support of available bit rate (ABR)
  - Physical interface support for UTOPIA (10/100-Mbps is not supported with this interface) and byte-aligned serial (for example, T1/E1/ADSL)
  - UTOPIA-mode ATM supports level-1 master with cell-level handshake, multi-PHY (up to four physical layer devices), connection to 25-, 51-, or 155-Mbps framers, and UTOPIA/system clock ratios of 1/2 or 1/3.
  - Serial-mode ATM connection supports transmission convergence (TC) function for T1/E1/ADSL lines, cell delineation, cell payload scrambling/descrambling, automatic idle/unassigned cell insertion/stripping, header error control (HEC) generation, checking, and statistics.
- Communications processor module (CPM)
  - RISC communications processor (CP)
  - Communication-specific commands (for example, GRACEFUL STOP TRANSMIT, ENTER HUNT MODE, and RESTART TRANSMIT)
  - Supports continuous mode transmission and reception on all serial channels

3 Maximum Tolerated Ratings

This section provides the maximum tolerated voltage and temperature ranges for the MPC860. Table 2 provides the maximum ratings.

This device contains circuitry protecting against damage due to high-static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or V_{DD}).

Table 2. Maximum Tolerated Ratings

(GND = 0 V)

Rating	Symbol	Value	Unit
Supply voltage[1]	V_{DDH}	–0.3 to 4.0	V
	V_{DDL}	–0.3 to 4.0	V
	KAPWR	–0.3 to 4.0	V
	V_{DDSYN}	–0.3 to 4.0	V
Input voltage[2]	V_{in}	GND – 0.3 to V_{DDH}	V
Temperature[3] (standard)	$T_{A(min)}$	0	°C
	$T_{j(max)}$	95	°C
Temperature[3] (extended)	$T_{A(min)}$	–40	°C
	$T_{j(max)}$	95	°C
Storage temperature range	T_{stg}	–55 to 150	°C

[1] The power supply of the device must start its ramp from 0.0 V.

[2] Functional operating conditions are provided with the DC electrical specifications in Table 6. Absolute maximum ratings are stress ratings only; functional operation at the maxima is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device.
Caution: All inputs that tolerate 5 V cannot be more than 2.5 V greater than the supply voltage. This restriction applies to power-up and normal operation (that is, if the MPC860 is unpowered, voltage greater than 2.5 V must not be applied to its inputs).

[3] Minimum temperatures are guaranteed as ambient temperature, T_A. Maximum temperatures are guaranteed as junction temperature, T_j.

Table 6. DC Electrical Specifications (continued)

Characteristic	Symbol	Min	Max	Unit
Input leakage current, V_{in} = 3.6 V (except TMS, TRST, DSCK, and DSDI pins)	I_{In}	—	10	µA
Input leakage current, V_{in} = 0 V (except TMS, TRST, DSCK, and DSDI pins)	I_{In}	—	10	µA
Input capacitance[2]	C_{in}	—	20	pF
Output high voltage, I_{OH} = –2.0 mA, V_{DDH} = 3.0 V (except XTAL, XFC, and open-drain pins)	V_{OH}	2.4	—	V
Output low voltage I_{OL} = 2.0 mA, CLKOUT I_{OL} = 3.2 mA [3] I_{OL} = 5.3 mA [4] I_{OL} = 7.0 mA, TXD1/PA14, TXD2/PA12 I_{OL} = 8.9 mA, TS, TA, TEA, BI, BB, HRESET, SRESET	V_{OL}	—	0.5	V

[1] V_{IL}(max) for the I^2C interface is 0.8 V rather than the 1.5 V as specified in the I^2C standard.

[2] Input capacitance is periodically sampled.

[3] A(0:31), TSIZ0/REG, TSIZ1, D(0:31), DP(0:3)/IRQ(3:6), RD/WR, BURST, RSV/IRQ2, IP_B(0:1)/IWP(0:1)/VFLS(0:1), IP_B2/IOIS16_B/AT2, IP_B3/IWP2/VF2, IP_B4/LWP0/VF0, IP_B5/LWP1/VF1, IP_B6/DSDI/AT0, IP_B7/PTR/AT3, RXD1/PA15, RXD2/PA13, L1TXDB/PA11, L1RXDB/PA10, L1TXDA/PA9, L1RXDA/PA8, TIN1/L1RCLKA/BRGO1/CLK1/PA7, BRGCLK1/TOUT1/CLK2/PA6, TIN2/L1TCLKA/BRGO2/CLK3/PA5, TOUT2/CLK4/PA4, TIN3/BRGO3/CLK5/PA3, BRGCLK2/ L1RCLKB/TOUT3/CLK6/PA2, TIN4/BRGO4/CLK7/PA1, L1TCLKB/TOUT4/CLK8/PA0, REJCT1/SPISEL/PB31, SPICLK/ PB30,SPIMOSI/PB29, BRGO4/SPIMISO/PB28, BRGO1/I2CSDA/PB27, BRGO2/I2CSCL/PB26, SMTXD1/PB25, SMRXD1/ PB24, SMSYN1/SDACK1/PB23, SMSYN2/SDACK2/PB22, SMTXD2/L1CLKOB/PB21, SMRXD2/L1CLKOA/PB20, L1ST1/ RTS1/PB19, L1ST2/RTS2/PB18, L1ST3/L1RQB/PB17, L1ST4/L1RQA/PB16, BRGO3/PB15, RSTRT1/PB14, L1ST1/RTS1/ DREQ0/PC15, L1ST2/RTS2/DREQ1/PC14, L1ST3/L1RQB/PC13, L1ST4/L1RQA/PC12, CTS1/PC11, TGATE1/CD1/PC10, CTS2/PC9, TGATE2/CD2/PC8, SDACK2/L1TSYNCB/PC7, L1RSYNCB/PC6, SDACK1/L1TSYNCA/PC5, L1RSYNCA/PC4, PD15, PD14, PD13, PD12, PD11, PD10, PD9, PD8, PD5, PD6, PD7, PD4, PD3, MII_MDC, MII_TX_ER, MII_EN, MII_MDIO, and MII_TXD[0:3]

[4] BDIP/GPL_B(5), BR, BG, FRZ/IRQ6, CS(0:5), CS(6)/CE(1)_B, CS(7)/CE(2)_B, WE0/BS_B0/IORD, WE1/BS_B1/IOWR, WE2/BS_B2/PCOE, WE3/BS_B3/PCWE, BS_A(0:3), GPL_A0/GPL_B0, OE/GPL_A1/GPL_B1, GPL_A(2:3)/GPL_B(2:3)/ CS(2:3), UPWAITA/GPL_A4, UPWAITB/GPL_B4, GPL_A5, ALE_A, CE1_A, CE2_A, ALE_B/DSCK/AT1, OP(0:1), OP2/MODCK1/STS, OP3/MODCK2/DSDO, and BADDR(28:30)

7 Thermal Calculation and Measurement

For the following discussions, $P_D = (V_{DD} \times I_{DD}) + PI/O$, where PI/O is the power dissipation of the I/O drivers.

7.1 Estimation with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J, in ºC can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_A = ambient temperature (ºC)
$R_{\theta JA}$ = package junction-to-ambient thermal resistance (ºC/W)
P_D = power dissipation in package

The junction-to-ambient thermal resistance is an industry standard value which provides a quick and easy estimation of thermal performance. However, the answer is only an estimate; test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

7.2 Estimation with Junction-to-Case Thermal Resistance

Historically, the thermal resistance has frequently been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (ºC/W)
$R_{\theta JC}$ = junction-to-case thermal resistance (ºC/W)
$R_{\theta CA}$ = case-to-ambient thermal resistance (ºC/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user adjusts the thermal environment to affect the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the airflow around the device, add a heat sink, change the mounting arrangement on the printed-circuit board, or change the thermal dissipation on the printed-circuit board surrounding the device. This thermal model is most useful for ceramic packages with heat sinks where some 90% of the heat flows through the case and the heat sink to the ambient environment. For most packages, a better model is required.

7.3 Estimation with Junction-to-Board Thermal Resistance

A simple package thermal model which has demonstrated reasonable accuracy (about 20%) is a two-resistor model consisting of a junction-to-board and a junction-to-case thermal resistance. The junction-to-case thermal resistance covers the situation where a heat sink is used or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed-circuit board. It has been observed that the thermal performance of most plastic packages, especially PBGA packages, is strongly dependent on the board temperature; see Figure 2.

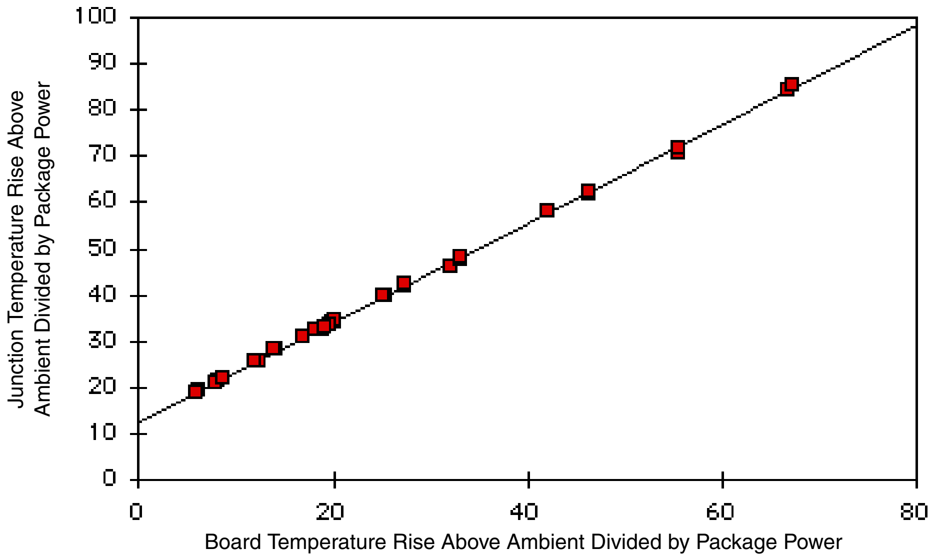


Figure 2. Effect of Board Temperature Rise on Thermal Behavior

If the board temperature is known, an estimate of the junction temperature in the environment can be made using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

$R_{\theta JB}$ = junction-to-board thermal resistance (ºC/W)
T_B = board temperature (ºC)
P_D = power dissipation in package

If the board temperature is known and the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. For this method to work, the board and board mounting must be similar to the test board used to determine the junction-to-board thermal resistance, namely a 2s2p (board with a power and a ground plane) and by attaching the thermal balls to the ground plane.

7.4 Estimation Using Simulation

When the board temperature is not known, a thermal simulation of the application is needed. The simple two-resistor model can be used with the thermal simulation of the application [2], or a more accurate and complex model of the package can be used in the thermal simulation.

7.5 Experimental Determination

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

9 Bus Signal Timing

Table 7 provides the bus operation timing for the MPC860 at 33, 40, 50, and 66 MHz.

The maximum bus speed supported by the MPC860 is 66 MHz. Higher-speed parts must be operated in half-speed bus mode (for example, an MPC860 used at 80 MHz must be configured for a 40-MHz bus).

The timing for the MPC860 bus shown assumes a 50-pF load for maximum delays and a 0-pF load for minimum delays.

Table 7. Bus Operation Timings

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B1	CLKOUT period	30.30	30.30	25.00	30.30	20.00	30.30	15.15	30.30	ns
B1a	EXTCLK to CLKOUT phase skew (EXTCLK > 15 MHz and MF <= 2)	–0.90	0.90	–0.90	0.90	–0.90	0.90	–0.90	0.90	ns
B1b	EXTCLK to CLKOUT phase skew (EXTCLK > 10 MHz and MF < 10)	–2.30	2.30	–2.30	2.30	–2.30	2.30	–2.30	2.30	ns
B1c	CLKOUT phase jitter (EXTCLK > 15 MHz and MF <= 2)[1]	–0.60	0.60	–0.60	0.60	–0.60	0.60	–0.60	0.60	ns
B1d	CLKOUT phase jitter[1]	–2.00	2.00	–2.00	2.00	–2.00	2.00	–2.00	2.00	ns
B1e	CLKOUT frequency jitter (MF < 10)[1]	—	0.50	—	0.50	—	0.50	—	0.50	%
B1f	CLKOUT frequency jitter (10 < MF < 500)[1]	—	2.00	—	2.00	—	2.00	—	2.00	%
B1g	CLKOUT frequency jitter (MF > 500)[1]	—	3.00	—	3.00	—	3.00	—	3.00	%
B1h	Frequency jitter on EXTCLK[2]	—	0.50	—	0.50	—	0.50	—	0.50	%
B2	CLKOUT pulse width low	12.12	—	10.00	—	8.00	—	6.06	—	ns
B3	CLKOUT width high	12.12	—	10.00	—	8.00	—	6.06	—	ns
B4	CLKOUT rise time[3]	—	4.00	—	4.00	—	4.00	—	4.00	ns
B5[33]	CLKOUT fall time[3]	—	4.00	—	4.00	—	4.00	—	4.00	ns
B7	CLKOUT to A(0:31), BADDR(28:30), RD/$\overline{\text{WR}}$, $\overline{\text{BURST}}$, D(0:31), DP(0:3) invalid	7.58	—	6.25	—	5.00	—	3.80	—	ns
B7a	CLKOUT to TSIZ(0:1), $\overline{\text{REG}}$, $\overline{\text{RSV}}$, AT(0:3), $\overline{\text{BDIP}}$, PTR invalid	7.58	—	6.25	—	5.00	—	3.80	—	ns
B7b	CLKOUT to $\overline{\text{BR}}$, $\overline{\text{BG}}$, FRZ, VFLS(0:1), VF(0:2) IWP(0:2), LWP(0:1), $\overline{\text{STS}}$ invalid [4]	7.58	—	6.25	—	5.00	—	3.80	—	ns
B8	CLKOUT to A(0:31), BADDR(28:30) RD/$\overline{\text{WR}}$, $\overline{\text{BURST}}$, D(0:31), DP(0:3) valid	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.04	ns
B8a	CLKOUT to TSIZ(0:1), $\overline{\text{REG}}$, $\overline{\text{RSV}}$, AT(0:3) $\overline{\text{BDIP}}$, PTR valid	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.04	ns
B8b	CLKOUT to $\overline{\text{BR}}$, $\overline{\text{BG}}$, VFLS(0:1), VF(0:2), IWP(0:2), FRZ, LWP(0:1), $\overline{\text{STS}}$ valid [4]	7.58	14.33	6.25	13.00	5.00	11.75	3.80	10.04	ns

Table 7. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B35	A(0:31), BADDR(28:30) to $\overline{CS}$ valid—as requested by control bit BST4 in the corresponding word in UPM	5.58	—	4.25	—	3.00	—	1.79	—	ns
B35a	A(0:31), BADDR(28:30), and D(0:31) to $\overline{BS}$ valid—as requested by control bit BST1 in the corresponding word in UPM	13.15	—	10.50	—	8.00	—	5.58	—	ns
B35b	A(0:31), BADDR(28:30), and D(0:31) to $\overline{BS}$ valid—as requested by control bit BST2 in the corresponding word in UPM	20.73	—	16.75	—	13.00	—	9.36	—	ns
B36	A(0:31), BADDR(28:30), and D(0:31) to $\overline{GPL}$ valid—as requested by control bit GxT4 in the corresponding word in UPM	5.58	—	4.25	—	3.00	—	1.79	—	ns
B37	UPWAIT valid to CLKOUT falling edge[9]	6.00	—	6.00	—	6.00	—	6.00	—	ns
B38	CLKOUT falling edge to UPWAIT valid[9]	1.00	—	1.00	—	1.00	—	1.00	—	ns
B39	$\overline{AS}$ valid to CLKOUT rising edge[10]	7.00	—	7.00	—	7.00	—	7.00	—	ns
B40	A(0:31), TSIZ(0:1), RD/$\overline{WR}$, $\overline{BURST}$, valid to CLKOUT rising edge	7.00	—	7.00	—	7.00	—	7.00	—	ns
B41	$\overline{TS}$ valid to CLKOUT rising edge (setup time)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B42	CLKOUT rising edge to $\overline{TS}$ valid (hold time)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B43	$\overline{AS}$ negation to memory controller signals negation	—	TBD	—	TBD	—	TBD	—	TBD	ns

[1] Phase and frequency jitter performance results are only valid if the input jitter is less than the prescribed value.

[2] If the rate of change of the frequency of EXTAL is slow (that is, it does not jump between the minimum and maximum values in one cycle) or the frequency of the jitter is fast (that is, it does not stay at an extreme value for a long time) then the maximum allowed jitter on EXTAL can be up to 2%.

[3] The timings specified in B4 and B5 are based on full strength clock.

[4] The timing for $\overline{BR}$ output is relevant when the MPC860 is selected to work with external bus arbiter. The timing for $\overline{BG}$ output is relevant when the MPC860 is selected to work with internal bus arbiter.

[5] The timing required for $\overline{BR}$ input is relevant when the MPC860 is selected to work with internal bus arbiter. The timing for $\overline{BG}$ input is relevant when the MPC860 is selected to work with external bus arbiter.

[6] The D(0:31) and DP(0:3) input timings B18 and B19 refer to the rising edge of the CLKOUT in which the $\overline{TA}$ input signal is asserted.

[7] The D(0:31) and DP(0:3) input timings B20 and B21 refer to the falling edge of the CLKOUT. This timing is valid only for read accesses controlled by chip-selects under control of the UPM in the memory controller, for data beats where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

[8] The timing B30 refers to $\overline{CS}$ when ACS = 00 and to $\overline{WE}$(0:3) when CSNT = 0.

[9] The signal UPWAIT is considered asynchronous to the CLKOUT and synchronized internally. The timings specified in B37 and B38 are specified to enable the freeze of the UPM output signals as described in Figure 18.

[10] The $\overline{AS}$ signal is considered asynchronous to the CLKOUT. The timing B39 is specified in order to allow the behavior specified in Figure 21.

Figure 7 provides the timing for the synchronous input signals.

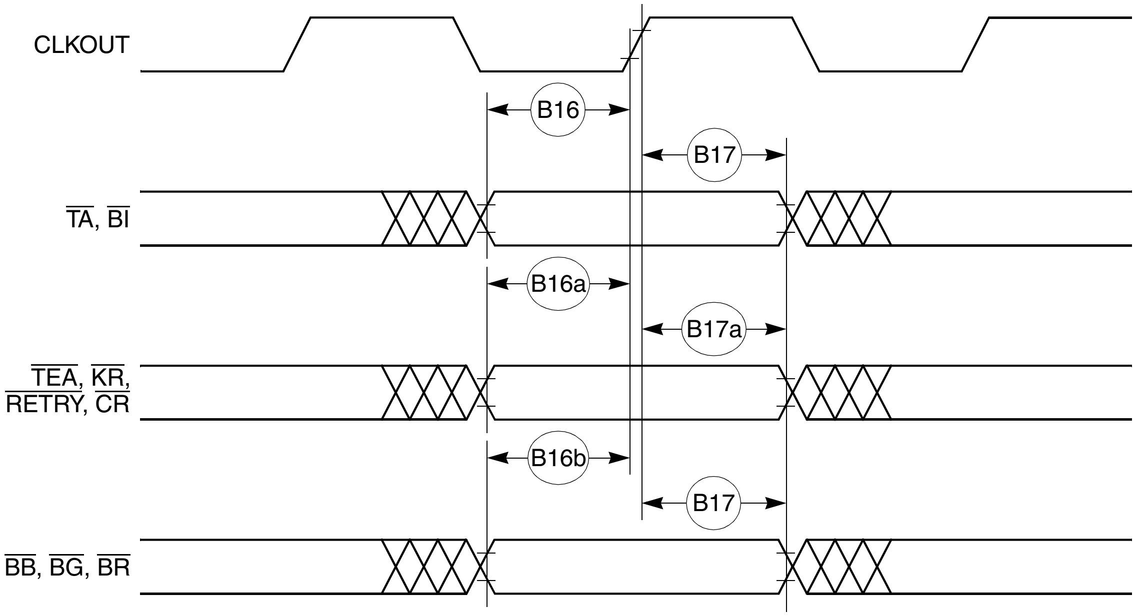


Figure 7. Synchronous Input Signals Timing

Figure 8 provides normal case timing for input data. It also applies to normal read accesses under the control of the UPM in the memory controller.

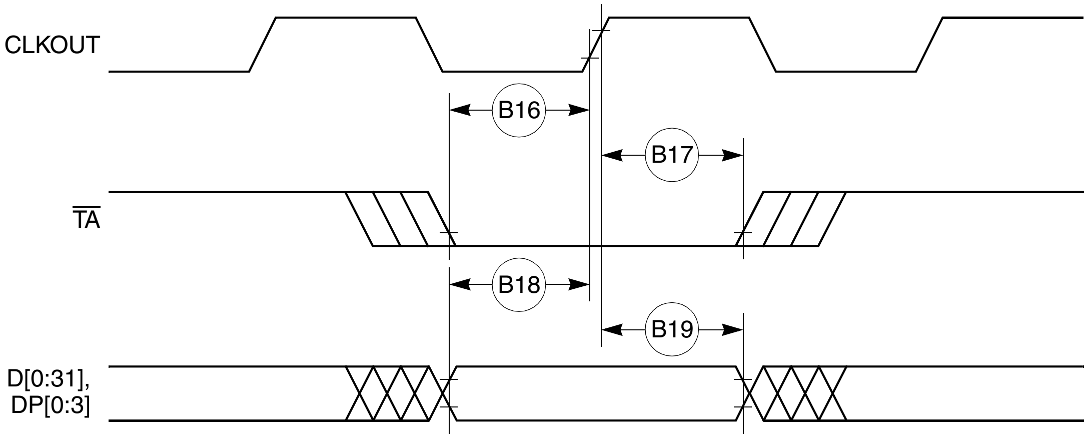


Figure 8. Input Data Timing in Normal Case

Figure 25 provides the PCMCIA access cycle timing for the external bus read.

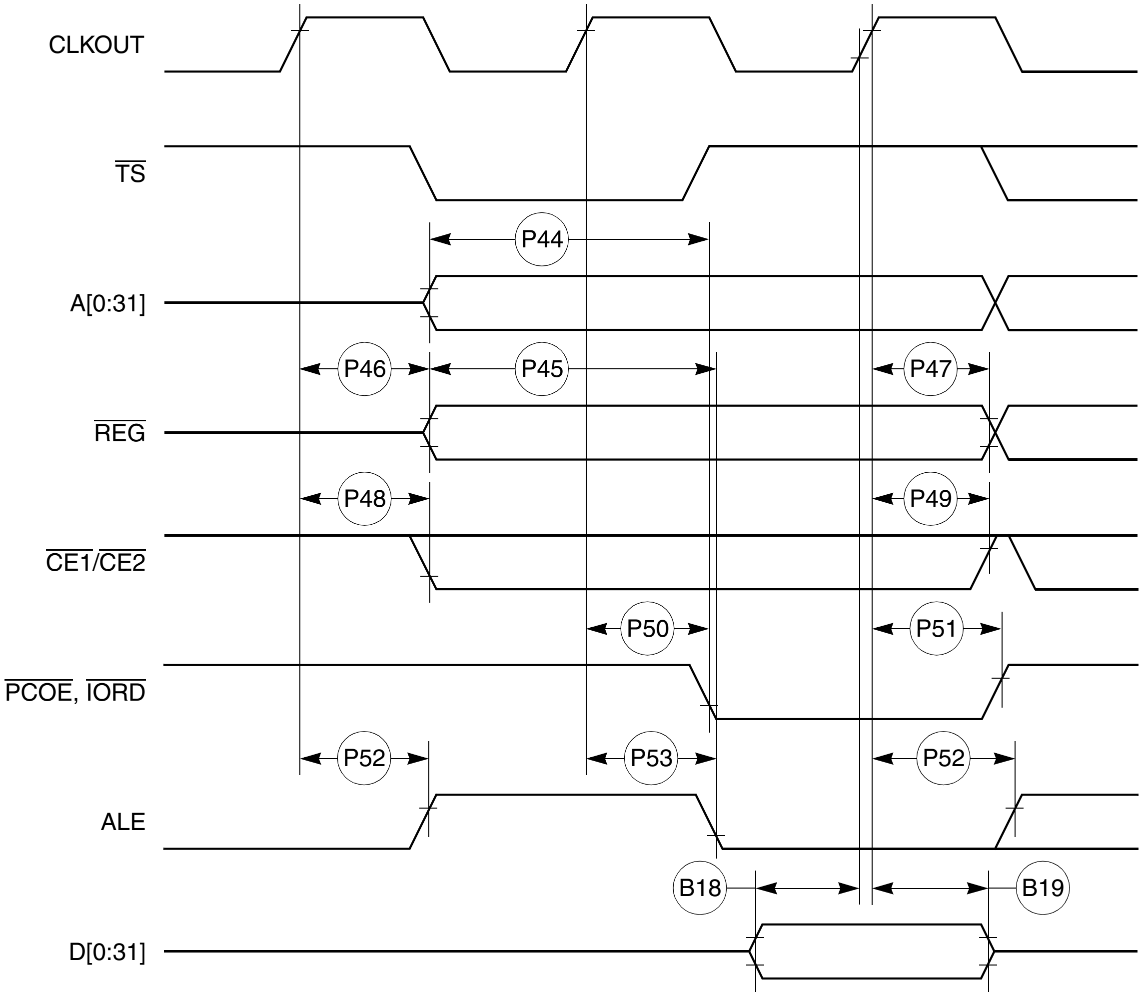


Figure 25. PCMCIA Access Cycle Timing External Bus Read

Figure 32 shows the reset timing for the data bus configuration.

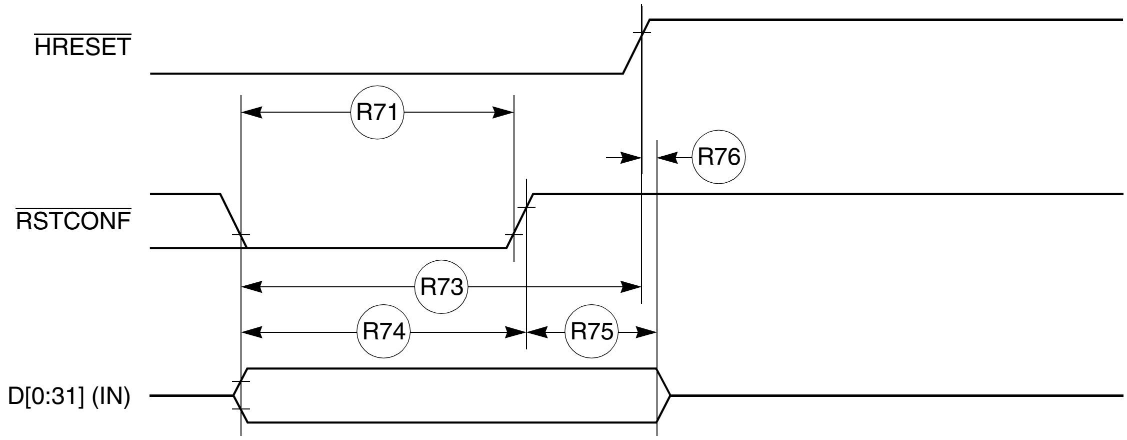


Figure 32. Reset Timing—Configuration from Data Bus

Figure 33 provides the reset timing for the data bus weak drive during configuration.

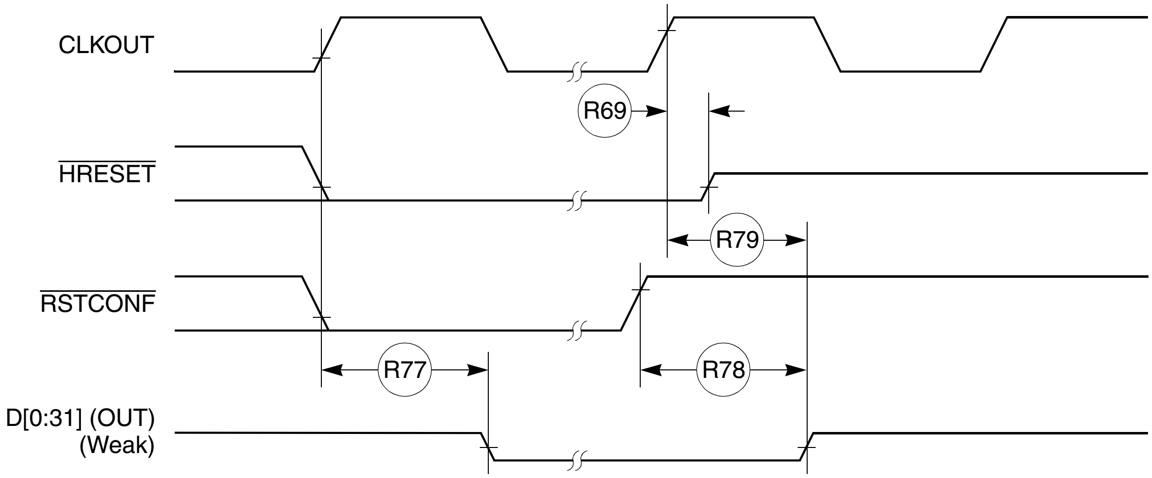


Figure 33. Reset Timing—Data Bus Weak Drive During Configuration

Figure 34 provides the reset timing for the debug port configuration.

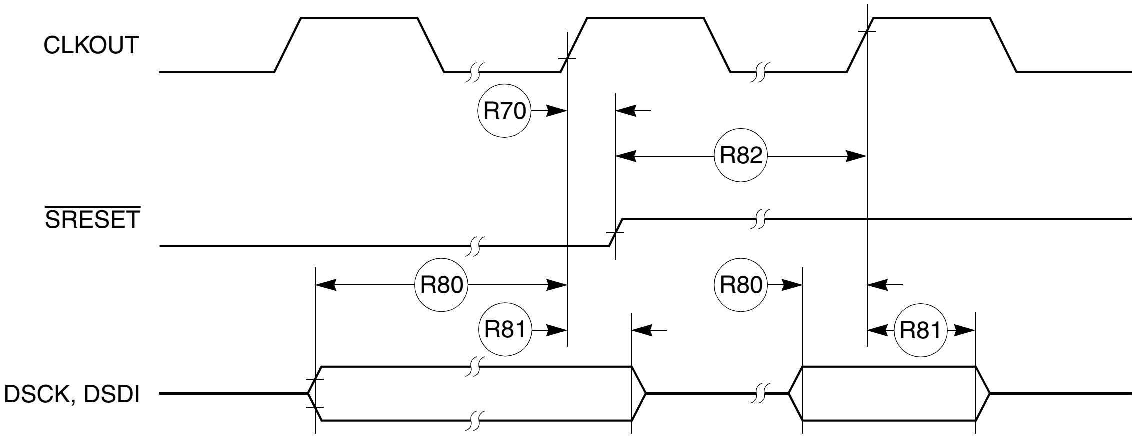


Figure 34. Reset Timing—Debug Port Configuration

10 IEEE 1149.1 Electrical Specifications

Table 13 provides the JTAG timings for the MPC860 shown in Figure 35 through Figure 38.

Table 13. JTAG Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
J82	TCK cycle time	100.00	—	ns
J83	TCK clock pulse width measured at 1.5 V	40.00	—	ns
J84	TCK rise and fall times	0.00	10.00	ns
J85	TMS, TDI data setup time	5.00	—	ns
J86	TMS, TDI data hold time	25.00	—	ns
J87	TCK low to TDO data valid	—	27.00	ns
J88	TCK low to TDO data invalid	0.00	—	ns
J89	TCK low to TDO high impedance	—	20.00	ns
J90	$\overline{\text{TRST}}$ assert time	100.00	—	ns
J91	$\overline{\text{TRST}}$ setup time to TCK low	40.00	—	ns
J92	TCK falling edge to output valid	—	50.00	ns
J93	TCK falling edge to output valid out of high impedance	—	50.00	ns
J94	TCK falling edge to output high impedance	—	50.00	ns
J95	Boundary scan input valid to TCK rising edge	50.00	—	ns
J96	TCK rising edge to boundary scan input invalid	50.00	—	ns

11 CPM Electrical Characteristics

This section provides the AC and DC electrical specifications for the communications processor module (CPM) of the MPC860.

11.1 PIP/PIO AC Electrical Specifications

Table 14 provides the PIP/PIO AC timings as shown in Figure 39 through Figure 43.

Table 14. PIP/PIO Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
21	Data-in setup time to STBI low	0	—	ns
22	Data-in hold time to STBI high	2.5 – t3[1]	—	CLK
23	STBI pulse width	1.5	—	CLK
24	STBO pulse width	1 CLK – 5 ns	—	ns
25	Data-out setup time to STBO low	2	—	CLK
26	Data-out hold time from STBO high	5	—	CLK
27	STBI low to STBO low (Rx interlock)	—	2	CLK
28	STBI low to STBO high (Tx interlock)	2	—	CLK
29	Data-in setup time to clock high	15	—	ns
30	Data-in hold time from clock high	7.5	—	ns
31	Clock low to data-out valid (CPU writes data, control, or direction)	—	25	ns

[1] t3 = Specification 23.

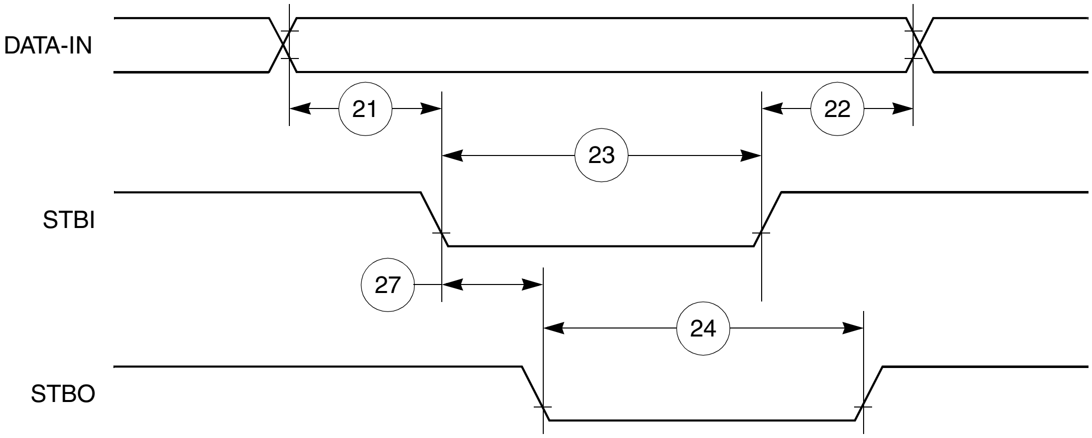


Figure 39. PIP Rx (Interlock Mode) Timing Diagram

11.7 SCC in NMSI Mode Electrical Specifications

Table 20 provides the NMSI external clock timing.

Table 20. NMSI External Clock Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
100	RCLK1 and TCLK1 width high[1]	1/SYNCCLK	—	ns
101	RCLK1 and TCLK1 width low	1/SYNCCLK + 5	—	ns
102	RCLK1 and TCLK1 rise/fall time	—	15.00	ns
103	TXD1 active delay (from TCLK1 falling edge)	0.00	50.00	ns
104	$\overline{\text{RTS1}}$ active/inactive delay (from TCLK1 falling edge)	0.00	50.00	ns
105	$\overline{\text{CTS1}}$ setup time to TCLK1 rising edge	5.00	—	ns
106	RXD1 setup time to RCLK1 rising edge	5.00	—	ns
107	RXD1 hold time from RCLK1 rising edge[2]	5.00	—	ns
108	$\overline{\text{CD1}}$ setup Time to RCLK1 rising edge	5.00	—	ns

[1] The ratios SYNCCLK/RCLK1 and SYNCCLK/TCLK1 must be greater than or equal to 2.25/1.

[2] Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as external sync signals.

Table 21 provides the NMSI internal clock timing.

Table 21. NMSI Internal Clock Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
100	RCLK1 and TCLK1 frequency[1]	0.00	SYNCCLK/3	MHz
102	RCLK1 and TCLK1 rise/fall time	—	—	ns
103	TXD1 active delay (from TCLK1 falling edge)	0.00	30.00	ns
104	$\overline{\text{RTS1}}$ active/inactive delay (from TCLK1 falling edge)	0.00	30.00	ns
105	$\overline{\text{CTS1}}$ setup time to TCLK1 rising edge	40.00	—	ns
106	RXD1 setup time to RCLK1 rising edge	40.00	—	ns
107	RXD1 hold time from RCLK1 rising edge[2]	0.00	—	ns
108	$\overline{\text{CD1}}$ setup time to RCLK1 rising edge	40.00	—	ns

[1] The ratios SYNCCLK/RCLK1 and SYNCCLK/TCLK1 must be greater than or equal to 3/1.

[2] Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as external sync signals.

Figure 56 through Figure 58 show the NMSI timings.

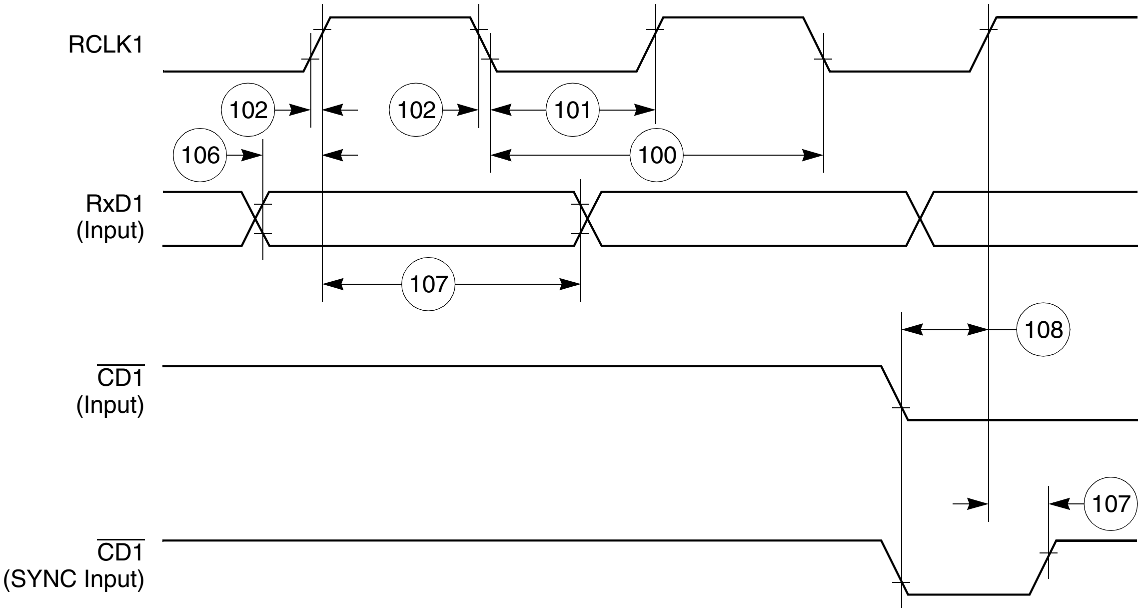


Figure 56. SCC NMSI Receive Timing Diagram

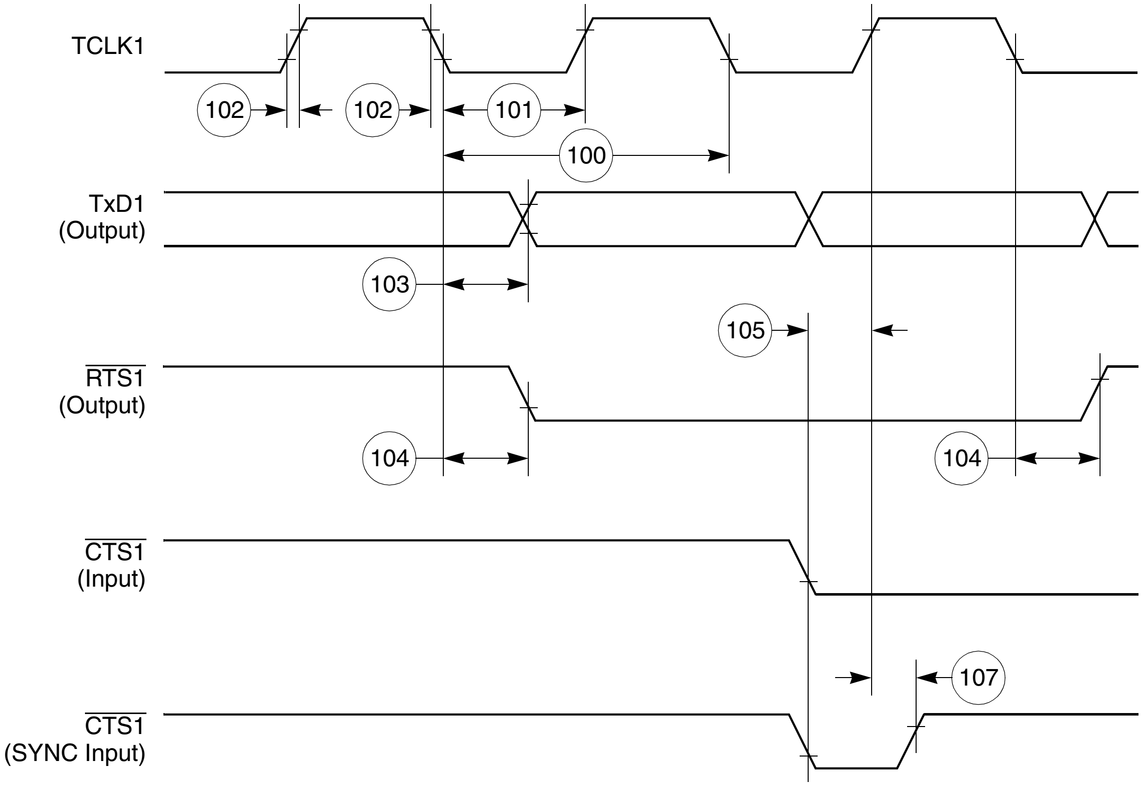


Figure 57. SCC NMSI Transmit Timing Diagram

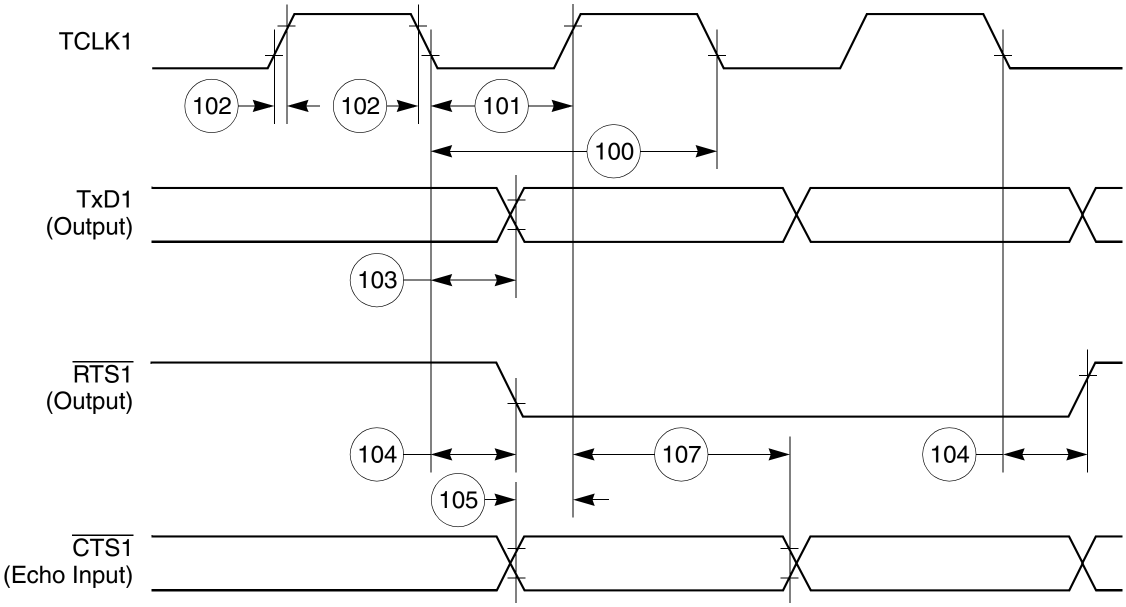


Figure 58. HDLC Bus Timing Diagram

11.8 Ethernet Electrical Specifications

Table 22 provides the Ethernet timings as shown in Figure 59 through Figure 63.

Table 22. Ethernet Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
120	CLSN width high	40	—	ns
121	RCLK1 rise/fall time	—	15	ns
122	RCLK1 width low	40	—	ns
123	RCLK1 clock period[1]	80	120	ns
124	RXD1 setup time	20	—	ns
125	RXD1 hold time	5	—	ns
126	RENA active delay (from RCLK1 rising edge of the last data bit)	10	—	ns
127	RENA width low	100	—	ns
128	TCLK1 rise/fall time	—	15	ns
129	TCLK1 width low	40	—	ns
130	TCLK1 clock period[1]	99	101	ns
131	TXD1 active delay (from TCLK1 rising edge)	10	50	ns
132	TXD1 inactive delay (from TCLK1 rising edge)	10	50	ns
133	TENA active delay (from TCLK1 rising edge)	10	50	ns
134	TENA inactive delay (from TCLK1 rising edge)	10	50	ns

Table 22. Ethernet Timing (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
135	$\overline{\text{RSTRT}}$ active delay (from TCLK1 falling edge)	10	50	ns
136	$\overline{\text{RSTRT}}$ inactive delay (from TCLK1 falling edge)	10	50	ns
137	$\overline{\text{REJECT}}$ width low	1	—	CLK
138	CLKO1 low to $\overline{\text{SDACK}}$ asserted[2]	—	20	ns
139	CLKO1 low to $\overline{\text{SDACK}}$ negated[2]	—	20	ns

[1] The ratios SYNCCLK/RCLK1 and SYNCCLK/TCLK1 must be greater than or equal to 2/1.

[2] $\overline{\text{SDACK}}$ is asserted whenever the SDMA writes the incoming frame DA into memory.

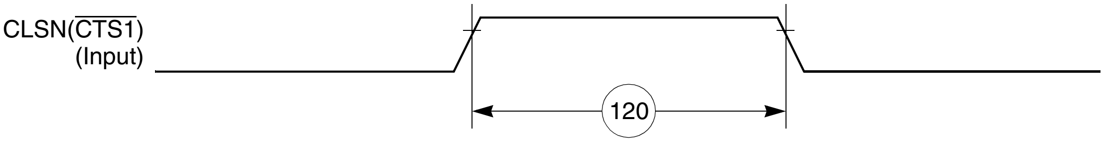


Figure 59. Ethernet Collision Timing Diagram

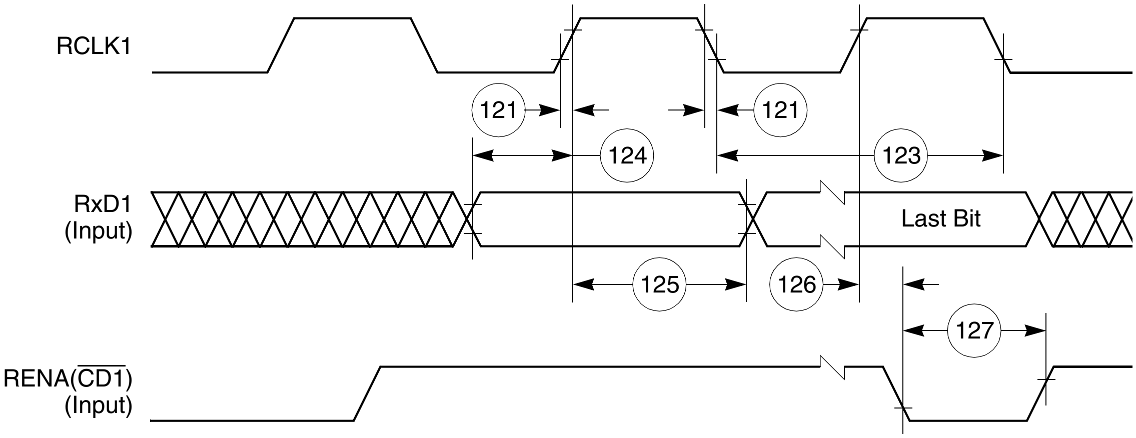
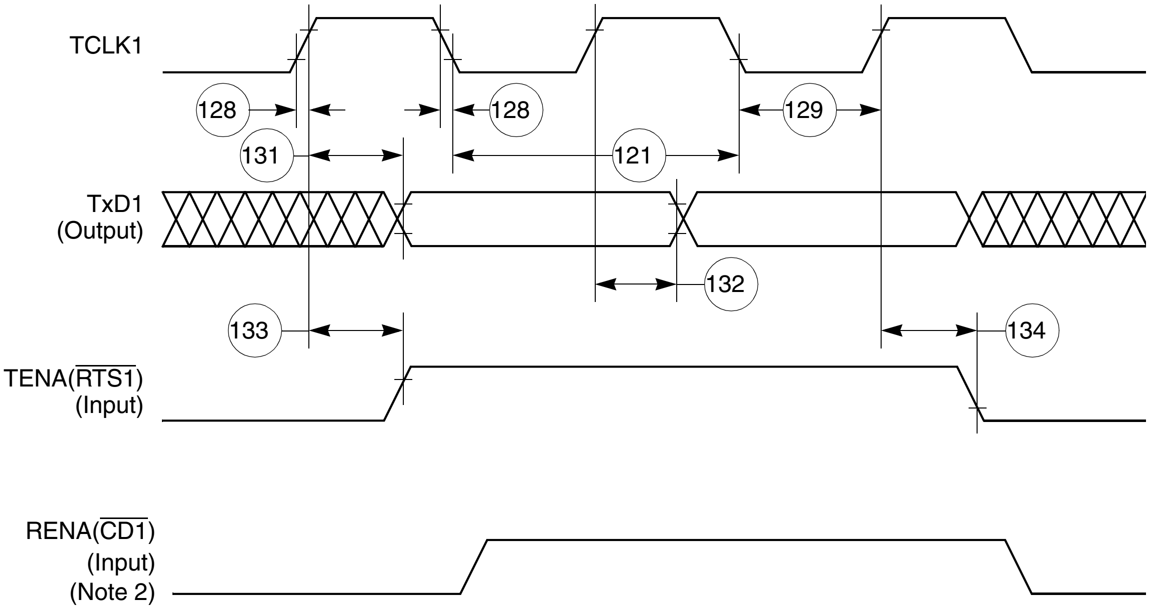


Figure 60. Ethernet Receive Timing Diagram



Notes:

1. Transmit clock invert (TCI) bit in GSMR is set.
2. If RENA is deasserted before TENA, or RENA is not asserted at all during transmit, then the CSL bit is set in the buffer descriptor at the end of the frame transmission.

Figure 61. Ethernet Transmit Timing Diagram

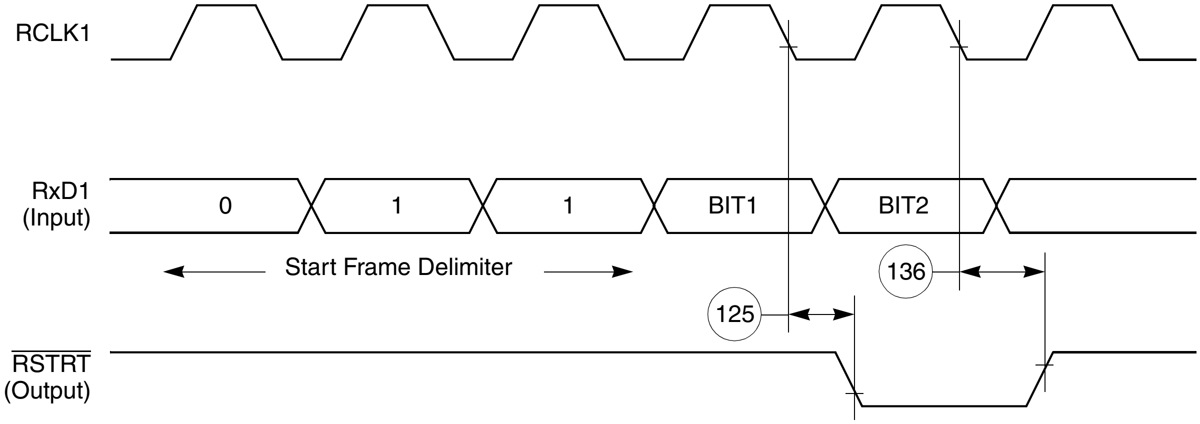


Figure 62. CAM Interface Receive Start Timing Diagram

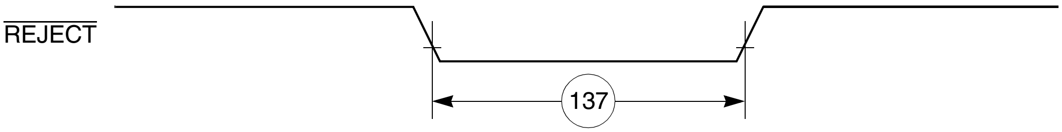


Figure 63. CAM Interface REJECT Timing Diagram

11.12 I^2C AC Electrical Specifications

Table 26 provides the I^2C ($SCL < 100$ kHz) timings.

Table 26. I^2C Timing ($SCL < 100$ kHz)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
200	SCL clock frequency (slave)	0	100	kHz
200	SCL clock frequency (master)[1]	1.5	100	kHz
202	Bus free time between transmissions	4.7	—	µs
203	Low period of SCL	4.7	—	µs
204	High period of SCL	4.0	—	µs
205	Start condition setup time	4.7	—	µs
206	Start condition hold time	4.0	—	µs
207	Data hold time	0	—	µs
208	Data setup time	250	—	ns
209	SDL/SCL rise time	—	1	µs
210	SDL/SCL fall time	—	300	ns
211	Stop condition setup time	4.7	—	µs

[1] SCL frequency is given by SCL = BRGCLK_frequency / ((BRG register + 3 × pre_scaler × 2).
The ratio SYNCCLK/(BRGCLK/pre_scaler) must be greater than or equal to 4/1.

Table 27 provides the I^2C ($SCL > 100$ kHz) timings.

Table 27. . I^2C Timing ($SCL > 100$ kHz)

Num	Characteristic	Expression	All Frequencies		Unit
			Min	Max	
200	SCL clock frequency (slave)	fSCL	0	BRGCLK/48	Hz
200	SCL clock frequency (master)[1]	fSCL	BRGCLK/16512	BRGCLK/48	Hz
202	Bus free time between transmissions		1/(2.2 * fSCL)	—	s
203	Low period of SCL		1/(2.2 * fSCL)	—	s
204	High period of SCL		1/(2.2 * fSCL)	—	s
205	Start condition setup time		1/(2.2 * fSCL)	—	s
206	Start condition hold time		1/(2.2 * fSCL)	—	s
207	Data hold time		0	—	s
208	Data setup time		1/(40 * fSCL)	—	s
209	SDL/SCL rise time		—	1/(10 * fSCL)	s
210	SDL/SCL fall time		—	1/(33 * fSCL)	s
211	Stop condition setup time		1/2(2.2 * fSCL)	—	s

[1] SCL frequency is given by SCL = BRGCLK_frequency / ((BRG register + 3) × pre_scaler × 2).
The ratio SYNCCLK/(BRGCLK / pre_scaler) must be greater than or equal to 4/1.

13.3 MII Async Inputs Signal Timing (MII_CRS, MII_COL)

Table 31 provides information on the MII async inputs signal timing.

Table 31. MII Async Inputs Signal Timing

Num	Characteristic	Min	Max	Unit
M9	MII_CRS, MII_COL minimum pulse width	1.5	—	MII_TX_CLK period

Figure 74 shows the MII asynchronous inputs signal timing diagram.

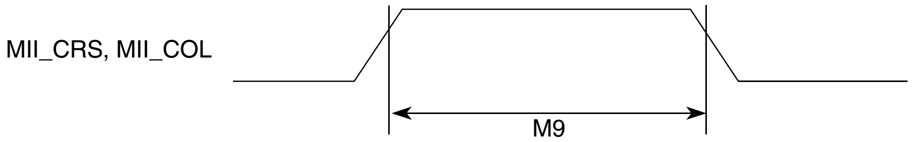


Figure 74. MII Async Inputs Timing Diagram

13.4 MII Serial Management Channel Timing (MII_MDIO, MII_MDC)

Table 32 provides information on the MII serial management channel signal timing. The FEC functions correctly with a maximum MDC frequency in excess of 2.5 MHz. The exact upper bound is under investigation.

Table 32. MII Serial Management Channel Timing

Num	Characteristic	Min	Max	Unit
M10	MII_MDC falling edge to MII_MDIO output invalid (minimum propagation delay)	0	—	ns
M11	MII_MDC falling edge to MII_MDIO output valid (max prop delay)	—	25	ns
M12	MII_MDIO (input) to MII_MDC rising edge setup	10	—	ns
M13	MII_MDIO (input) to MII_MDC rising edge hold	0	—	ns
M14	MII_MDC pulse width high	40%	60%	MII_MDC period
M15	MII_MDC pulse width low	40%	60%	MII_MDC period