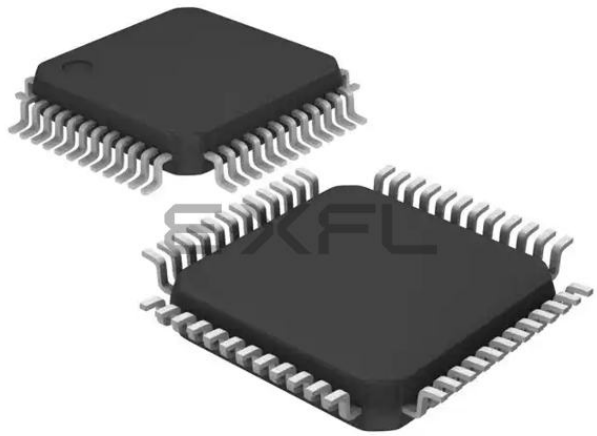

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0+ |
| Core Size | 32-Bit Single-Core |
| Speed | 50MHz |
| Connectivity | I²C, Microwire, SPI, SSI, SSP, UART/USART, USB |
| Peripherals | Brown-out Detect/Reset, DMA, POR, PWM, WDT |
| Number of I/O | 34 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 4K x 8 |
| RAM Size | 12K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.4V ~ 3.6V |
| Data Converters | A/D 8x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 48-LQFP |
| Supplier Device Package | 48-LQFP (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc11u66jbd48e |

**Table 3. Pin description**

*Pin functions are selected through the IOCON registers. See Table 2 for availability of USART3 and USART4 pin functions.*

| Symbol | LQFP48 | LQFP64 | LQFP100 | | Reset state[1] | Type | Description of pin functions |
|---|---|---|---|---|---|---|---|
| PIO0_6 | 23 | 29 | 44 | [6] | I; PU | IO | **PIO0_6 —** General-purpose port 0 input/output 6. |
| | | | | | | - | **R —** Reserved. |
| | | | | | | IO | **SSP0_SCK —** Serial clock for SSP0. |
| | | | | | | - | **R_4 —** Reserved. |
| PIO0_7 | 24 | 30 | 45 | [5] | I; PU | IO | **PIO0_7 —** General-purpose port 0 input/output 7 (high-current output driver). |
| | | | | | | I | **$\overline{\text{U0\_CTS}}$ —** Clear To Send input for USART. |
| | | | | | | - | **R_5 —** Reserved. |
| | | | | | | IO | **I2C1_SCL —** $I^2C$-bus clock input/output. This pin is not open-drain. |
| PIO0_8 | 26 | 37 | 58 | [6] | I; PU | IO | **PIO0_8 —** General-purpose port 0 input/output 8. |
| | | | | | | IO | **SSP0_MISO —** Master In Slave Out for SSP0. |
| | | | | | | O | **CT16B0_MAT0 —** Match output 0 for 16-bit timer 0. |
| | | | | | | - | **R_6 —** Reserved. |
| PIO0_9 | 27 | 38 | 59 | [6] | I; PU | IO | **PIO0_9 —** General-purpose port 0 input/output 9. |
| | | | | | | IO | **SSP0_MOSI —** Master Out Slave In for SSP0. |
| | | | | | | O | **CT16B0_MAT1 —** Match output 1 for 16-bit timer 0. |
| | | | | | | - | **R_7 —** Reserved. |
| SWCLK/PIO0_10 | 28 | 39 | 60 | [6] | I; PU | IO | **SWCLK —** Serial Wire Clock. SWCLK is enabled by default on this pin. In boundary scan mode: TCK (Test Clock). |
| | | | | | | IO | **PIO0_10 —** General-purpose digital input/output pin. |
| | | | | | | IO | **SSP0_SCK —** Serial clock for SSP0. |
| | | | | | | O | **CT16B0_MAT2 —** 16-bit timer0 MAT2 |
| TDI/PIO0_11 | 30 | 42 | 64 | [3] | I; PU | IO | **TDI —** Test Data In for JTAG interface. In boundary scan mode only. |
| | | | | | | IO | **PIO0_11 —** General-purpose digital input/output pin. |
| | | | | | | AI | **ADC_9 —** A/D converter, input channel 9. |
| | | | | | | O | **CT32B0_MAT3 —** Match output 3 for 32-bit timer 0. |
| | | | | | | O | **$\overline{\text{U1\_RTS}}$ —** Request To Send output for USART1. |
| | | | | | | IO | **U1_SCLK —** Serial clock input/output for USART1 in synchronous mode. |
| TMS/PIO0_12 | 31 | 43 | 66 | [3] | I; PU | IO | **TMS —** Test Mode Select for JTAG interface. In boundary scan mode only. |
| | | | | | | IO | **PIO0_12 —** General-purpose digital input/output pin. |
| | | | | | | AI | **ADC_8 —** A/D converter, input channel 8. |
| | | | | | | I | **CT32B1_CAP0 —** Capture input 0 for 32-bit timer 1. |
| | | | | | | I | **$\overline{\text{U1\_CTS}}$ —** Clear To Send input for USART1. |

**Table 3. Pin description**

*Pin functions are selected through the IOCON registers. See Table 2 for availability of USART3 and USART4 pin functions.*

| Symbol | LQFP48 | LQFP64 | LQFP100 | | Reset state[1] | Type | Description of pin functions |
|---|---|---|---|---|---|---|---|
| PIO0_20 | 10 | 12 | 17 | [6] | I; PU | IO | **PIO0_20 —** General-purpose digital input/output pin. |
| | | | | | | I | **CT16B1_CAP0 —** Capture input 0 for 16-bit timer 1. |
| | | | | | | I | **U2_RXD —** Receiver input for USART2. |
| PIO0_21 | 17 | 22 | 33 | [6] | I; PU | IO | **PIO0_21 —** General-purpose digital input/output pin. |
| | | | | | | O | **CT16B1_MAT0 —** Match output 0 for 16-bit timer 1. |
| | | | | | | IO | **SSP1_MOSI —** Master Out Slave In for SSP1. |
| PIO0_22 | 29 | 40 | 62 | [3] | I; PU | IO | **PIO0_22 —** General-purpose digital input/output pin. |
| | | | | | | AI | **ADC_11 —** A/D converter, input channel 11. |
| | | | | | | I | **CT16B1_CAP1 —** Capture input 1 for 16-bit timer 1. |
| | | | | | | IO | **SSP1_MISO —** Master In Slave Out for SSP1. |
| PIO0_23 | 39 | 52 | 83 | [3] | I; PU | IO | **PIO0_23 —** General-purpose digital input/output pin. |
| | | | | | | AI | **ADC_1 —** A/D converter, input channel 1. |
| | | | | | | - | **R_9 —** Reserved. |
| | | | | | | I | **$\overline{\text{U0\_RI}}$ —** Ring Indicator input for USART0. |
| | | | | | | IO | **SSP1_SSEL —** Slave select for SSP1. |
| PIO1_0 | - | 62 | 97 | [6] | I; PU | IO | **PIO1_0 —** General-purpose digital input/output pin. |
| | | | | | | O | **CT32B1_MAT0 —** Match output 0 for 32-bit timer 1. |
| | | | | | | - | **R_10 —** Reserved. |
| | | | | | | O | **U2_TXD —** Transmitter output for USART2. |
| PIO1_1 | - | - | 28 | [6] | I; PU | IO | **PIO1_1 —** General-purpose digital input/output pin. |
| | | | | | | O | **CT32B1_MAT1 —** Match output 1 for 32-bit timer 1. |
| | | | | | | - | **R_11 —** Reserved. |
| | | | | | | O | **$\overline{\text{U0\_DTR}}$ —** Data Terminal Ready output for USART0. |
| PIO1_2 | - | - | 55 | [6] | I; PU | IO | **PIO1_2 —** General-purpose digital input/output pin. |
| | | | | | | O | **CT32B1_MAT2 —** Match output 2 for 32-bit timer 1. |
| | | | | | | - | **R_12 —** Reserved. |
| | | | | | | I | **U1_RXD —** Receiver input for USART1. |
| PIO1_3 | - | - | 72 | [3] | I; PU | IO | **PIO1_3 —** General-purpose digital input/output pin. |
| | | | | | | O | **CT32B1_MAT3 —** Match output 3 for 32-bit timer 1. |
| | | | | | | - | **R_13 —** Reserved. |
| | | | | | | IO | **I2C1_SDA —** $I^2C$-bus data input/output (not open-drain). |
| | | | | | | AI | **ADC_5 —** A/D converter, input channel 5. |
| PIO1_4 | - | - | 23 | [6] | I; PU | IO | **PIO1_4 —** General-purpose digital input/output pin. |
| | | | | | | I | **CT32B1_CAP0 —** Capture input 0 for 32-bit timer 1. |
| | | | | | | - | **R_14 —** Reserved. |
| | | | | | | I | **$\overline{\text{U0\_DSR}}$ —** Data Set Ready input for USART0. |

**Table 3. Pin description**

*Pin functions are selected through the IOCON registers. See Table 2 for availability of USART3 and USART4 pin functions.*

| Symbol | LQFP48 | LQFP64 | LQFP100 | Reset state[1] | Type | Description of pin functions |
|---|---|---|---|---|---|---|
| VBAT | 47 | 63 | 99 | - | - | Battery supply. Supplies power to the RTC. If no battery is used, tie VBAT to VDD. |
| $V_{SSA}$ | 41 | 54 | 85 | - | - | Analog ground. $V_{SSA}$should typically be the same voltage as $V_{SS}$ but should be isolated to minimize noise and error. $V_{SSA}$ should be tied to $V_{SS}$ if the ADC is not used. |
| $V_{SS}$ | 43, 2, 5 | 57, 3, 7 | 91, 7, 11, 53, 70 | - | - | Ground. |

[1] Pin state at reset for default function: I = Input; AI = Analog Input; O = Output; PU = internal pull-up enabled; IA = inactive, no pull-up/down enabled;
F = floating; If the pins are not used, tie floating pins to ground or power to minimize power consumption.

[2] Special analog pad.

[3] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as analog input, digital section of the pad is disabled and the pin is not 5 V tolerant; includes digital, programmable filter.

[4] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as analog input, digital section of the pad is disabled and the pin is not 5 V tolerant; includes digital input glitch filter. WAKEUP pin. The wake-up pin function can be disabled and the pin can be used for other purposes if the RTC is enabled for waking up the part from Deep power-down mode.

[5] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis; includes high-current output driver.

[6] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis.

[7] $I^2C$-bus pin compliant with the $I^2C$-bus specification for $I^2C$ standard mode, $I^2C$ Fast-mode, and $I^2C$ Fast-mode Plus. The pin requires an external pull-up to provide output functionality. When power is switched off, this pin is floating and does not disturb the I2C lines. Open-drain configuration applies to all functions on this pin.

[8] 5 V tolerant pad. $\overline{\text{RESET}}$ functionality is not available in Deep power-down mode. Use the WAKEUP pin to reset the chip and wake up from Deep power-down mode. An external pull-up resistor is required on this pin for the Deep power-down mode.

[9] Pad provides USB functions. It is designed in accordance with the USB specification, revision 2.0 (Full-speed and Low-speed mode only). This pad is not 5 V tolerant.

[10] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog crystal oscillator connections. When configured for the crystal oscillator input/output, digital section of the pad is disabled and the pin is not 5 V tolerant; includes digital, programmable filter.

## 8.3 On-chip flash programming memory

The LPC11U6x contain up to 256 KB on-chip flash program memory. The flash can be programmed using In-System Programming (ISP) or In-Application Programming (IAP) via the on-chip bootloader software.

The flash memory is divided into 24 x 4 KB and 5 x 32 KB sectors. Individual pages of 256 byte each can be erased using the IAP erase page command.

## 8.4 EEPROM

The LPC11U6x contain 4 KB of on-chip byte-erasable and byte-programmable EEPROM data memory. The EEPROM can be programmed using In-Application Programming (IAP) via the on-chip bootloader software.

## 8.5 SRAM

The LPC11U6x contain a total of up to 36 KB on-chip static RAM memory. The main SRAM block contains either 8 KB, 16 KB, or 32 KB of main SRAM0. Two additional SRAM blocks of 2 KB (SRAM1 and USB SRAM) are located in separate areas of the memory map. See Figure 8.

## 8.6 On-chip ROM

The on-chip ROM contains the bootloader and the following Application Programming Interfaces (APIs):

- In-System Programming (ISP) and In-Application Programming (IAP) support for flash including IAP erase page command.
- IAP support for EEPROM
- USB API
- Power profiles for configuring power consumption and PLL settings
- 32-bit integer division routines
- APIs to use the following peripherals:
  - I2C
  - USART0 and USART1/2/3/4
  - DMA

## 8.7 Memory mapping

The LPC11U6x incorporates several distinct memory regions, shown in the following figures. Figure 8 shows the overall map of the entire address space from the user program viewpoint following reset. The interrupt vector area supports address remapping.

The AHB (Advanced High-performance Bus) peripheral area is 2 MB in size and is divided to allow for up to 128 peripherals. The APB (Advanced Peripheral Bus) peripheral area is 512 KB in size and is divided to allow for up to 32 peripherals. Each peripheral of either type is allocated 16 KB of space. This addressing scheme allows simplifying the address decoding for each peripheral.

### 8.8.1 Features

- Controls system exceptions and peripheral interrupts.
- In the LPC11U6x, the NVIC supports vectored interrupts for each of the peripherals and the eight pin interrupts. The following peripheral interrupts are ORed to contribute to one interrupt in the NVIC:
  - USART1, USART4
  - USART2, USART3
  - SCTimer0/PWM, SCTimer1/PWM
  - BOD, WWDT
  - ADC end-of-sequence A interrupt, threshold crossing interrupt
  - ADC end-of-sequence B interrupt, overrun interrupt
  - Flash, EEPROM
- Four programmable interrupt priority levels with hardware priority level masking.
- Software interrupt generation.

### 8.8.2 Interrupt sources

Each peripheral device has at least one interrupt line connected to the NVIC but can have several interrupt flags. Individual interrupt flags can also represent more than one interrupt source.

## 8.9 IOCON block

The IOCON block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on-chip peripherals.

Connect peripherals to the appropriate pins before activating the peripheral and before enabling any related interrupt.

Enabling an analog function disables the digital pad. However, the internal pull-up and pull-down resistors as well as the pin hysteresis must be disabled to obtain an accurate reading of the analog input.

### 8.9.1 Features

- Programmable pin function.
- Programmable pull-up, pull-down, or repeater mode.
- All pins (except PIO0_4 and PIO0_5) are pulled up to 3.3 V ($V_{DD}$ = 3.3 V) if their pull-up resistor is enabled.
- Programmable pseudo open-drain mode.
- Programmable (on/off) 10 ns glitch filter on pins PIO0_22, PIO0_23, PIO0_11 to PIO0_16, PIO1_3, PIO1_9, PIO1_22, and PIO1_29. The glitch filter is turned on by default.
- Programmable hysteresis.
- Programmable input inverter.

## 8.12 GPIO group interrupts

The GPIO pins can be used in several ways to set pins as inputs or outputs and use the inputs as combinations of level and edge sensitive interrupts. For each port/pin connected to one of the two the GPIO Grouped Interrupt blocks (GINT0 and GINT1), the GPIO grouped interrupt registers determine which pins are enabled to generate interrupts and w the active polarities of each of those inputs.

The GPIO grouped interrupt registers also select whether the interrupt output is level or edge triggered and whether it is based on the OR or the AND of all of the enabled inputs.

When the designated pattern is detected on the selected input pins, the GPIO grouped interrupt block generates an interrupt. If the part is in a power-savings mode, it first asynchronously wakes up the part prior to asserting the interrupt request. The interrupt request line can be cleared by writing a one to the interrupt status bit in the control register.

### 8.12.1 Features

- Two group interrupts are supported to reflect two distinct interrupt patterns.
- The inputs from any number of digital pins can be enabled to contribute to a combined group interrupt.
- The polarity of each input enabled for the group interrupt can be configured HIGH or LOW.
- Enabled interrupts can be logically combined through an OR or AND operation.
- The grouped interrupts can wake up the part from sleep, deep-sleep or power-down modes.

## 8.13 DMA controller

The DMA controller can access all memories and the USART and SSP peripherals using DMA requests. DMA transfers can also be triggered by internal events like the ADC interrupts, timer match outputs, the pin interrupts (PINT0 and PINT1) and the SCTimer DMA requests.

### 8.13.1 Features

- 16 channels with 14 channels connected to peripheral request inputs.
- DMA operations can be triggered by on-chip events or two pin interrupts. Each DMA channel can select one trigger input from 12 sources.
- Priority is user selectable for each channel.
- Continuous priority arbitration.
- Address cache with two entries.
- Efficient use of data bus.
- Supports single transfers up to 1,024 words.
- Address increment options allow packing and/or unpacking data.

- Optional warning interrupt can be generated at a programmable time before watchdog time-out.
- Software enables the WWDT, but a hardware reset or a watchdog reset/interrupt is required to disable the WWDT.
- Incorrect feed sequence causes reset or interrupt, if enabled.
- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{24} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The WatchDog Clock (WDCLK) source can be selected from the IRC or the dedicated watchdog oscillator (WDOsc). The clock source selection provides a wide range of potential timing choices of watchdog operation under different power conditions.

## 8.22 Real-Time Clock (RTC)

The RTC resides in a separate always-on voltage domain with battery back-up. The RTC uses an independent oscillator, also located in the always-on voltage domain.

### 8.22.1 Features

- 32-bit, 1 Hz RTC counter and associated match register for alarm generation.
- Separate 16-bit high-resolution/wake-up timer clocked at 1 kHz for 1 ms resolution with a more that one minute maximum time-out period.
- RTC alarm and high-resolution/wake-up timer time-out each generate independent interrupt requests. Either time-out can wake up the part from any of the low-power modes, including Deep power-down.

## 8.23 Analog-to-Digital Converter (ADC)

The ADC supports a resolution of 12 bit and fast conversion rates of up to 2 MSamples/s. Sequences of analog-to-digital conversions can be triggered by multiple sources. Possible trigger sources are the counter/timer match outputs and capture inputs and the ARM TXEV.

The ADC includes a hardware threshold compare function with zero-crossing detection.

### 8.23.1 Features

- 12-bit successive approximation analog to digital converter.
- 12-bit conversion rate of up to 2 MSamples/s.
- Temperature sensor voltage output selectable as internal voltage source for channel 0.
- Two configurable conversion sequences with independent triggers.
- Optional automatic high/low threshold comparison and zero-crossing detection.
- Power-down mode and low-power operating mode.
- Measurement range VREFN to VREFP (typically 3 V; not to exceed $V_{DDA}$ voltage level).
- Burst conversion mode for single or multiple inputs.

## 8.24 Temperature sensor

The temperature sensor transducer uses an intrinsic pn-junction diode reference and outputs a CTAT voltage (Complement To Absolute Temperature). The output voltage varies inversely with device temperature with an absolute accuracy of better than ±5 °C over the full temperature range (−40 °C to +105 °C) for typical samples. The temperature sensor is approximately linear with a slight curvature. The output voltage is measured over different ranges of temperatures and fit with linear-least-square lines.

After power-up and after switching the input channels of the ADC, the temperature sensor output must be allowed to settle to its stable value before it can be used as an accurate ADC input.

For an accurate measurement of the temperature sensor by the ADC, the ADC must be configured in single-channel burst mode. The last value of a nine-conversion (or more) burst provides an accurate result.

1. CRP1 disables access to the chip via the SWD and allows partial flash update (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors cannot be erased.
2. CRP2 disables access to the chip via the SWD and only allows full flash erase and update using a reduced set of the ISP commands.
3. Running an application with level CRP3 selected, fully disables any access to the chip via the SWD pins and the ISP. This mode effectively disables ISP override using PIO0_1 pin as well. If necessary, the application must provide a flash update mechanism using IAP calls or using a call to the reinvoke ISP command to enable flash update via the USART.

**CAUTION**

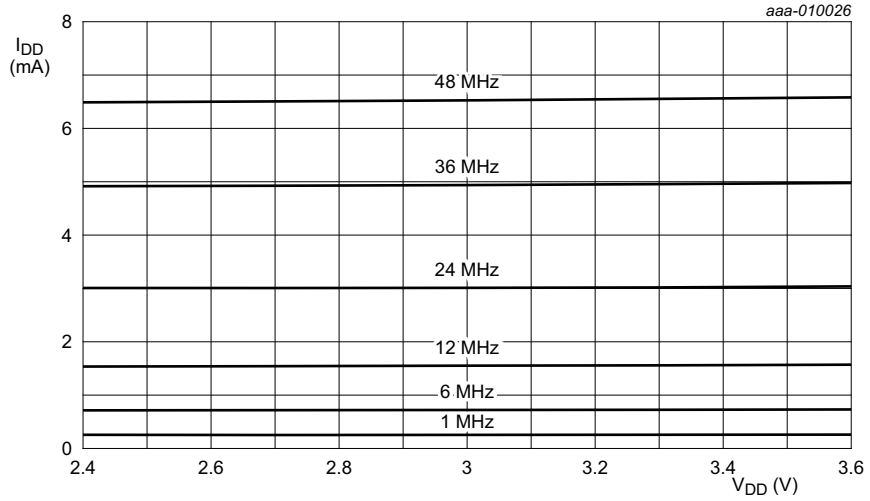
If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

In addition to the three CRP levels, sampling of pin PIO0_1 for valid user code can be disabled. For details, see the *LPC11U6x user manual*.

## 11.1 Power consumption

Power measurements in Active, Sleep, and Deep-sleep modes were performed under the following conditions:

- Configure all pins as GPIO with pull-up resistor disabled in the IOCON block.
- Configure GPIO pins as outputs using the GPIO DIR register.
- Write 1 to the GPIO CLR register to drive the outputs LOW.



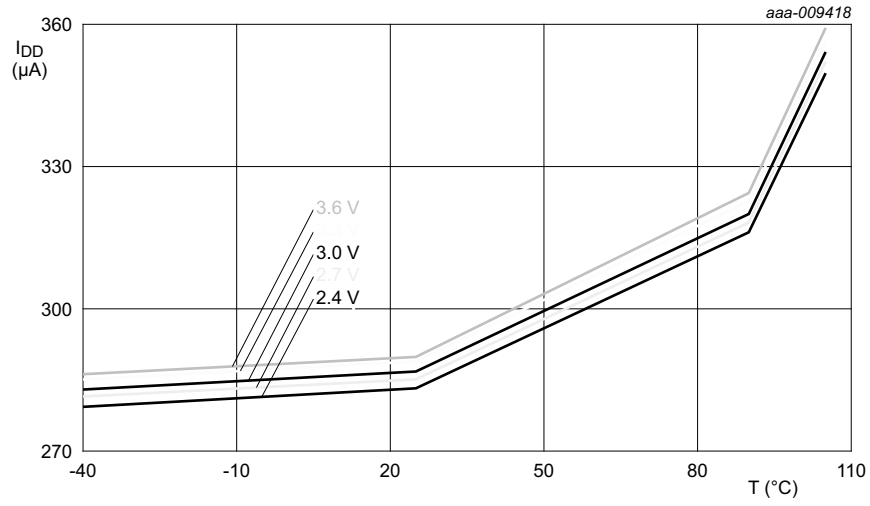

Conditions: $T_{amb}$ = 25 °C; active mode entered executing code `while(1){}` from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F), all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled; low-current mode.

1 MHz to 6 MHz: IRC enabled; PLL disabled.

12 MHz: IRC enabled; PLL disabled.

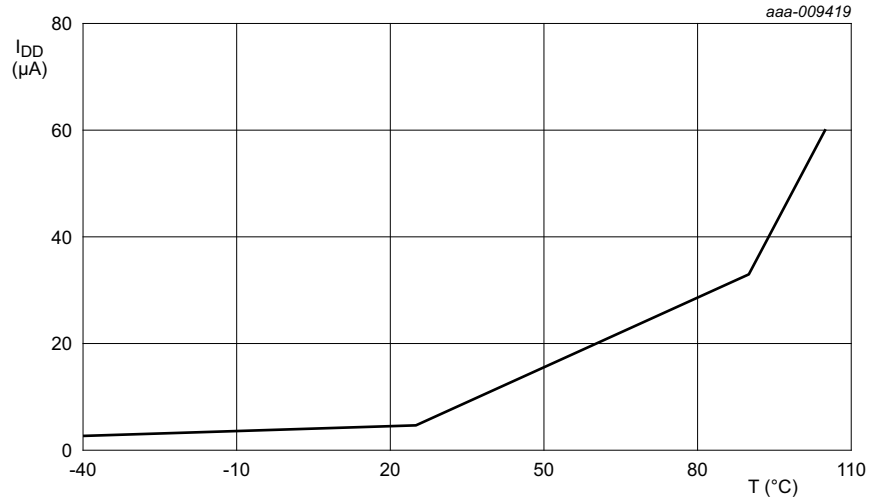
24 MHz to 50 MHz: IRC disabled; PLL enabled; sysosc enabled.

**Fig 14. Active mode: Typical supply current $I_{DD}$ versus supply voltage $V_{DD}$**




Conditions: BOD disabled; all oscillators and analog blocks disabled

**Fig 17. Deep-sleep mode: Typical supply current $I_{DD}$ versus temperature for different supply voltages $V_{DD}$**




Conditions: BOD disabled; all oscillators and analog blocks disabled; $V_{DD}$ = 2.4 V to 3.6 V.

**Fig 18. Power-down mode: Typical supply current $I_{DD}$ versus temperature for different supply voltages $V_{DD}$**

The power profiles optimize the chip performance for power consumption or core efficiency by controlling the flash access and core power. As shown in Figure 21 and Figure 22, different power modes result in different CoreMark scores reflecting the trade-off of efficiency and power consumption. In CPU and efficiency modes, the power profiles aim to keep the core efficiency at a maximum for the given system frequency. Depending on optimal flash access parameters that change with frequency, the CoreMark score and also the power consumption change. Since the compiled code for CoreMark testing runs out of flash memory, the CoreMark score depends on the compiler version.

## 11.3 Peripheral power consumption

The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled in the SYSAHBCLKCFG and PDRUNCFG (for analog blocks) registers. All other blocks are disabled in both registers and no code accessing the peripheral is executed except for the ADC. Measured on a typical sample at $T_{amb}$ = 25 °C. Unless noted otherwise, the system oscillator and PLL are running in both measurements.

The supply currents are shown for system clock frequencies of 12 MHz and 48 MHz.

**Table 9. Power consumption for individual analog and digital blocks**

| Peripheral | Typical supply current in mA | | | Notes |
|---|---|---|---|---|
| | n/a | 12 MHz | 48 MHz | |
| IRC | 0.24 | - | - | System oscillator running; PLL off; independent of main clock frequency. |
| System oscillator at 12 MHz | 0.28 | - | - | IRC running; PLL off; independent of main clock frequency. |
| WatchDog oscillator at 600 kHz/2 | 0 | - | - | System oscillator running; PLL off; independent of main clock frequency. |
| BOD | 0.05 | - | - | Independent of main clock frequency. |
| System PLL | 0.25 | - | - | - |
| USB PLL | 0.37 | - | - | - |
| CLKOUT | - | 0.25 | 0.89 | System PLL is source of CLKOUT. |
| ROM | - | 0.09 | 0.37 | - |
| FLASHREG | - | 0.17 | 0.66 | - |
| FLASHARRAY | - | 0.13 | 0.52 | - |
| SRAM1 | - | 0.15 | 0.59 | - |
| USB SRAM | - | 0.14 | 0.56 | - |
| GPIO + pin interrupt/pattern match | - | 0.18 | 0.69 | GPIO pins configured as outputs and set to LOW. Direction and pin state are maintained if the GPIO is disabled in the SYSAHBCLKCFG register. |
| IOCON | - | 0.08 | 0.30 | - |
| SCTimer0/PWM + SCTimer1/PWM | - | 0.29 | 1.1 | - |
| CT16B0 | - | 0.05 | 0.17 | - |
| CT16B1 | - | 0.04 | 0.16 | - |
| CT32B0 | - | 0.04 | 0.13 | - |
| CT32B1 | - | 0.03 | 0.13 | - |

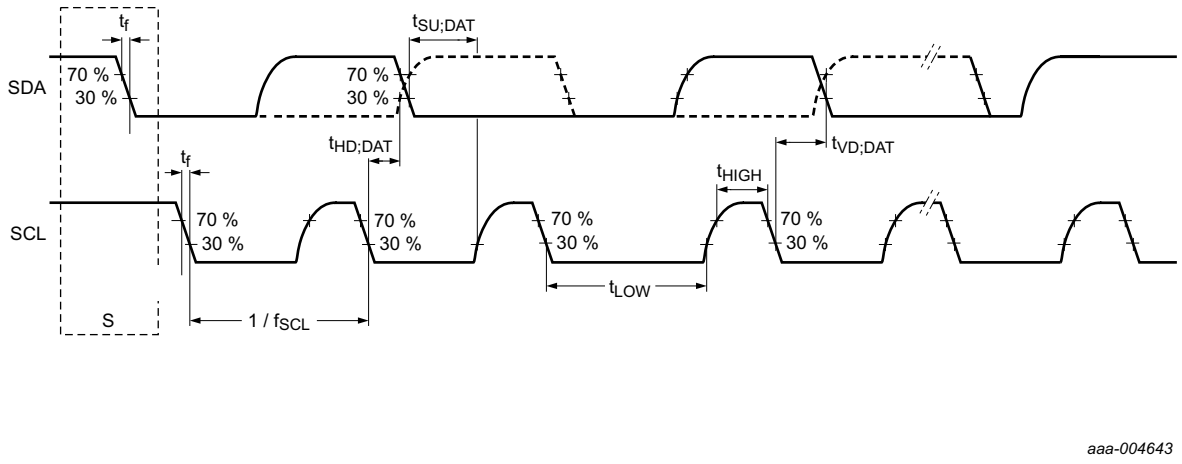



**Fig 31. $I^2C$-bus pins clock timing**

## 12.6 SSP interface

**Table 17. Dynamic characteristics of SPI pins in SPI mode**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **SPI master (in SPI mode)** | | | | | | | |
| $T_{cy(clk)}$ | clock cycle time | full-duplex mode | [1] | 50 | - | - | ns |
| | | when only transmitting | [1] | 40 | | | ns |
| $t_{DS}$ | data set-up time | in SPI mode | [2] | 15 | - | - | ns |
| $t_{DH}$ | data hold time | in SPI mode | [2] | 0 | - | - | ns |
| $t_{v(Q)}$ | data output valid time | in SPI mode | [2] | - | - | 10 | ns |
| $t_{h(Q)}$ | data output hold time | in SPI mode | [2] | 0 | - | - | ns |
| **SPI slave (in SPI mode)** | | | | | | | |
| $T_{cy(PCLK)}$ | PCLK cycle time | | | 20 | - | - | ns |
| $t_{DS}$ | data set-up time | in SPI mode | [3][4] | 0 | - | - | ns |
| $t_{DH}$ | data hold time | in SPI mode | [3][4] | $3 \times T_{cy(PCLK)} + 4$ | - | - | ns |
| $t_{v(Q)}$ | data output valid time | in SPI mode | [3][4] | - | - | $3 \times T_{cy(PCLK)} + 11$ | ns |
| $t_{h(Q)}$ | data output hold time | in SPI mode | [3][4] | - | - | $2 \times T_{cy(PCLK)} + 5$ | ns |

[1] $T_{cy(clk)} = (SSPCLKDIV \times (1 + SCR) \times CPSDVSR) / f_{main}$. The clock cycle time derived from the SPI bit rate $T_{cy(clk)}$ is a function of the main clock frequency $f_{main}$, the SPI peripheral clock divider (SSPCLKDIV), the SPI SCR parameter (specified in the SSP0CR0 register), and the SPI CPSDVSR parameter (specified in the SPI clock prescale register).

[2] $T_{amb} = -40$ °C to 105 °C; 2.4 V ≤ $V_{DD}$ ≤ 3.6 V.

[3] $T_{cy(clk)} = 12 \times T_{cy(PCLK)}$.

[4] $T_{amb}$ = 25 °C; for normal voltage supply range: $V_{DD}$ = 3.3 V.

## 12.7 USART interface

The maximum USART bit rate for all USARTs is 3.125 Mbit/s in asynchronous mode and 10 Mbit/s in synchronous slave and master mode.

**Table 18. USART dynamic characteristics USART0**

*$T_{amb}$ = −40 °C to 105 °C; 2.4 V <= $V_{DD}$ <= 3.6 V; $C_L$ = 10 pF. Simulated parameters sampled at the 50 % level of the falling or rising edge; values guaranteed by design.*

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $T_{cy(clk)}$ | clock cycle time [1] | 100 | - | ns |
| **USART master (in synchronous mode)** | | | | |
| $t_{su(D)}$ | data input set-up time | 44 | - | ns |
| $t_{h(D)}$ | data input hold time | 0 | - | ns |
| $t_{v(Q)}$ | data output valid time | - | 10 | ns |
| $t_{h(Q)}$ | data output hold time | 0 | - | ns |
| **USART slave (in synchronous mode)** | | | | |
| $t_{su(D)}$ | data input set-up time | 5 | - | ns |
| $t_{h(D)}$ | data input hold time | 20 | - | ns |
| $t_{v(Q)}$ | data output valid time | - | 40 | ns |
| $t_{h(Q)}$ | data output hold time | 25 | - | ns |

[1] $T_{cy(clk)}$ = (main clock cycle time)/(UARTCLKDIV x 2 x (256 x DLM + DLL)). See the LPC11U6x *User manual UM10732*.

**Table 19. USART dynamic characteristics USART1/2/3/4**

*$T_{amb}$ = −40 °C to 105 °C; 2.4 V <= $V_{DD}$ <= 3.6 V; $C_L$ = 10 pF. Simulated parameters sampled at the 50 % level of the falling or rising edge; values guaranteed by design.*

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $T_{cy(clk)}$ | clock cycle time [1] | 100 | - | ns |
| **USART master (in synchronous mode)** | | | | |
| $t_{su(D)}$ | data input set-up time | 44 | - | ns |
| $t_{h(D)}$ | data input hold time | 0 | - | ns |
| $t_{v(Q)}$ | data output valid time | - | 10 | ns |
| $t_{h(Q)}$ | data output hold time | 0 | - | ns |
| **USART slave (in synchronous mode)** | | | | |
| $t_{su(D)}$ | data input set-up time | 5 | - | ns |
| $t_{h(D)}$ | data input hold time | 0 | - | ns |
| $t_{v(Q)}$ | data output valid time | - | 40 | ns |
| $t_{h(Q)}$ | data output hold time | 20 | - | ns |

[1] $T_{cy(clk)}$ = U_PCLK/BRGVAL. See the LPC11U6x *User manual UM10732*.

**Table 22. 12-bit ADC static characteristics**

*$T_{amb}$ = −40 °C to +105 °C; $V_{DD}$ = 2.4 V to 3.6 V; VREFP = $V_{DDA}$; $V_{SSA}$ = 0; VREFN = $V_{SSA}$. ADC calibrated at T = 25 °C.*

| Symbol | Parameter | Conditions | Min | Typ [1] | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IA}$ | analog input voltage | [2] | 0 | - | $V_{DDA}$ | V |
| $C_{ia}$ | analog input capacitance | [3] | - | - | 0.32 | pF |
| $f_{clk(ADC)}$ | ADC clock frequency | $V_{DDA} \geq 2.7$ V | | | 50 | MHz |
| | | $V_{DDA} \geq 2.4$ V | | | 25 | MHz |
| $f_s$ | sampling frequency | $V_{DDA} \geq 2.7$ V | - | - | 2 | Msamples/s |
| | | $V_{DDA} \geq 2.4$ V | - | - | 1 | Msamples/s |
| $E_D$ | differential linearity error | [4] | - | - | ±2.5 | LSB |
| $E_{L(adj)}$ | integral non-linearity | [5] | - | - | ±2.5 | LSB |
| $E_O$ | offset error | [6] | - | - | ±4.5 | LSB |
| $V_{err(FS)}$ | full-scale error voltage | [7] | - | - | ±0.5 | % |
| $Z_i$ | input impedance | $f_s$ = 2 Msamples/s [8][9] | 0.1 | - | - | MΩ |

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] The input resistance of ADC channel 0 is higher than for all other channels.

[3] $C_{ia}$ represents the external capacitance on the analog input channel for sampling speeds of 2 Msamples/s.

[4] The differential linearity error ($E_D$) is the difference between the actual step width and the ideal step width. See Figure 35.

[5] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 35.

[6] The offset error ($E_O$) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 35.

[7] The full-scale error voltage or gain error ($E_G$) is the difference between the straight-line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 35.

[8] $T_{amb}$ = 25 °C; maximum sampling frequency $f_s$ = 2 Msamples/s and analog input capacitance $C_{ia}$ = 0.32 pF.

[9] Input impedance $Z_i$ is inversely proportional to the sampling frequency and the total input capacity including $C_{ia}$: $Z_i \propto 1 / (f_s \times C_i)$. See Table 8 for $C_{io}$.

One method is to use a voltage divider to connect the USB_VBUS pin to the VBUS on the USB connector. The voltage divider ratio should be such that the USB_VBUS pin is greater than 0.7 $V_{DD}$ to indicate a logic HIGH while below the 3.6 V allowable maximum voltage.

For the following operating conditions

$VBUS_{max}$ = 5.25 V

$V_{DD}$ = 3.6 V,

the voltage divider should provide a reduction of 3.6 V/5.25 V or ~0.686 V.

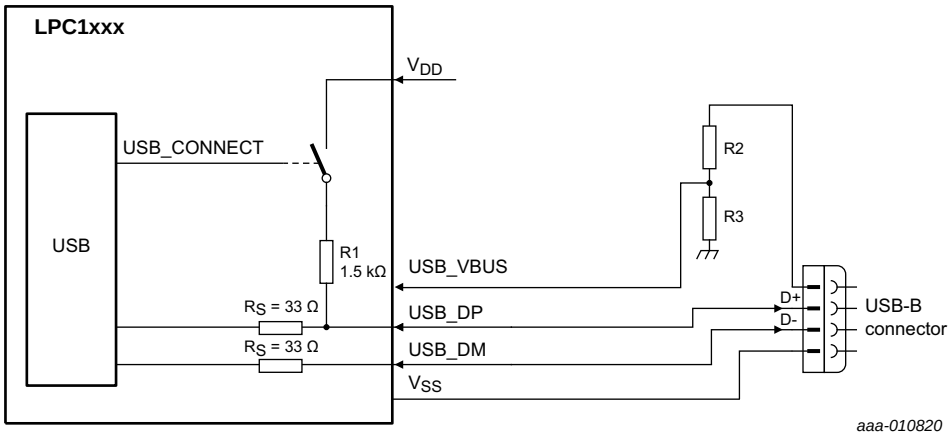



**Fig 38. USB interface on a self-powered device where USB_VBUS = 5 V**

The USB_CONNECT function can be enabled internally by setting the DCON bit in the DEVCMDSTAT register to prevent the USB from timing out when there is a significant delay between power-up and handling USB traffic. External circuitry is not required for the USB_CONNECT functionality.

## 14.6 RTC oscillator component selection

The 32 kHz crystal must be connected to the part via the RTCXIN and RTCXOUT pins as shown in Figure 43. If the RTC is not used, the RTCXIN pin can be grounded.

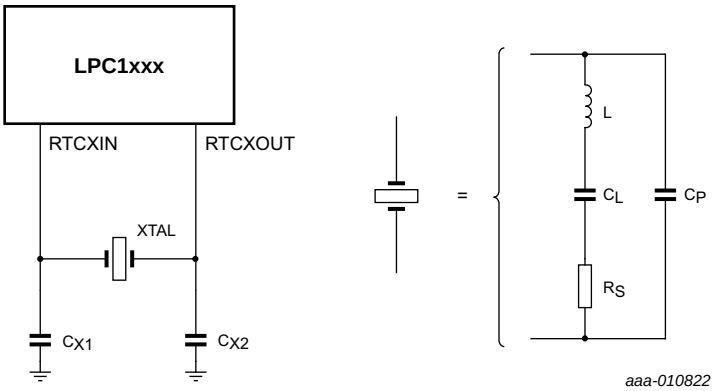



**Fig 43. RTC oscillator components**

Select $C_{x1}$ and $C_{x2}$ based on the external 32 kHz crystal used in the application circuitry. The pad capacitance $C_P$ of the RTCXIN and RTCXOUT pad is 3 pF. If the load capacitance of the external crystal is $C_L$, the optimal $C_{x1}$ and $C_{x2}$ can be selected as:

$C_{x1} = C_{x2} = 2 \times C_L - C_P$

## 14.7 Connecting power, clocks, and debug functions

Figure 44 shows the basic board connections used to power the LPC11U6x, connect the external crystal and the 32 kHz oscillator for the RTC, and provide debug capabilities via the serial wire port.

## 14.10 ElectroMagnetic Compatibility (EMC)

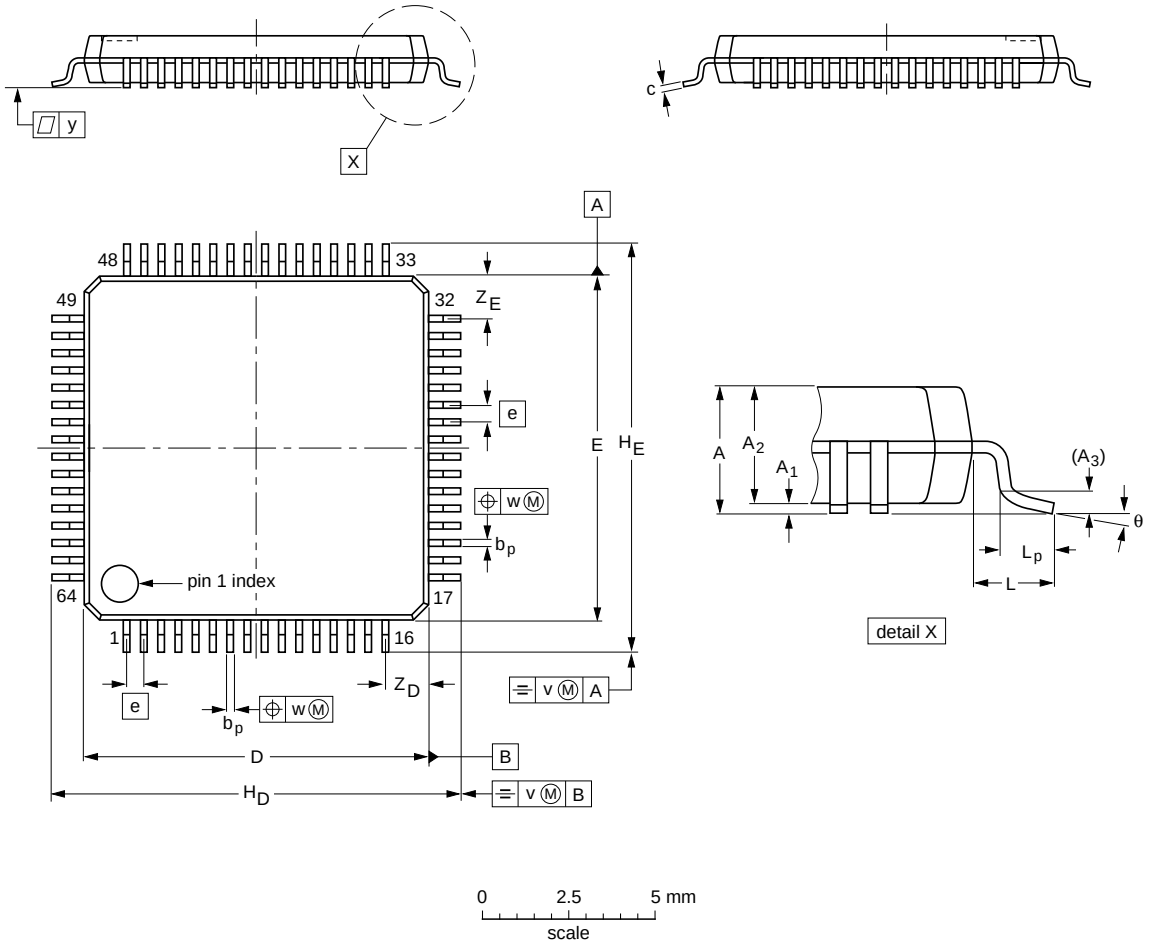
Radiated emission measurements according to the IEC61967-2 standard using the TEM-cell method are shown for part LPC11U68JBD100.

**Table 30. ElectroMagnetic Compatibility (EMC) for part LPC11U68 (TEM-cell method)**
*$V_{DD}$ = 3.3 V; $T_{amb}$ = 25 °C.*

| Parameter | Frequency band | System clock = | | | | Unit |
|---|---|---|---|---|---|---|
| | | 12 MHz | 24 MHz | 36 MHz | 48 MHz | |
| **Input clock: IRC (12 MHz)** | | | | | | |
| maximum peak level | 1 MHz to 30 MHz | -5 | -5 | -5 | -5 | dBμV |
| | 30 MHz to 150 MHz | -1 | 0 | +4 | +4 | dBμV |
| | 150 MHz to 1 GHz | -1 | 0 | +4 | +4 | dBμV |
| IEC level[1] | - | O | O | O | O | - |
| **Input clock: crystal oscillator (12 MHz)** | | | | | | |
| maximum peak level | 1 MHz to 30 MHz | -2 | –6 | -4 | -5 | dBμV |
| | 30 MHz to 150 MHz | -1 | 0 | +3 | +3 | dBμV |
| | 150 MHz to 1 GHz | -2 | 0 | +2 | +5 | dBμV |
| IEC level[1] | - | O | O | O | O | - |

[1] IEC levels refer to Appendix D in the IEC61967-2 Specification.

**LQFP64: plastic low profile quad flat package; 64 leads; body 10 x 10 x 1.4 mm** **SOT314-2**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_D$ | $H_E$ | L | $L_p$ | v | w | y | $Z_D^{(1)}$ | $Z_E^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.6 | 0.20<br>0.05 | 1.45<br>1.35 | 0.25 | 0.27<br>0.17 | 0.18<br>0.12 | 10.1<br>9.9 | 10.1<br>9.9 | 0.5 | 12.15<br>11.85 | 12.15<br>11.85 | 1 | 0.75<br>0.45 | 0.2 | 0.12 | 0.1 | 1.45<br>1.05 | 1.45<br>1.05 | $7^o$<br>$0^o$ |

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT314-2 | 136E10 | MS-026 | | | | ~~00-01-19~~<br>03-02-25 |

**Fig 46. Package outline LQFP64 (SOT314-2)**

# 18. Revision history

**Table 31. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| LPC11U6x v.1.3 | 20160907 | Product data sheet | - | LPC11U6x v.1.2 |
| Modifications: | • Section 14.10 “ElectroMagnetic Compatibility (EMC)” added.<br>• Replaced CT16B0_CAP1 with CT16B0_CAP2 for pin PI01_21. See Table 3 “Pin description”.<br>• Replaced CT32B0_CAP1 with CT32B0_CAP2 for pin PIO1_6 and pin PIO1_29. See Table 3 “Pin description”.<br>• Updated Figure 7 “AHB multilayer matrix”: HS GPIO connects with M0+ Core, not with DMA or USB. | | | |
| LPC11U6x v.1.2 | 20140526 | Product data sheet | - | LPC11U6x v.1.1 |
| Modifications: | • Part marking updated with revision indicator.<br>• Changed recommendation for VBAT connection if unused: Tie to VDD. See Table 3 “Pin description”.<br>• Section 14.7 “Connecting power, clocks, and debug functions” added.<br>• Section 14.9 “Pin states in different power modes” added.<br>• Remark added about using the regulator in the USB bus-powered set-up. See Section 14.3 “Suggested USB interface solutions”.<br>• Figure 39 “USB interface on a bus-powered device” changed to show USB_VBUS connection to part.<br>• Parts added: LPC11U67JBD100, LPC11U67JBD64, LPC11U66JBD48. | | | |
| LPC11U6x v.1.1 | 20140312 | Product data sheet | - | LPC11U6x v.1 |
| Modifications: | • Parameter $R_I$ renamed to $Z_I$ (input impedance) in Table 22.<br>• Description of the internal USB_CONNECT function clarified in Section 14.3 “Suggested USB interface solutions”. The USB_CONNECT function can be set internally by software and does not require external circuitry.<br>• Parameter Cia corrected in Table 22 “12-bit ADC static characteristics”.<br>• Figure 36 “ADC input impedance” added.<br>• Parameter pin capacitance added in Table 8.<br>• Pin description for VBAT updated: If no battery is used, tie VBAT to VDD or to ground. See Table 3.<br>• Pin description for $\overline{\text{RESET}}$/PIO0_0 updated: In deep power-down mode, this pin must be pulled HIGH externally. The $\overline{\text{RESET}}$ pin can be left unconnected or be used as a GPIO pin if an external $\overline{\text{RESET}}$ function is not needed. See Table 3.<br>• Pin functions TMS, TDI, TDO, and $\overline{\text{TRST}}$ changed to default function in Table 3.<br>• Pin description table updated for clarity (VBAT, I2C-bus pins, WAKEUP pin).<br>• Section 14.1 “ADC usage notes” added.<br>• Use of USB_CONNECT signal explained when VBUS is not connected. See Section 14.3. | | | |
| LPC11U6x v.1 | 20140117 | Product data sheet | - | - |